1993 SEMINAR REFERENCE BOOK

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LINEAR DESIGN SEMINAR

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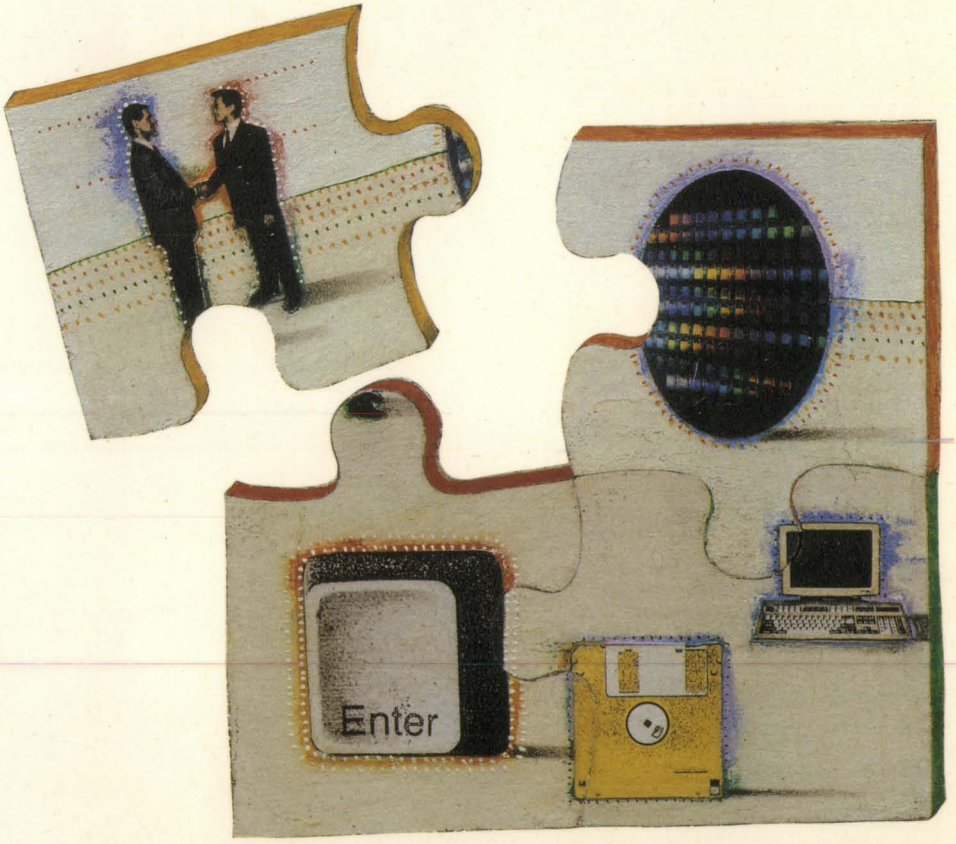

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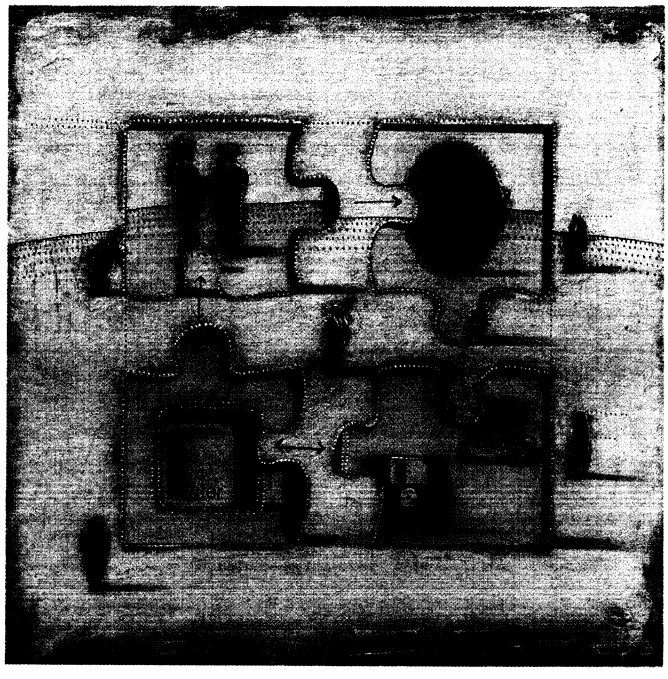

EXTENDING YOUR REACH WITH TOTAL INTEGRATION

TEXAS INSTRUMENTS

1993
LINEAR DESIGN SEMINAR

Written by members of the Technical Staff, Linear Products Division
Texas Instruments

Tim Ardley
Geoffrey Arnold
Bridget Barrett
Brian Colligan
David Cotton
Dave Cox
Andrew Faulkner
Kevin Gingerich
Steve Goacher
Julie Holland
Ross Hugo
Mick Maytum
Al Miller
Richard Nail
Simon Ramsdale
Derrick Robinson
Alun Webber
Charles Wray

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IMPORTANT NOTICE

CONTENTS

Section 1
Introduction

1. Linear Design Seminar Structure

This 1993 Texas Instruments Linear Design Seminar is intended to demonstrate how a wide variety of problems frequently encountered by analogue, mixed-mode, and Data Transmission engineers can be solved using T.I.'s latest Linear products.

In simple terms, Texas Instruments' Linear products address the generic task of joining the real analogue world we inhabit to the world of electronic digital processing. The structure of this seminar reflects this by partitioning the general electronic 'system' into functional blocks which form separate seminar sections. For each block, major design principles and concepts will be reviewed, and then illustrated practically with new products that address important application concerns.

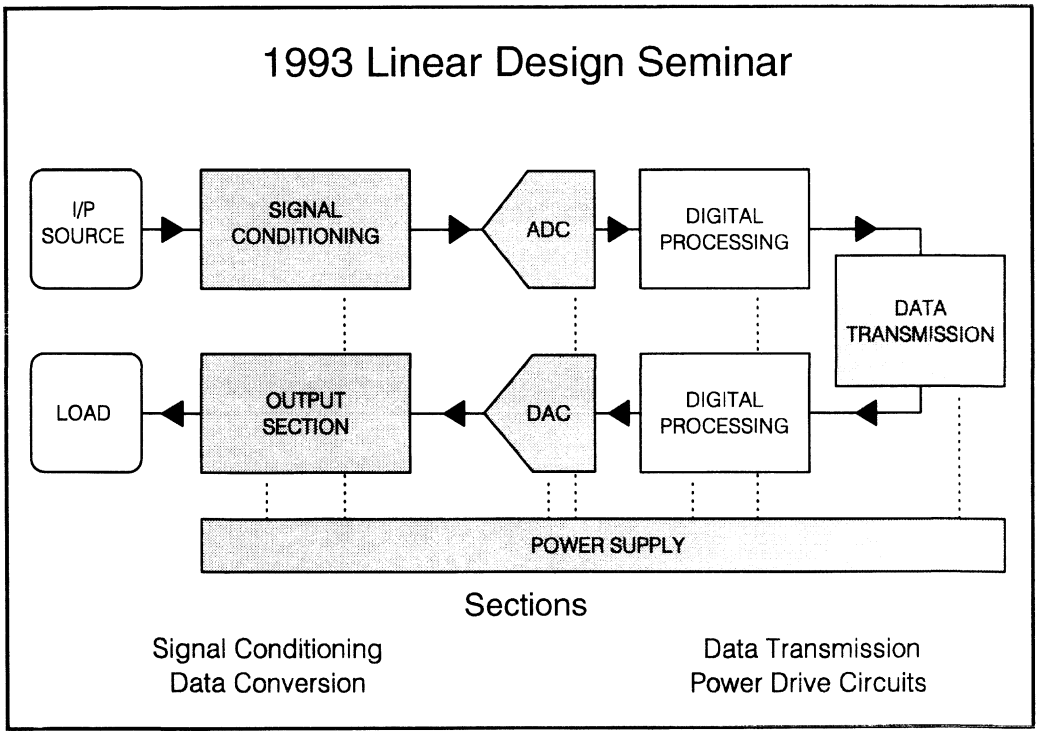

Figure 1.1 - 1993 Linear Design Seminar

The four parts of this seminar are:

Signal Conditioning

Data Conversion

Data Transmission

Power Drive Circuits

In the **Signal Conditioning** section we shall consider how to use products in ac, dc and single supply applications. The use of Texas Instruments new range of 3 volt and high temperature analogue products will be specifically discussed.

The **Data Conversion** section addresses the choice of A-D and D-A converters for specific applications. Both general and application specific converters will be described, including complete acquisition systems on a single chip. Guidance will be given on how to use them. Included in this section is an introduction to the Texas Instruments family of Video Interface Palettes.

The **Data Transmission** section discusses the key specifications of the EIA/TIA-232E, RS-485, and SCSI data communication standards. Discussion will focus on the physical layer and on devices operating within these communication standards. Specific topics covered will be the practical relationship between data-rate and transmission distance, and transmission quality measurement.

At the output side of digital systems there is often the need to deliver significant power to a load; and to protect the small-signal digital part of the system from damage from the high power levels in the world outside. In the **Power Drive Circuits** section we shall discuss how to apply the latest Texas Instruments integrated power devices to motor, lamp and solenoid loads.

2. Integration and the Technology Roadmap

Many of the products in this Linear Design Seminar are more than simply analogue devices. For electronics systems to remain competitive in an increasingly global market, ever greater integration is demanded to increase functionality and reduce both cost and size. Texas Instruments fully recognises this and a common high-volume silicon technology roadmap has been laid down. This will enable the integration of high performance analogue, digital, memory and processor core functions in the near future. Further, significant investment has been made in high-volume, sub-micron geometry silicon wafer processing capacity world wide.

In this Linear Design Seminar, we shall show, of course, new and purely analogue components such as operational amplifiers and voltage regulators. These offer specific benefits to designers of classic analogue circuits. However, and perhaps even more significantly, we shall also discuss products which show the increasing integration on a single chip of the precision analogue world, and the high density and high speed digital world. Moreover, this integration can increasingly be found in catalogue, as well as custom products. Examples of complete sub-systems on a chip that will be discussed in detail are the Video Interface Palettes, and Voice-Band Audio Processors.

Last, sub-micron silicon technology clearly essential for higher capacity memory and higher speed digital processors, may seem at first sight to offer little to the specialist analogue engineer. However, we shall show that specific data conversion problems pose similar demands to high speed digital processing. Further, even in the world of power drives we shall show how specific application benefits can be derived from T.I's sub-micron silicon technologies.

Thus, we believe that through an integrated high density roadmap Texas Instruments will bring value to the inhabitants of digital and 'real' analogue world alike.

Section 2
Signal Conditioning

Section Contributions by:

Simon Ramsdale
Tim Ardley
Brian Colligan
Steve Goacher
Derrick Robinson

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Section 2.

1. Introduction

1.1. Signal Conditioning System

This section of the seminar will discuss some of Texas Instruments' high performance Linear signal conditioning products

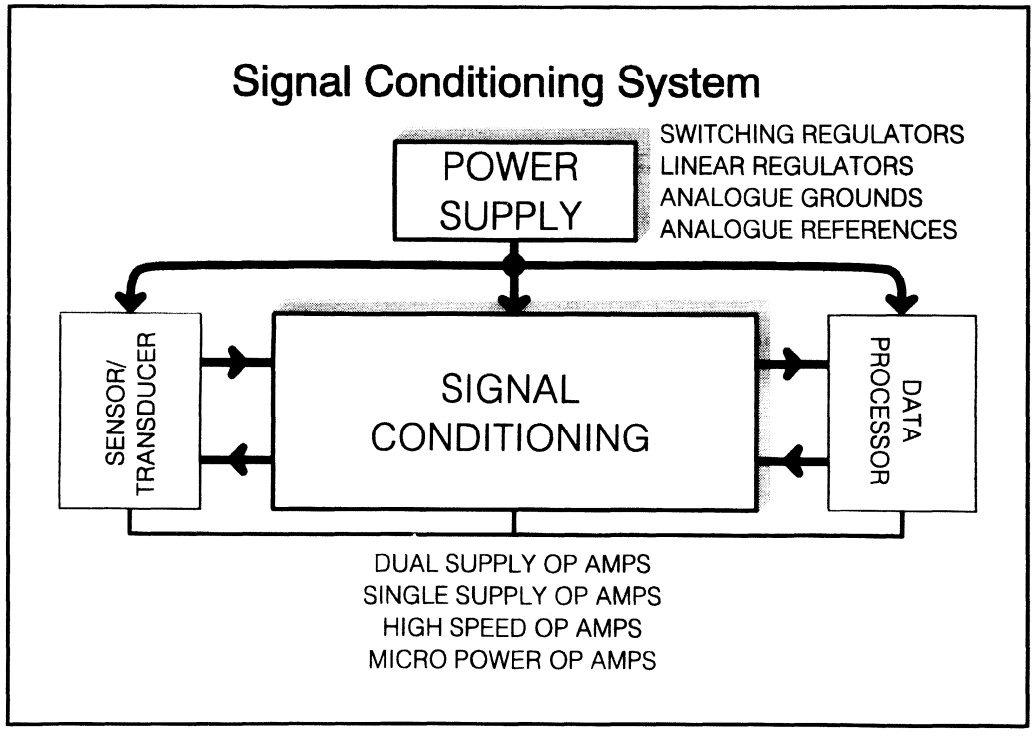


Figure 2.1.01. - Signal Conditioning System

Designing both Analogue and Digital systems entails some consideration of the supplies required. So, when considering a whole signal conditioning system, be it just analogue or with analogue preconditioning and digital processing of the data fed back from the sensors, the power supply must be as carefully considered as the op amps used.

Op amps will normally fall into two fundamental categories, although devices that fit into the same category may vary enormously on other parameters. The simplest category is whether or not they can function from a single supply. These categories can then be further split, with high speed op amps fitting with the dual supply op amps, while micro-power op amps fit with the single supply op amps.

The power supply will come from one of two sources:- mains powered or battery powered, and with the correct choice of regulator, the efficiency and board space savings can be maximised. The power supply regulation will normally be done by switching regulators and/or linear regulators.

Switching regulators come into their own when dealing with either large drop-out voltages (the voltage drop between the input and output), large output currents or where the output voltage must be increased above the input voltage.

Linear regulators are normally much more easier to design with and are much less noisy. There are however different forms of Linear regulators;- serial and shunt regulators. The serial regulator acts as a variable resistor between the input and output; the resistance will decrease as the output increases. A shunt regulator also works as a variable resistor, but this time the variable resistor is between the output and ground with a fixed resistor between the input and the output. As the output current increases, the variable resistor increases thus shunting less current to ground.

1.2. Designing the Right Device

TI is and will continue to be a leading supplier of cost effective performance operational amplifiers. To maintain this position, performance products must be developed which satisfy the demands of both the system design engineers and the end equipment. TI, must, therefore understand exactly what these requirements are.

To be able to provide the right op amps for the market place, any company must have a clear understanding of 'The Total Need'. This understanding must reach beyond the 'Quest for the Ideal op amp ' - many other factors need to be considered.

TI has identified the following areas as being crucial in the development and supply of performance amplifiers;

1.2.1. Market and System Understanding

TI focuses its products at particular applications and market segments. By understanding actual system requirements it is possible to provide devices which are highly suited to the actual end equipment. TI has op amps ideally suited to applications in the following areas:- Automotive, Telecom, Instrumentation, Test and Measurement, Industrial Control, and Audio. By understanding the demands of these systems, an op amps parameters can be fully optimised.

1.2.2. Characterisation and Design Support Material

Having an operational amplifier which performs well is not enough - it must also be easy to use and its particular characteristics well understood. TI, like many other companies, is putting significant effort into giving excellent support and design information. Characterisation data has meant that the datasheet for a single op amp is now normally longer than 30 pages!

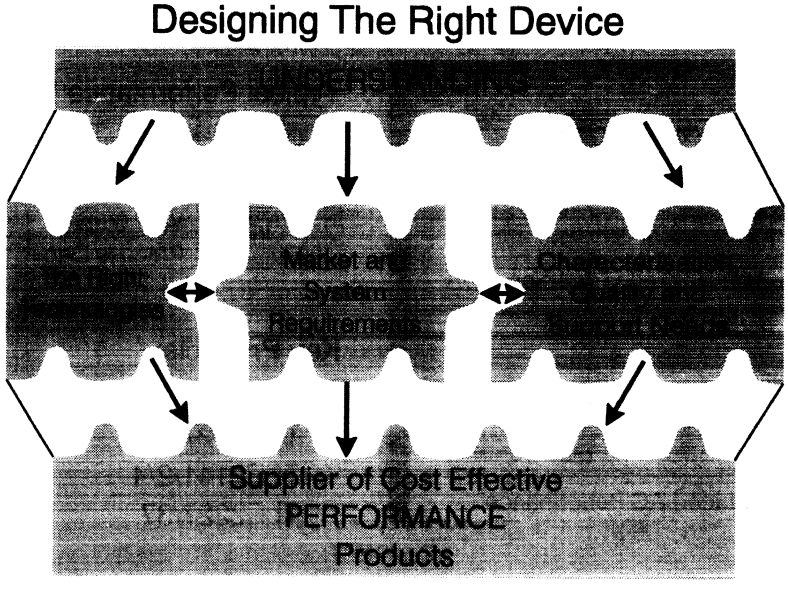


Figure 2.1.02. - Designing The Right Device

1.2.3. New Technologies

It is essential for design engineers to be able to use the most advanced and suitable technologies to enable the development of performance products. Skilled designers can only do so much - eventually the actual technology becomes the limiting factor. Throughout TI's history great emphasis has been placed on developing leading technologies to enable the production of performance products. Texas Instruments is the industry's leading supplier of products designed using Bifet and LinCMOS™ processes. Excalibur, TI's new complementary Bipolar/Bifet technology, has enabled the development of a number of precision, high speed, low power op amps - all of which are proving extremely popular in a wide range of applications. The development of advanced, quality, performance technologies is one of TI's strengths and these skills are being put to good use in all areas of linear products.

1.3. Bipolar Operational Amplifiers

Bipolar is still, by far, the most popular technology used to develop operational amplifiers and new higher performance bipolar technologies are being developed continuously - the μa741 would not recognise the technologies being used today

Devices designed using bipolar technology have a number of benefits over Bifet or CMOS products.

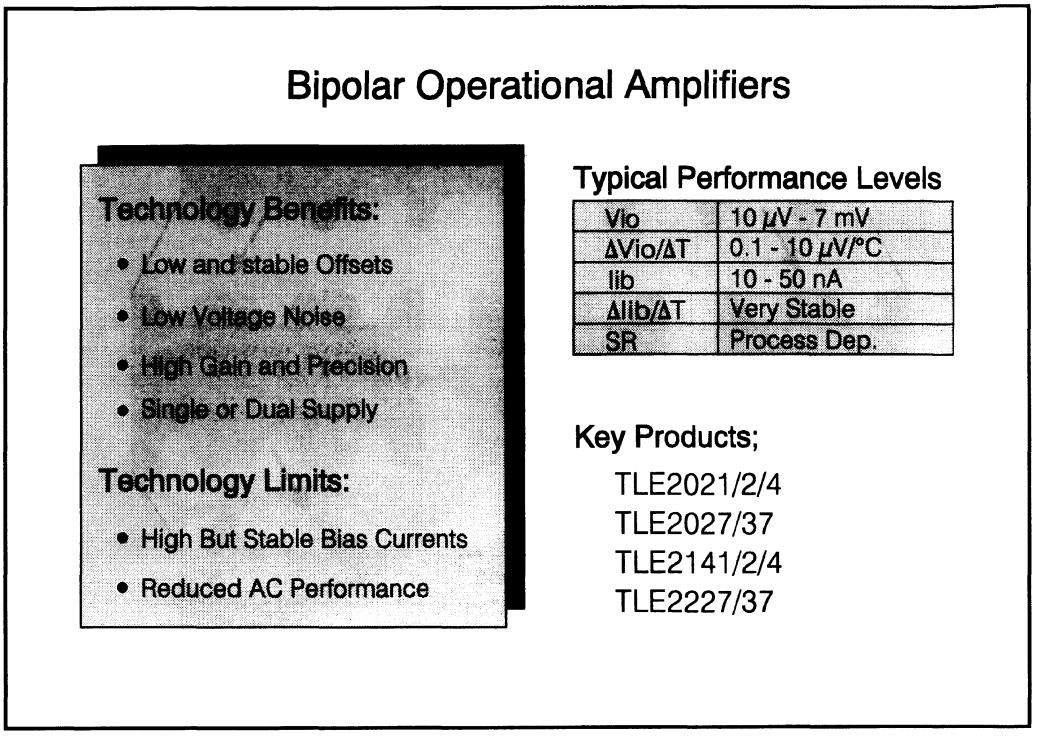


Figure 2.1.03. - Bipolar Operational Amplifiers

1.3.1. Bipolar Advantages

Low and stable offsets;

Since bipolar transistors are relatively easy to match and their behaviour due to temperature and current change is well understood, it is possible to develop operational amplifiers with low and stable offsets. Offset voltage errors are due to Vbe mismatches and differing collector currents flowing through the input stage transistors. By using various trimming techniques, bipolar designs are now available with offset voltages as low as 10µV and will drift less than 0.1µV/°C.

Low Noise;

A low noise voltage is more important than low noise current specification is of most importance in the majority of applications (e.g. audio, Telecom and many instrumentation systems). Bipolar op amps offer the lowest noise voltage performance among commercially available devices. The noise voltage from the input of a bipolar amplifier is dominated by the thermal noise from the base spread resistance and the emitter small signal resistance. These, and other factors, can be optimised to achieve op amps with $<2nV/\sqrt{Hz}$ noise voltage specification. This performance is impossible to achieve using a FET

input amplifier. When interfacing to high impedance sources however, bipolar op amps become inferior to CMOS designs, due to their high noise current specifications dominate noise errors.

High Gain;

The transconductance, gm, of the bipolar input stage is high and therefore the related open loop gain of the amplifier is also high. This enables the design of circuit that are much more 'accurate' than Bifet or CMOS designs. The high gain, however, does mean that a complicated compensation networks need to be used to ensure stability, a factor which lower gain JFETs have benefited from to achieve higher slew rates.

1.3.2. Bipolar Disadvantages

High Offset and Bias Currents;

Due to the bipolar input stage, the bias currents (effectively the the input transistor's base current), of bipolar op amps are high . Various design techniques such as SuperBeta NPNs, or bias current cancellation circuits can be used to reduce these currents, However, it would be very unusual for a bipolar device to be able to compete with a FET design at room temperature.

Bias currents for bipolar designs are, however, much more stable than for FET input designs. At high temperatures it is possible for a FET input device to actually have higher bias currents than a good bipolar design, particularly a super beta part.

Slow Lateral PNPs;

Lateral PNPs are much slower (and noisier) than the NPNs of the same process. A typical technology would have PNPs with an F_T (transistor bandwidth) of 3MHz, compared to NPNs which have an F_T of 150MHz. As it is very difficult to design a device without using PNPs, the overall ac performance of an amplifier is severely limited.

Realising this many manufacturers have developed 'Complementary Bipolar Technologies' which have much faster PNPs who's F_Ts are similar to the NPNs. The result has been much faster bipolar op amps.

Excalibur is TI's new complementary bipolar process, and as well as having faster PNPs it includes a number of other features necessary for the development of performance amplifiers.

1.3.3. TI's Bipolar Op Amps

TLE2021	LM301	LT1014	OP07
TLE2022	LM307	LT1037	OP27
TLE2024	LM308	MC1458	OP37
TLE2027	LM324	MC1558	RC4156
TLE2037	LM348	MC3303	RC4138
TLE2141	LM358	MC3403	RC4558
TLE2142	LM2902	MC34071	RC4559
TLE2144	LM2904	MC34072	TL2828
TLE2227	LT1001	MC34074	TL2829
TLE2237	LT1007	NE5532	uA741
	LT1013	NE5534	

1.4. Bifet Operational Amplifiers

Bifet operational amplifiers were first introduced in the early 1970's and today they are among the most common op amp type. They are essentially bipolar op amps which use high voltage p-channel JFETs on the input. These JFETs have a number of advantages and disadvantages;

1.4.1. BIFET Advantages

High input impedance and low bias currents;

The inherent high input impedance of JFET transistors enables op amps with extremely low bias currents. This brings a number of significant advantages to many applications including integrators, sample and holds and filter type circuits. Care must be taken however as the bias currents will double for every 10°C increase in temperature. At high temperatures a Bifet's bias current may be higher than some bipolar circuits!

Improved ac performance;

When JFETs are used in an op amp's input, the resulting gain of the op amps differential input stage is significantly reduced. The amplifier's internal compensation capacitor (which provides device stability) can therefore be reduced giving a significant increase in slew rate. For the same supply current, a Bifet op amp can easily have up to a five fold increase in slew rate over a bipolar equivalent.

Reduced Input Noise Current;

A benefit of both CMOS and Bifet operational amplifiers is their improved noise current. This is very important when interfacing to sources of a very high impedance. The input noise current is determined by the shot noise of the gate current - which is very low at 25°C.

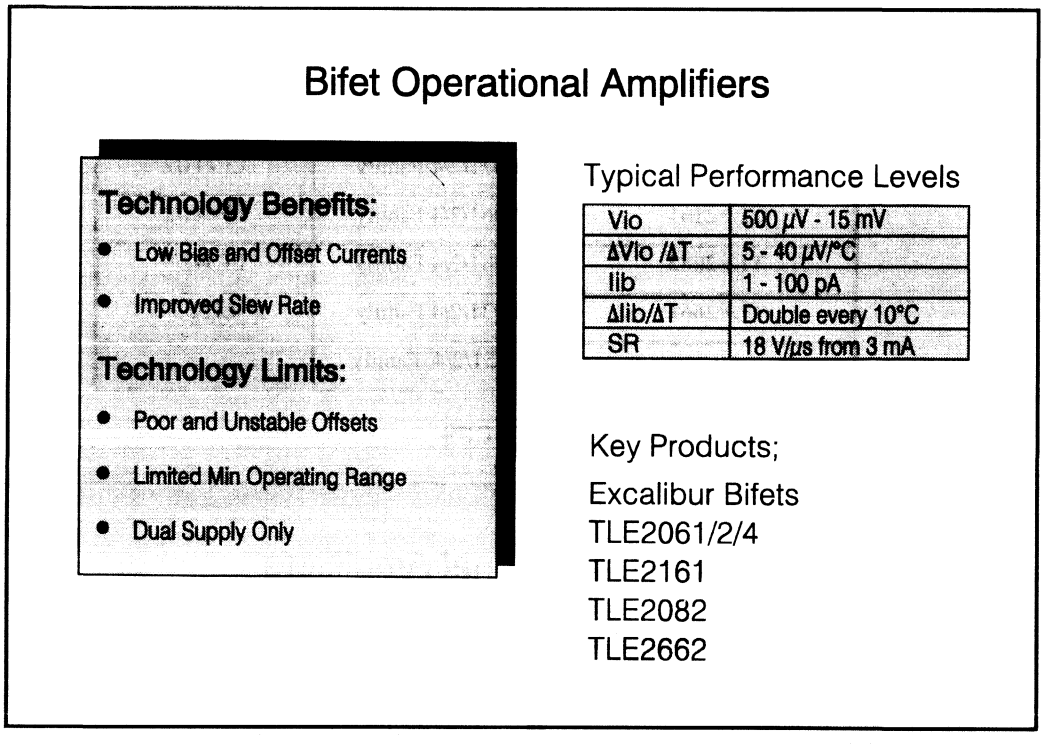


Figure 2.1.04. - Bifet Operational Ampifiers

1.4.2. BIFET Disadvantages

Poor and unstable offset voltages;

Bifet designs have typically far greater offset voltages than their bipolar equivalents. Their less uniform dc characteristics and poor thermal drift makes the essential accurate matching of the input transistors very difficult. They are also very prone to the induced stresses of plastic packages - real precision Bifets are normally only available in ceramic, metal can or hybrid packages.

Typical standard selection Bifets in a plastic package may only achieve 2mV - 3mV offset voltage and their stability will be poor. Newer designs, such as the TL051 and TL031 series have improved processing and design techniques to achieve new levels of precision and stability.

Poorer CMRR, PSRR and Open Loop Gain specifications;

The reduced gain of the Bifet's input stage, which enables the improved ac performance, also causes a reduction in various gain parameters of the device. This further reduces the suitability of the designs in precision applications.

Increased Noise Voltage;

A FET input stage will have a higher noise voltage and higher 1/f frequency when compared to bipolar devices.

1.4.3. TI's Bifets

TLE2061/2/4 Family	TL071/2/4 Family	LF411/2
TLE2161	TL061/2/4 Family	LF441/2
TLE2082	TL081/2/4 Family	LF347/9
TLE2662	TL031/2/4 Family	LF353
	TL051/2/4 Family	

1.5. CMOS Operational Amplifiers

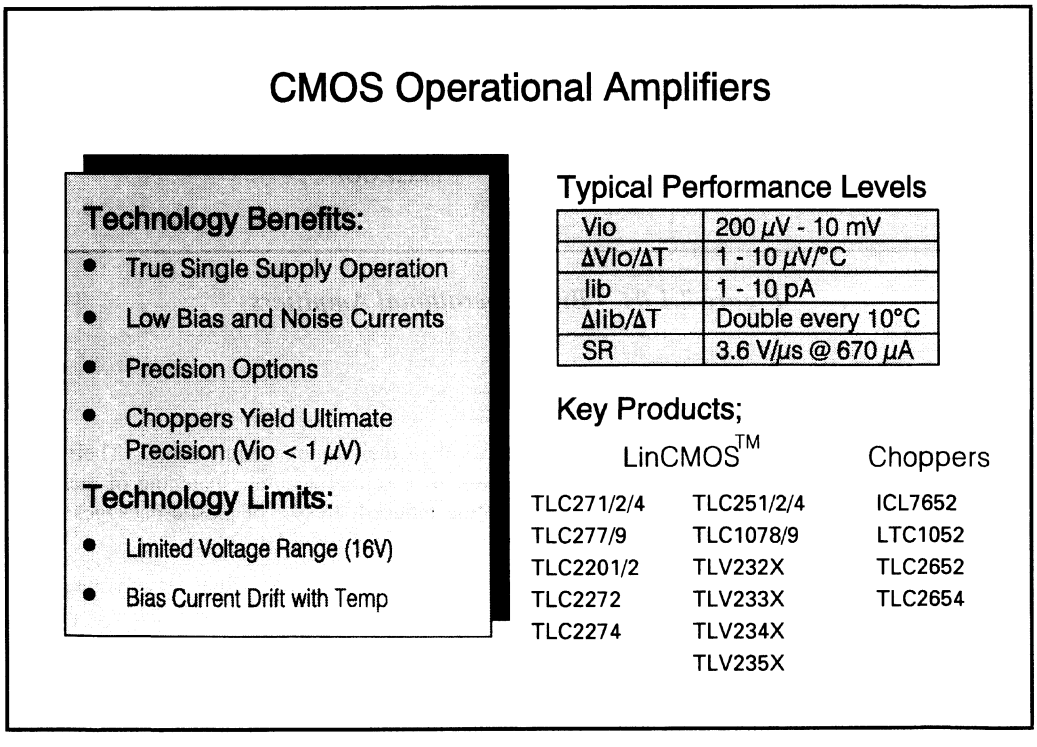


Figure 2.1.05. - CMOS Operational Amplifiers

Although originally considered to be too unstable for many linear functions, CMOS amplifiers are now well accepted as a real alternative to many bipolar, Bifet and even dielectrically isolated op amps.

Texas Instruments was the first company to release linear devices designed using a CMOS process, LinCMOS™, specifically developed for linear circuits. The first products were released in 1983, and LinCMOS™ and its next generations are still being used today to realise a whole range of linear functions - from op amps to A-D converters.

1.5.1. CMOS Advantages

Single supply operation;

By far one of the most significant advantages of using a device designed using CMOS technology is their excellent single supply operation. By using PMOS on the input stage and an NMOS on the output stage it is possible to develop a device with an input common mode range that includes the negative rail and an output stage that swings all the way down to the negative supply - true single supply operation! This feature obviously makes the devices extremely popular in battery powered applications.

Low Voltage and low Supply current applications;

TI has low quiescent supply current op amps capable of operating with supply currents of less than 10μA and at supply voltages down to 1.4V. TI has also released a new family of op amps designed specifically for 3 V applications. Single supply battery powered applications particularly benefit from using these parts.

High input impedance and low bias currents;

Like Bifet op amps, using MOS transistors on the input stage enables the design of op amps with high input impedance and low offset and bias currents. Bias currents can be in the fA range, but difficulty in testing, and various leakage currents mean that these levels of performance are rarely specified. A typical LinCMOS™ op amp has a bias current at 25°C of 100fA. Over temperature, however, the bias currents will double for every 10°C increase in temperature.

1.5.2. ESD (Electrostatic Discharge) Protection;

ESD is something that is perceived to be a problem with CMOS, but not with devices designed using LinCMOS™. All devices produced using LinCMOS™ are designed to withstand 2kV ESD - something many bipolar designs cannot claim. Protection circuits found in LinCMOS™ devices are discussed in the System Protection section.

1.5.3. CMOS Disadvantages

Limited Supply Voltage range;

Although ideal for low supply voltage applications, most CMOS parts will not operate with supply voltages greater than 16 or 18 Volts. This is a limitation in some wide supply, instrumentation applications.

Limited Offset Voltages;

The best CMOS devices can achieve offset voltages as low as 200μV which is better than most Bifet parts but does not compete with the best bipolar designs. Typical CMOS op amps will have an offset

voltage specification of 2mV - 10mV. The stability of CMOS devices is however, improved over Bifet designs.

Chopper stabilised op amps however, which are discussed in detail later, are designed using CMOS technology and achieve the ultimate in dc precision. Maximum offsets as low as 1μV are realisable.

High Noise voltage;

Like Bifets, a MOS input stage causes devices to suffer from high input noise voltages and a high 1/f corner frequency although their input noise current is normally extremely low. The TLC2201 however, discussed later in the signal conditioning section, actually features a combination of low voltage and current noise specifications.

1.5.4. TI's CMOS amplifiers

TLC2201/2	**TLV2341**	TLC271	TLC1078/9
TLC2272/4	**TLV2322/4**	TLC277/9	TLC272/4
TLC2652/4	**TLV2332/4**	TLC27L7/9	TLC27L2/4
	TLV2342/4	TLC27M7/9	TLC27M2/4

LinCMOS™ was TI's first linear CMOS technology and the resulting products are now industry standards. It has since been upgraded with **Advanced LinCMOS™** which, because of smaller geometries and more compact capacitors has enabled the true interface of digital and analogue structures. The most obvious result has been high performance ADCs. **LinBiCMOS™** is the latest revision; featuring the CMOS structures as found in Advanced LinCMOS™ as well as true bipolar transistors. This being used to great effect in TI's Data Transmission products.

1.6. Device Macro-Models and Simulations

Since the introduction of operational amplifiers, very much simplified models of their behaviour have been used to try and predict the output of the device when stressed with various forms of inputs.

The simplest model is that of the virtual short between the inputs of the device. This assumes infinite gain and infinite input impedance. The model works reasonably well on high performance op amps with high open loop gains of more than one million. It proves unsatisfactory when trying to consider other aspects in the performance of the op amp, such as the errors associated with its input and more importantly the device's frequency response.

For dc applications, high input impedance is normally a very good assumption, since almost all op amps have impedances greater than 1 MΩ and the gains frequently used are low enough such that the op amp is not used in open loop conditions. Taking into consideration all the offset voltages, input bias and offset currents adds to the complications of the simplified model. Hence, a more complete model has the virtual short across the inputs replaced with an offset voltage in series with the non-inverting input and biasing current sources connected to the inputs of the device. These are all dc effects, and can reflect the performance of the op amp reasonably well, however, modelling most of the ac aspects of the op amp can be very difficult.

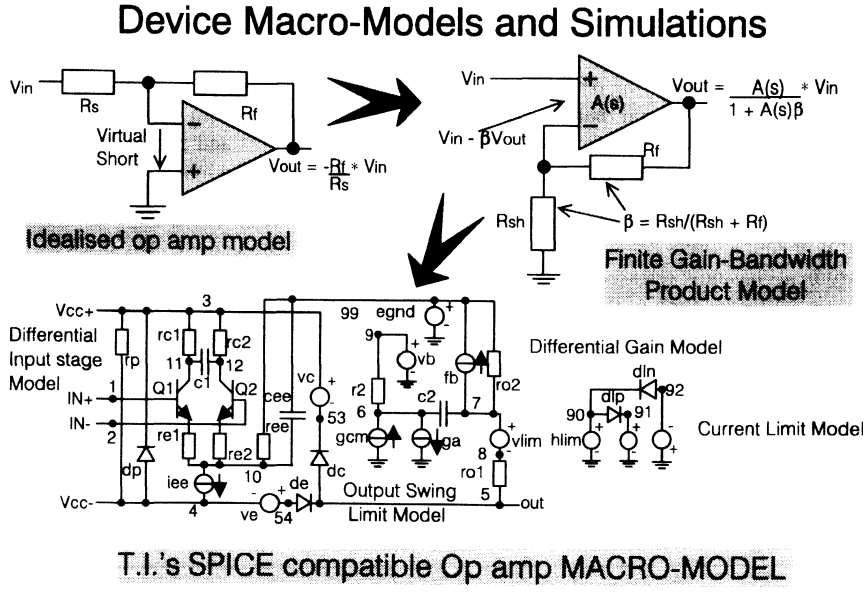


Figure 2.1.06. - Device Macro-Models And Simulations

The op amp can be considered as a low pass filter with enormous gain; the large gain minimises most of the low pass filter effects at low frequencies, but at higher frequencies these effects must be taken into account. The analysis can be made easier by use of the Bode plot, and by relating the circuit's ideal gain to the op amp's actual gain. This will show the point where the open loop gain of the op amp takes over from the ideal gain.

The whole model can be improved by considering the feedback equation of any system:-

$$G_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

Where G_{CL} is the closed loop gain, A_{OL} is the open loop gain and β is the feedback around the amplifier. Using this equation increases the accuracy of the model considerably but can also increase the complexity to beyond that of pen, paper and calculator, especially for systems using several op amps. The difficulty of ac analysis is compounded when operating the op amp with large signals, which can drive the device out of its assumed linear mode.

With the advent of personal computers, a much simpler way of analysing op amp circuits has arrived: op amp macro-models. The macro-model is a simplified model of the op amp taking into account all of its key parameters. Texas Instruments has released macro-models of all its op amps and these are

capable of operating with a wide variety of simulation packages, one example is Microsim's PSPICE™.

The macro-model is a derivative of Boyle's model, which uses real transistors to model the actual input stage of the op amp. Bias current errors and further input (ac and dc) errors can also be modelled. Current and voltage sources, along with passives are used to model the gain and its roll-off over frequency of the input and following stages. Each of the parameters are derived from the specifications of the op amp and so simulate the performance of op amp to a much higher level of accuracy than the designer, with only a pen and paper, can. The macro-models, as with most things, provide a compromise between optimum performance and simulating speed, cost and ease of use. A full model of the device will give a better representation of the device but would take much longer to simulate and would also cost considerably more.

Note op amp manufacturers seldom release full SPICE simulation models of their devices, however; Texas Instruments has now released a Macro-Model Data Manual. The manual contains model for each of its op amps, with exception of the latest products which contain the model on their datasheet.

2. DC Applications

2.1. DC Precision Design

Any signal conditioning circuit will be required to meet some given system specifications. This is true even from most simple circuits to the most complicated circuits.

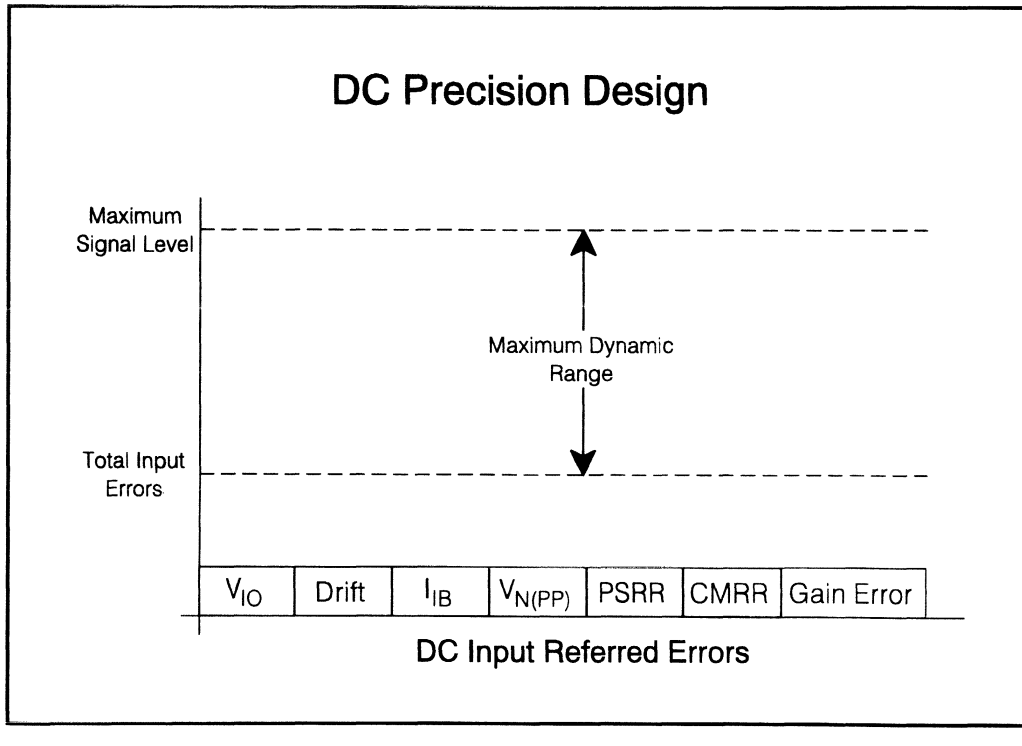
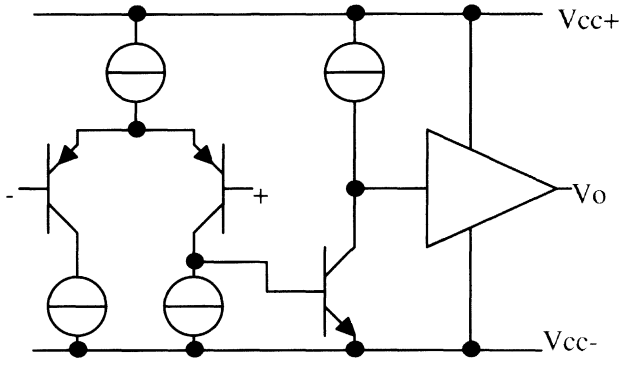


Figure 2.2.01. - D.C. Precision Design

The dynamic range is one way of stating system specifications. It can also be used as a measure of system errors. In most applications the devices having the greatest effect on the performance of the whole system will be those in the input stage, since there is not any way of recovering the errors that these devices introduce.

The most basic internal configuration for an op amp is that shown below



The transistors in the input stage are not perfectly matched and so have an offset between them. This offset voltage is affected by the supply voltage and the input voltage that is common to both of them. These effects are normally known as the Power Supply Rejection Ratio and the Common Mode Rejection Ratio, and can have large effects on the overall offset voltage of the device if too small.

The input stage transistors also have current flowing through them and so draw input bias current. This will once again affect the accuracy of the device by adding another offset voltage equivalent to the product of the bias current and the equivalent source resistance as seen by the input. For a simple inverting amplifier configuration, this source resistance will be equivalent to the parallel combination of the source resistance and the feedback resistance.

Further input offset voltage errors arise from changes in junction temperature of the device as well as during the lifetime of the device.

Further errors will be introduced by the limited open loop gain. Most approximations in the open loop gain of an op amp assume it to be infinite. When designing systems requiring an accuracy better than 0.1%, the finite open loop gain can start to be a limiting factor in the performance of the op amp.

Low frequency noise can also be a problem in very low frequency, high precision applications. In most cases only the flicker noise be need considered and in these applications it is important to use devices with a very low flicker noise content.

2.2. Bits of Accuracy

One measure of a system's accuracy is its **dynamic range** which is normally measured in decibels (dB) and is the ratio of the maximum output signal to the total output errors. This is normally used in ac applications where wide-band noise can often be a limiting factor in the performance of the whole system.

However, with the increase in digital signal processing another way of expressing the accuracy of a system is to express it in the number of BITs that can be accurately recorded.

BITs of Accuracy

D.C. Input Referred Errors

- Input Offset Errors

$$I_{IO} = I_{IB+} - I_{IB-}$$

$$V_{IE} = V_{IO} + V_{N(PP)} + V_{PSRR} + V_{CMRR}$$

- Gain Related Errors

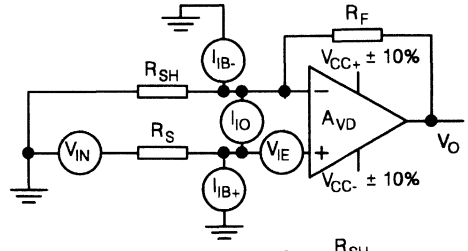
$$V_O = \frac{1}{\beta} V_{IN} - \frac{V_{IN}}{1 + A_{VD}\beta} \frac{1}{\beta}$$

- Total Input Referred Errors

$$V_{IET} = \frac{V_{IN}}{1 + A_{VD}\beta} - R_S I_{IO} + I_{IB-}\left(R_F\beta - R_S\right) + V_{IE}$$

- Total Output Errors for $V_{O(MAX)}$

$$V_{OET} = \frac{V_{O(MAX)}}{1 + A_{VD}\beta} - \frac{R_S I_{IO}}{\beta} + I_{IB-}\left(\frac{R_F}{\beta} - \frac{R_S}{\beta}\right) + \frac{V_{IE}}{\beta}$$



$$V_+ = V_{IN} - R_S I_{IB+} + V_{IE} \qquad \beta = \frac{R_{SH}}{R_F + R_{SH}}$$

$$\frac{V_O - V_-}{R_F} = I_{IB-} + \frac{V_-}{R_{SH}} \Leftrightarrow V_- = V_O\beta - I_{IB-} R_F\beta$$

$$V_{ID} = V_+ - V_-$$
$$= V_{IN} - R_S I_{IO} + I_{IB-}\left(R_F\beta - R_S\right) + V_{IE} - V_O\beta$$

- BITs of Accuracy $= -\text{Log}\left(\frac{V_{OET}}{V_{O(MAX)}}\right) / \text{Log } 2 - 1 = -\text{Log}_2\left(\frac{V_{OET}}{V_{O(MAX)}}\right) - 1$

Figure 2.2.02. - BITs of Accuracy

Figure 2.2.02 shows an op amp, including all of its input errors, in a non-inverting configuration. The voltage seen on the non-inverting input will be:-

$$V_+ = V_{IN} - R_S I_{IB+} + V_{IE}$$

V_{IE} includes the offset voltage of the device and also its power supply and common-mode rejection ratio limits, as well as the low frequency noise.

$$V_{IE} = V_{IO} + V_{N(PP)} + V_{PSRR} + V_{CMRR}$$

Summing the currents flowing into the inverting input node:-

$$\frac{V_O - V_-}{R_F} = I_{IB-} + \frac{V_-}{R_{SH}}$$

The voltage on the inverting input will be:-

$$V_- = V_O\beta - I_{IB-} R_F\beta \quad \text{.....Where } \beta = \frac{R_{SH}}{R_F + R_{SH}}$$

The differential input, V_{ID}, is now equal to V_+-V:-

$$V_{ID} = V_{IN} - R_S I_{IO} + I_{IB-}(R_F\beta - R_S) + V_{IE} - V_O\beta$$

Where $I_{OS} = I_{IB+} - I_{IB-}$

The output voltage, V_O, equals V_{ID} multiplied by the op amp's open loop gain:-

$$V_O = V_{ID} * A_{VD}$$

$$= \frac{1}{\beta}V_{IN} - \frac{V_{IN}}{(1+A_{VD}\beta)\beta} \quad \text{.....Ignoring input offset errors.}$$

Referring this and the other input offset errors, the total input referred errors, V_{IET}, are equal to

$$V_{IET} = \frac{V_{IN}}{1+A_{VD}\beta} - R_S I_{IO} + I_{IB-}(R_F\beta - R_S) + V_{IE}$$

All these errors will be multiplied by the op amp's non-inverting gain, $^1/_\beta$ to give the total output referred errors, V_{OET},:-

$$V_{OET} = \frac{V_{IN}}{(1+A_{VD}\beta)\beta} - \frac{R_S I_{IO}}{\beta} + I_{IB-}\left(R_F - \frac{R_S}{\beta}\right) + \frac{V_{IE}}{\beta}$$

The maximum dynamic range will be reached when the output signal has reached its largest level, so the total output referred errors at maximum output swing will be:-

$$V_{OET} = \frac{V_{O(MAX)}}{(1+A_{VD}\beta)} - \frac{R_S I_{IO}}{\beta} + I_{IB-}\left(R_F - \frac{R_S}{\beta}\right) + \frac{V_{IE}}{\beta}$$

The maximum dynamic range attainable by the system will therefore be equal to maximum output voltage swing divided by the total output referred errors. Converting this to decibels we get:-

$$\text{Dynamic Range} = -20\text{Log}\left(\frac{V_{OET}}{V_{O(MAX)}}\right) \text{..... dB}$$

$$= -20\text{Log}\left(\frac{1}{(1+A_{VD}\beta)} - \frac{\frac{R_S I_{IO}}{\beta} + I_{IB-}\left(R_F - \frac{R_S}{\beta}\right) + \frac{V_{IE}}{\beta}}{V_{O(MAX)}}\right) \text{.. dB}$$

$$\text{BITs of Accuracy} = -\text{Log}\left(\frac{V_{OET}}{V_{O(MAX)}}\right) \Big/ \text{Log}2 - 1 \text{..... BITs}$$

$$= \frac{\text{Dynamic Range}}{6.02} - 1 \text{ ..... BITs}$$

Dividing by the logarithm of 2 converts the equivalent base of the logarithm to 2. Subtracting 1 allows for 0.5 BIT error.

This is another way of measuring the accuracy of a system, and can be used when relating the performance of an op amp to an ADC. However, when the device is being as an ADC interface

amplifier the maximum output swing will normally be limited to the reference voltages used by the ADC.

Bearing this in mind the BITs of accuracy would become:-

$$\text{BITs of Accuracy} = -\text{Log}\left(\frac{V_{OET}}{V_{REF}}\right) \Big/ \text{Log}2 - 1 \quad \text{BITs}$$

2.3. TLE2027 and TLE2227 Precision Op Amps

The TLE2027 and TLE2227 are among the most recent op amps to be developed and fabricated using the Excalibur technology. These devices have been optimised for precision and include a novel output stage that features a 'Saturation Recovery Circuit' which enables much improved small signal response and outstanding levels of distortion.

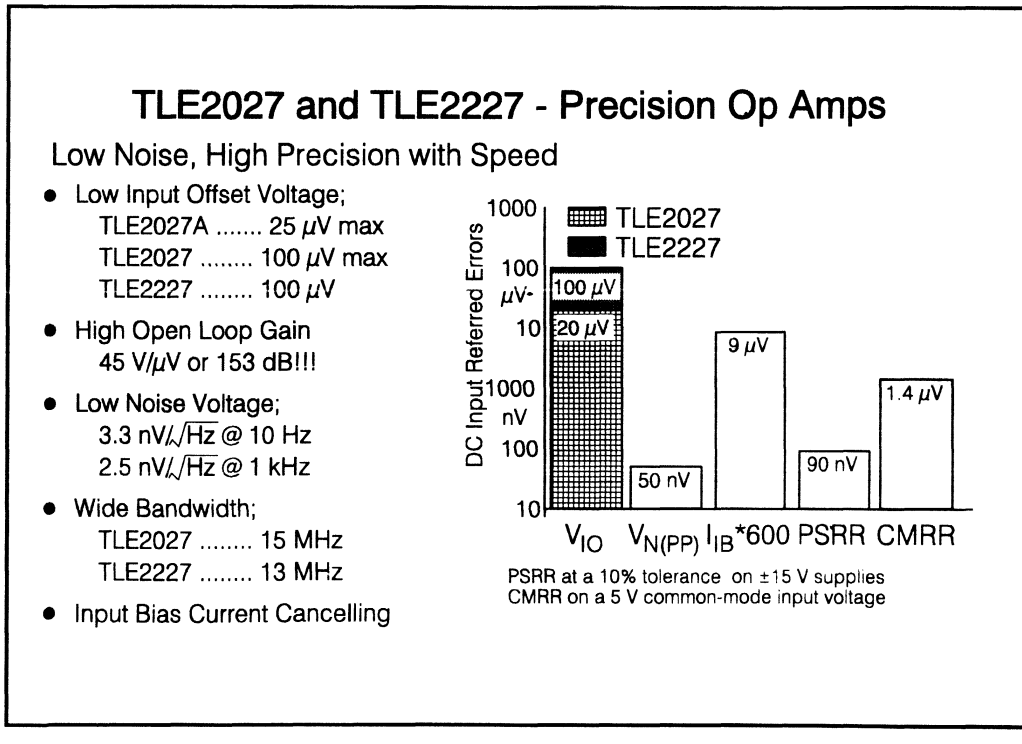


Figure 2.2.03. - TLE2027 and TLE2227 - Precision Op Amps

Precision - The parameters of most importance in a precision application are; Offset Voltage, Drift, Bias Currents and Open Loop Gain. The TLE2027A, single op amp, has a maximum offset voltage of only **25µV** and a maximum offset voltage drift of **1µV/°C and 1µV/month**. While the TLE2227, dual op amp) has an offset voltage of 100 µV, with similar offset voltage drifts to that of the TLE2027. Both

devices have bias current cancellation circuitry to reduce bias currents to typically 15 nA enabling larger external resistors without impacting overall dc accuracy.

The chart in figure 2.2.03 puts the precision of the device in perspective. Due to the devices' high open loop gains the gain error in almost all dc applications can be ignored. While the PSRR and CMRR effects are also reduced to levels far below that of similar op amps.

An outstanding parameter of both devices is their open loop gain, **Avd; - at 153dB**, it is probably the **highest in the world!** This results in an improvement in the op amp's 'loop-gain' even when used in large closed loop gain applications, yielding an increase in overall performance.

ac Performance - Both Devices have an excellent unity gain bandwidth, **15 MHz**, for the **TLE2027** and **13 MHz** for the **TLE2227**, with Slew Rates of better or equal to **2.5 V/µs**.

Low Noise - A large input stage, and clever design and layout techniques has given the device an extremely low noise voltage specification - **3.3 nV/$\sqrt{Hz}$ at 10Hz**, and **2.5 nV/$\sqrt{Hz}$ at 1kHz.** The low frequency noise and the low frequency 1/f corner give these devices a very small low frequency noise figure, only 50 nV for the 0.1 Hz to 10 Hz bandwidth. The low overall noise is an obvious benefit to precision measurement systems and audio applications.

Applications - The low offsets and excellent overall precision has enabled the parts to be used in Instrumentation, Measurement and Test equipment applications, whilst the excellent ac performance and low noise also makes the devices well suited to Audio and Telecom applications.

2.4. High Precision Differential Amplifier

As with any design, the input stage will have a significant effect on the overall performance of the system, particularly noise levels, dc accuracy and ac accuracy. One configuration which needs maximum performance is the instrumentation or difference amplifier, typically used in applications that require the ability to pick-out small differential voltages which are super-imposed on large common-mode signals. Two op amps ideal for such applications are the **TLE2027**and **TLE2227** devices.

The ideal instrumentation amplifier has infinite input impedance, large differential voltage gain and zero common-mode gain. The most simple instrumentation amplifier consists of a single amplifier configured as amplifier B in figure 2.2.04. This has major drawbacks in:-

1) The input impedance is not infinite, but is equal to the sum of R_6 and R_7 on the non-inverting input and varies with differential input voltage on the inverting input.

2) The common-mode gain depends largely on the matching of resistors R_6 and R_7 to R_8 and R_9.

These problems can be overcome by the configuration shown above. Amplifiers A1 and A2 provide high differential gain, and unity common-mode gain. Another advantage is that the input impedance of the instrumentation amplifier is now the input impedance of the amplifiers.

The choice of amplifier will now have the largest effect on the total performance of the system, and for optimum performance errors associated with each amplifier will need to be reduced. Op amps are always used in a feedback loop and due to their finite open-loop gain and finite gain-bandwidth

product, errors will be introduced. The feedback will reduce some of these problems and using a high performance op-amp will set most problems at a much lower level than others.

2.4.1. Op amp considerations.

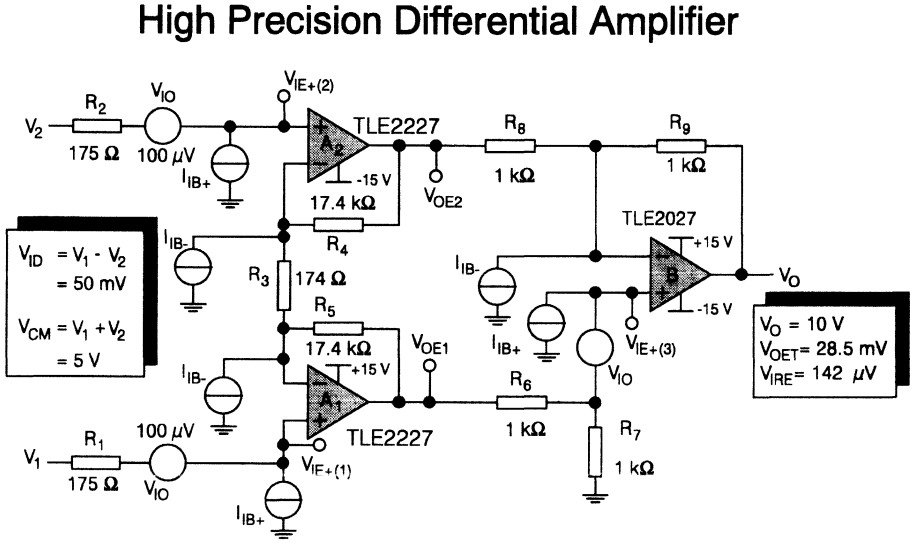


Figure 2.2.04. - High Precision Differential Amplifier

One consideration is **input impedance**, which is the input impedance of the op-amp multiplied by its desensitising factor 1+Aβ; An op-amp with a large open loop gain will increase the input impedance to the order of $10^{12}\Omega$. This means that the **bias currents** are a much more important problem, especially when considering performance over temperature. The TLE2027 implements bias current cancellation techniques, resulting in the op-amp having low bias currents coupled with high speed and large open-loop gain.

Common-mode and **power supply** effects are another source of error and should not be neglected. The op amps will normally be looking at very small differential signals superimposed on large common-mode signals, which means that to preserve performance and accuracy the op amp needs to have a large common-mode rejection ratio. The TLE2027 has a typical CMRR of 131 dB, which is equal to 282 nV/V, and a PSRR of 144 dB equivalent to 63 nV/V.

The **gain error** due to the op-amp can introduce further system performance limitations, especially when operating at the high gains demanded by instrumentation amplifiers. The TLE2027 and TLE2227 has an open loop gain of 45 million! - hence with a gain of 1000 the gain error is still only 0.0022%.

Drift of the op amp's offset voltage can limit the overall accuracy of the system, in particular with time and temperature, as this is one parameter which cannot be corrected or nulled out. The effects of both these are normally technology dependent, and as already discussed the Excalibur process provides stability in both domains. The TLE2027 and TLE2227 have a typical temperature co-efficient of input offset voltage, αV_{IO}, of 400 nV/°C. When considering the drift with temperature there are two aspects to take into account, the most obvious being the change in ambient temperature. The other is due to changes in junction temperature caused by self heating of the integrated circuit. The ultimate drift in offset voltage due to self heating will be package dependent due to differing thermal resistances.

2.4.2. Application errors

The configuration shown uses op amps A1 and A2 to provide a large differential gain (201) whilst providing a unity common mode gain. The errors associated with these op amps will be very similar.

The worst case values of CMRR and PSRR of the TLE2227 reduces errors associated with a common-mode voltage of 5 V and a 15 V supply (10% tolerance) to16.5 µV. The quiescent supply current dissipates a power of 219 mW, this coupled with power dissipated in the output stages to drive the feedback and load resistors increases the junction temperature by 36°C. This increases the offset voltages of A1 and A2 by 14.4 µV. The cancellation circuitry for the bias currents reduces their related errors to 2.6 µV; while the open loop gain of the TLE2027 reduces any gain error to 112 nV (for a 50 mV differential input voltage).

Taking these into account the errors referred to the non-inverting input, V_{IE+}, is equal to:-

$$V_{IE+} = V_{IO1} + I_{IB+}*R_1 + \Delta T\alpha V_{IO} + V_{IN1}* CMRR + 2V_{CC}*10\%*PSRR.$$

For the TLE2227 the input referred errors should be:- $V_{IE+} = 123\ \mu V$

The feedback network around each op amp ensures that the inverting input will be equal to the non-inverting input (the actual system input) plus or minus the errors, V_{IE+}, discussed above. This results in V_{IE+} also appearing as an input for the opposing op amp in the differential input pair. Therefore op amp A1 will multiply its offset errors by its normal non-inverting gain and it will also multiply the offset errors of A2 by its inverting gain, (the converse is true for A2). Op amp A3 with its differential gain will effectively result in the offset errors of A2 being multiplied by -201, and the offset errors of A1 multiplied by 201. The bias currents from the inverting input cause an offset voltage on the output of each amplifier equal to the bias current multiplied by the feedback resistor (R_5 or R_4), this can be referred to the input of the op amp by dividing by the non-inverting gain.

This results in the output of amplifier A1, V_{OE1}, being equal to:-

$$V_{OE1} = V_{IE+1}*\left(1+\frac{R_5}{R_3}\right) - I_{IB-}*R_5 - V_{IE+2}*\left(\frac{R_5}{R_3}\right)$$

while the output of amplifier A2, V_{OE2}, will be:-

$$V_{OE2} = V_{IE+2}*\left(1+\frac{R_4}{R_3}\right) - I_{IB-}*R_4 - V_{IE+2}*\left(\frac{R_4}{R_3}\right)$$

These equations ignore the very small gain error of the TLE2027. The inverting input bias current error, $I_{IB-}*R_5$, equals 261 μV.

2.4.3. Differencing Amplifier

Op amp B should remove the common-mode signal still present on the outputs of A1 and A2. It will also introduce similar errors to A1 and A2 except that the bias current error will be greater due to the larger source resistors. Assuming true matching between resistors R_6, R_7, R_8 and R_9, the bias current error will be reduced to the offset current error. When using op amps with bias current cancellation techniques the benefits of matching source resistances are reduced and will actually reduce the performance for low noise applications. The input stage has special circuitry, using matched transistors, to provide the bias currents for the differential input transistors.

The self heating of op amp B will introduce errors due to changes in the by junction temperature. The output of B will be approximately 10 V while its inputs should be about 5V, resulting in its output sourcing 5 mA which dissipates a further 25 mW within its output. This extra power dissipation coupled with quiescent power will cause a drift of 6.95 μV. Taking this drift and the offset current error of 3 μV, (6 nA x 500 Ω, into account the error introduced by A3 will be 31.6 μV; the non-inverting gain of A3 doubles this to yield 63.2 μV, which in this configuration is negligible.

2.4.4. Total Errors

The non-inverting errors due to A1 and A2 are multiplied by 201. This results in an error due to A1 of

201 x 123 μV - 261 μV = 24.46 mV.

and an error due to A2 of:-

201 x 123 μV - 261 μV = 24.46 mV.

However, because op amps A1 and A2 are on the same die their input stage will be at similar temperatures resulting in most of the offset drift due to temperature cancelling out. Although all the other errors are common to the same integrated circuit the biasing circuitry within the device will be separate, and are therefore uncorrelated. These errors will be less than on an op amp with similar accuracies.

A way of minimising the probable overall error is to take a RMS sum of the remaining errors. If this is done the error achieved is 30.2 mV. Relating this error to the input of the instrumentation amplifier results in an offset error of only 150 μV.

The large common-mode signal has increased the errors due to the op amps' finite common mode rejection ratio, and such a large common-mode signal applied to the third amplifier could add further errors caused by mismatching between resistors R_6 to R_9. Replacing R_7 with a trimming variable resistor allows for any further error adjustment.

2.5. Improved Linearity Strain Gauge Amplifier

One problem with most strain gauges is their relatively low resistance. This low resistance will cause a compromise between the voltage used to drive the strain gauge itself and the voltage that can be measured between its output.

To increase the voltage that is read out of the strain gauge, the voltage used to drive the stain gauge can be increased. This will increase the self heating within the strain gauge, and so affect the accuracy of the system. To minimise this problem the TLE2227 is used to place a 5 V drive across the strain gauge. To reduce the power dissipation within the TLE2227 its power supply rails have been reduced to ±7.5 V.

The use of the TLE2227 in this application allows any temperature drift within each amplifier to cancel out with the other.

2.5.1. Circuit Operation

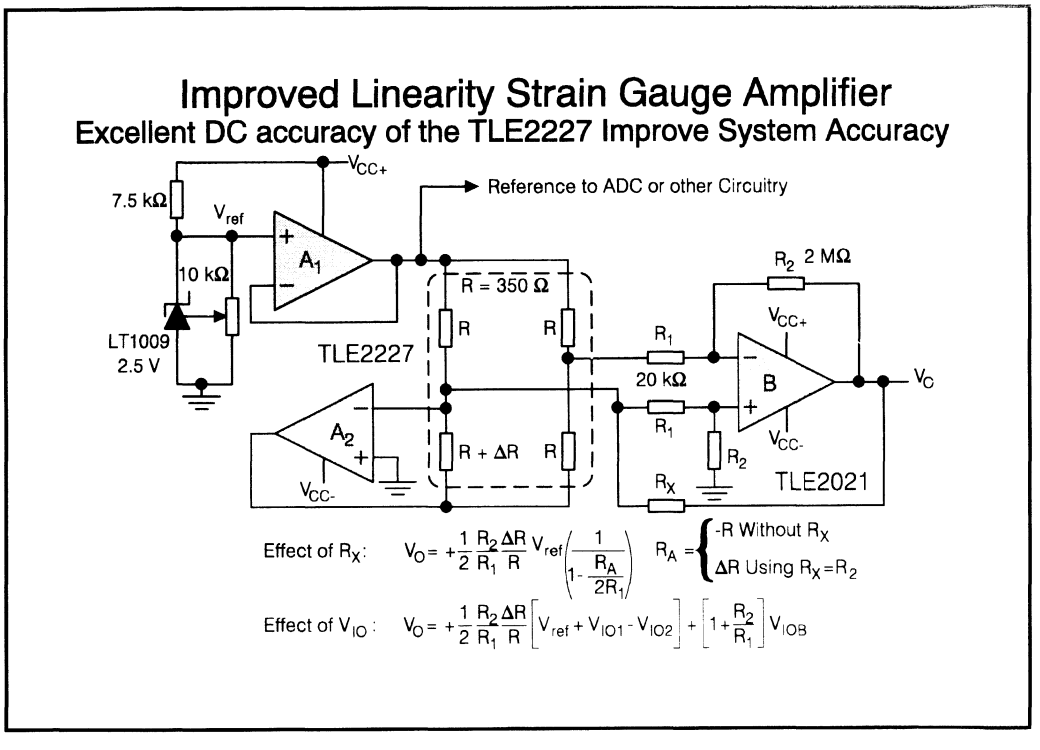


Figure 2.2.05. - Improved Linearity Strain Gauge Amplifier

Op amp A_1, is used to buffer the output of a trimmed LT1009, providing a +2.5 V bias onto the strain gauge. Op amp A_2 is configured as an inverting amplifier, and uses the strain gauge's resistors as its source and feedback resistors. The voltage appearing on the output of A_2, V_{O2},will therefore be equal to:-

$$V_{O2} = -V_{O1} * \frac{R + \Delta R}{R}$$

Op amp B is configured as a single instrumentation amplifier, and is used amplify the difference between the outputs of the strain gauge. The output of the strain gauge going to the non-inverting input of the instrumentation amplifier will be essentially 0 V, the inverting input to the instrumentation amplifier will measure the average of the outputs from A_1 and A_2. So the inverting input to the instrumentation amplifier, V_{IN-}, is equal to:-

$$V_{IN-} = V_{O1} * \frac{1}{2} - V_{O1} * \frac{R + \Delta R}{R} \frac{1}{2}$$

$$= -V_{O1} * \frac{1}{2} \frac{\Delta R}{R} \quad \text{..... Where } V_{O1} = V_{ref}$$

The output of op amp B, V_O, would therefore ideally be:-

$$V_O = \frac{1}{2} \frac{R_2}{R_1} \frac{\Delta R}{R} V_{REF}$$

But the source resistance is not just R1, but the resistance of the strain gauge must also be taken into account. So the actual gain of the instrumentation amplifier is

$$V_O = \frac{1}{2} \frac{R_2}{R_1 + R/2} \frac{\Delta R}{R} V_{REF}$$

$$= \frac{1}{2} \frac{R_2}{R_1} \frac{\Delta R}{R} V_{REF} * \frac{1}{1 + \frac{R}{2R_1}}$$

A compromise between the ratio of R_1 to the resistance of the strain gauge, R, can clearly be seen. In order to keep the offset current errors low the source resistance, R_1, of the instrumentation amplifier must be kept low as must the offset current of op amp B.

2.5.2. Bootstrapping

Another way to minimise the error due to op amp B's finite input impedance is the use of bootstrapping. The extra resistor, R_X, provides positive feedback around op amp B, and increases the effective input resistance of the instrumentation amplifier, and helps to eliminate any loading effects of the strain gauge. R_X will have maximum effect when it is set equal to R_2. Providing the variation in the bridge resistance, ΔR, is small compared with R then R_X can reduce the loading errors of the strain gauge to insignificant levels.

Considering R_X to be another source resistor with V_O as its input the equation for is modified to yield:-

$$V_O = \frac{1}{2} \frac{R_2}{R_1} \frac{\Delta R}{R} V_{REF} * \frac{1}{1 - \frac{\Delta R}{2R_1}}$$

2.5.3. Op Amp Input Errors

The offset of op amp A_1 will appear on its output and will be amplified by A_2. So the output of A_1 will be:-

$$V_{O1} = V_{ref} + V_{IO1}$$

The output of A2 will be:-

$$V_{O2} = -\frac{R+\Delta R}{R}*(V_{ref}+V_{IO1})+\left(1+\frac{R+\Delta R}{R}\right)V_{IO2}$$

The offset voltage of op amp A2 will appear on its inverting input, so the differential input to op amp B will be:-

$$V_{ID} = V_{IO2}+\frac{1}{2}\left(1+\frac{\Delta R}{R}\right)*(V_{ref}+V_{IO1})+\left(2+\frac{\Delta R}{R}\right)V_{IO2}-\frac{V_{ref}+V_{IO1}}{2}$$

$$= \frac{1}{2}\frac{\Delta R}{R}[V_{ref}+V_{IO1}-V_{IO2}]$$

This differential input will be multiplied by the inverting gain of op amp B. The errors of op amp be must also be added to the errors due to op amps A1 and A2. The errors due to op amp B are:-

$$V_{IEB} = V_{IOB}+I_{IO}\frac{R_1R_2}{R_1+R_2}$$

This will be multiplied by the non-inverting gain of op amp B to yield the output of op amp B including offset errors:-

$$V_O = \frac{1}{2}\frac{R_2}{R_1}\frac{\Delta R}{R}[V_{ref}+V_{IO1}-V_{IO2}]+\left[1+\frac{R_2}{R_1}\right]\left[V_{IOB}+I_{IO}\frac{R_1R_2}{R_1+R_2}\right]$$

Choosing an op amp with low offset current errors reduces the total errors of the system to:-

$$V_{OET} = \frac{1}{2}\frac{R_2}{R_1}\frac{\Delta R}{R}[V_{IO1}-V_{IO2}]+\left[1+\frac{R_2}{R_1}\right]V_{IOB}$$

Using the TLE2021 as the instrumentation amplifier combines low supply voltage operation, low offset voltage and its low input offset currents. The low offset current would normally yield an error of 60 μV. The offset current error could be further minimised by replacing the TLE2021 with the TLC2201, which offers lower bias and offset currents along with a rail to rail output swing.

2.6. TLE2021/2/4 Low Power Precision op Amps

The TLE2021, TLE2022 and TLE2024 were the first operational amplifiers to be processed using the Excalibur technology. These low power products were designed using the new high speed vertical PNPs available in Excalibur, and the result is a family of devices that offer significant ac performance with minimal supply currents.

2.6.1. Improved ac Performance

The graph above compares the Bandwidth and Supply current for a number of low power operational amplifiers. It immediately shows that all TLE2021/2/4 devices achieve much improved bandwidth without any increase in supply current. Performance in fact exceeds that of some Bifet and CMOS op amps.

Slew rate is also significantly improved when compared to low power industry standard alternatives - typically 0.9 V/μs from 235 μA. The device is now a viable alternative to Bifet and CMOS designs which are often used for their improved ac performance.

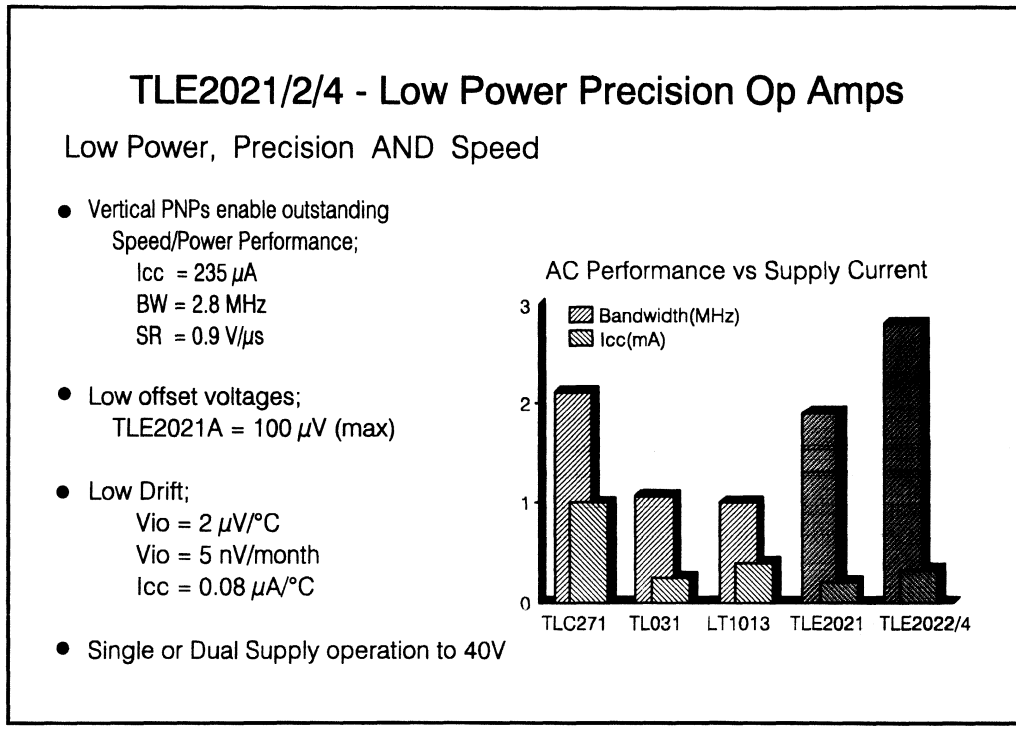


Figure 2.2.06. - TLE2021/2/4 - Low Power Precision Op Amps

2.6.2. Precision

What further makes this device stand out is its suitability for precision applications. The tightest selection has a maximum offset of just 200 μV in a plastic package. This combined with a high Open Loop Gain (A_{vd} equals 120dB), and superior stability with time and temperature results in an amplifier ideal for low power instrumentation, test and measurement equipment. The op amps offsets will typically vary by 2 μV/°C and 5 nV/month - this equates to a V_{io} change of 1 μV in 16 years!

The 'A' selection part has 200 μV maximum offset voltage while the standard part has a Vio of 500 μV.

2.6.3. Performance stability

In addition to low offset voltage drift, a patented bias circuit was designed using Excalibur's JFETs. The result is that the supply current varies typically by 0.08 μV/°C. In fact **all** temperature versions specify the same supply current spec. at both 25°C and over the full range.

Supply current stability has a number of system benefits above its obvious advantage to low power circuits. Supply current impacts the performance of most op amp parameters, including gains, slew rate, bandwidth, offset voltage, bias currents and even the output drive capability. By maintaining a relatively constant supply current, the drift with temperature of these other specifications is also reduced. Well defined and constant system performance with temperature is very achievable.

2.6.4. Single or Dual Supply Operation

Using Excalibur's new PNPs, the devices have a common mode input range down to the negative supply (0V to 3.2V from 0V and 5V supplies) and so are the ideal choice for low level, single supply single conditioning applications. The absolute maximum voltage range is +/-20V, so applications with large supply voltages for increased dynamic range can also benefit.

2.6.5. Phase-Reversal Protection

All devices feature phase-reversal protection circuitry that eliminates unexpected change in output states when one of the inputs goes below the negative rail.

2.6.6. Applications

Low power systems will benefit the most from using the TLE2021 family of op amps. Several hand-held Telecom equipment gain a significant advantage from the combination of low power consumption and good ac performance, while portable test and measurement applications can take full advantage of the precision and stability of these designs. The parts have been used in magnetic sensors, process monitoring and control equipment, and also single supply instrumentation systems such as interfacing to a strain gauge.

2.7. Precision 2-Wire 4-20 mA Current Loop

2.7.1. What is a Current Loop?

Often information from an analogue sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The most commonly used current loop interface standard consists of a minimum of two wires providing both the power supply for the sensor and signal conditioning circuit as well as transferring the information sensed in form of a current, which varies proportionally with the measured signal. The current in the loop varies usually from 4mA, corresponding to no signal, to 20mA for full scale - referring to the well known 4 to 20mA current loop. Up to 4mA of the loop current can be used for supplying the sensor, signal conditioning and voltage-to-current converter.

2.7.2. Precision 4 to 20mA Current Loop

The circuit presented provides a 4 to 20 mA output current for a 0 to 100 mV input voltage. By modifying R_1, R_2 and R_3 the input range or the output current can be adjusted. The total error is kept very low provided that the recommended precision components are used.

The employed Excalibur op amp, the TLE2021A, is a high performance op amp well suited for this type of application. The TLE2021A is here configured as a voltage-to-current converter, transmitting a very stable loop current, I_{loop}, proportional with the input voltage, V_{in}. The converter's

transconductance or "gain" can be adjusted by R_1 and its current-offset varies with R_2. Resistor R_4 reduces the influence of the op amp's input bias current to that of its input offset current.

The loop current is divided up in three major paths: The primary current path is through transistor Q_1, whilst the secondary paths are via the reference and through the op amp. All current flowing through R_S is within the controlled and regulated 4 to 20 mA current loop. The current flowing through R_3 is outside the loop control and contributes to the circuit's total error. This current can be taken into consideration in the design equations but with the chosen component values, its error becomes insignificant.

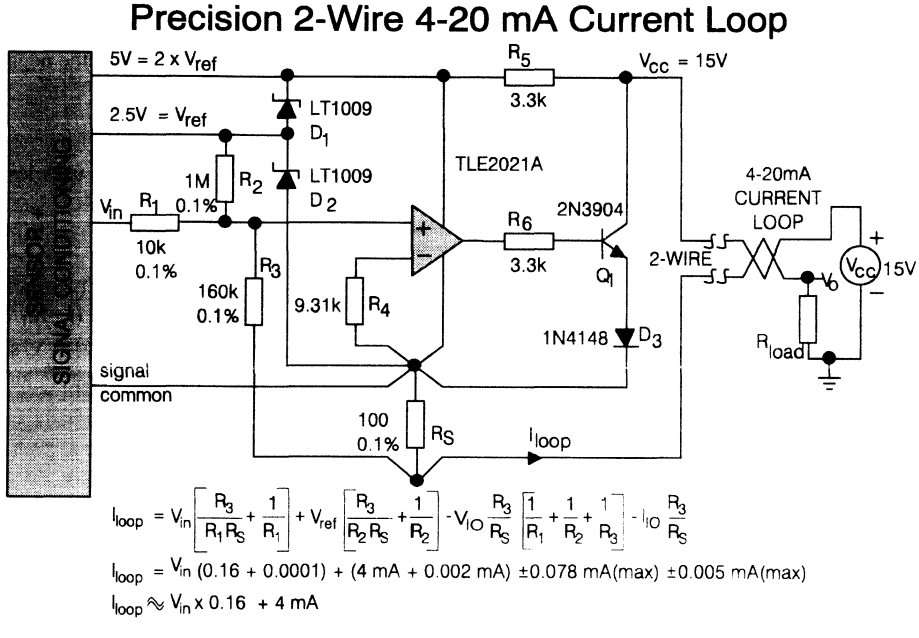


Figure 2.2.07. - Precision 2 - Wire 4-20 mA Current Loop

High system accuracy and stability is achieved without trimming by using two LT1009 voltage references in series producing a precision +5 V reference. This implementation not only provides a stable 0.2% precision reference for the voltage-to-current converter but also ensures that picked up noise and hum from long loop wires are suppressed from the op amp supply by the reference element's low dynamic impedance. In addition, the reference and its +2.5V centre point are available for external signal conditioning circuitry, provided that a limited current is taken. The converter itself needs a minimum of 630 µA (400 µA for the reference and 230 µA for the op amp), leaving (4 - 0.63) mA = 3.37 mA to be used by additional circuitry. If really low power is required, the LT1009 voltage

references should be replaced by LT1004s reducing the quiescent current consumption to basically that of the TLE2021A op amp or 240µA.

2.7.3. Why use the Excalibur TLE2021 Op Amp?

Common Mode Input Voltage to Negative Supply Rail

By analysing the application it is seen that the input common mode voltage is zero volt.

5 V Single Supply Capability

This op amp feature eliminates the need for a third negative supply wire or a charge-pump creating a negative rail from the positive. Also, the low minimum operational voltage is utilised.

Output Swing Close to the Negative Rail

By analysing the circuitry it is seen that an output swing down to two V_{be} from the negative rail is required. Few dual supply op amps can actually swing that low.

Low Power Consumption

A total of 4 mA is available for the converter and sensor interface. TLE2021 uses less than 230 µA leaving more current for other parts of the circuit.

Low and Stable Input Offset Voltage

From the output current expression on the figure, it is clear that low input offset voltage is required. A 1mV offset voltage would contribute with a current error of 0.17mA. The TLE2021A with its maximum input offset voltage of 200 µV (300 µV max. @ 5 V supply) gives low error. Additionally, its offset voltage also remains stable with temperature and time featuring 2 µV/°C and 5 nV/month typical drift.

2.7.4. Design Details

Assuming that the voltage at the non-inverting input terminal of the TLE2021A is of zero volt relative to "Signal Common", and that $I_{R_S} = I_{loop}$, the sum of the currents at the non-inverting terminal gives:

$$\frac{V_{in}}{R_1} + \frac{V_{ref}}{R_2} - \frac{I_{loop} R_S}{R_3} = 0 ;$$

Solving this with respect to I_{loop} gives:

$$\boxed{I_{loop} = V_{in} \frac{R_3}{R_1 R_S} + V_{ref} \frac{R_3}{R_2 R_S}} \quad (1)$$

The design equations specifying the resistor values can be derived from (1). Assuming

V_{ref} = 2.5V and V_{in} ranges from 0- to 100mV, it follows:

(a) $I_{loop(min)} = V_{ref} \frac{R_3}{R_2 R_S} \quad \Rightarrow \quad 4mA = 2.5 \frac{R_3}{R_2 R_S} ;$

(b) $I_{loop(max)} = V_{in(max)} \frac{R_3}{R_1 R_S} + 4mA \quad \Rightarrow \quad 20mA = 0.1 \frac{R_3}{R_1 R_S} + 4mA ;$

Equation (a) and (b) have in total four unknown resistor values. By choosing two of them the equations decide on the other two. The basic guidelines applied for the choice of the resistor set satisfying (a) and (b) are:

R_S should be small to minimise its voltage drop. Two problems are associated with a high voltage drop across R_S. Firstly, it causes variation in the reference diodes current with the loop current and hence affects their stability. Secondly, a high voltage drop increases the current flowing outside the control loop through R_3. However, very small resistor values are not available with high accuracy - say 0.1%, but a good compromise is 100 Ω.

R_1's value is a compromise between minimising errors resulting from the op amp's input offset currents, I_{io}, to a level below that of the op amp's offset voltage, and simultaneously not loading the source. With I_{io}(max.) = 3 nA, a 10 kΩ resistor gives only 30 μV offset error compared with the op amp's 300μV (max.) offset voltage at 5 V supply. $R_4 = R_1 \| R_2 \| R_3$ ensures that only input offset current rather than input bias current contributes to the error.

R_2 should maximum be 1 MΩ to allow a 0.1% high precision resistor to be used.

R_3 should be as high as possible to limit the current flowing outside the control loop but satisfy the same criteria as for R_2.

A set of values satisfying the above criteria and equation (a) and (b) is:

R_S = 100 Ω; R_1 = 10 kΩ; R_2 = 1M Ω; R_3 = 160 kΩ R_4 = 9.32 kΩ;

R_5 delivers the current required for the LT1009 shunt references, the op amp plus additional current for the sensor and its interface circuit. This current is stable with constant V_{in} but as the voltage drop across R_S varies with I_{loop}, the drop across R_5 varies as well. This in turn causes the current through the LT1009 references to shift accordingly. To avoid changes in the reference voltage this current must be kept fairly stable; hence the drop change across R_5 must be minimised placing constraints on a minimum power supply voltage and the value of R_{load}. Choosing R_5 = 3.3 kΩ causes the current in the LT1009 references to vary by only 700 μA, provided that R_{load} = 50 Ω. This choice also allows for up to 1.5 mA reference current to be used for the sensor and its interface.

2.7.5. Error budget

The op amp's offset error, V_{io}, modifies the loop current, I_{loop}, of equation (1) as the voltage at the non-inverting input is $\pm V_{io}$ rather than zero volt with respect to Signal Common assumed for (1). If the op amp's input offset current, I_{io}, is taken into consideration, it should be summed with the other currents at the non-inverting terminal of the op amp. This yields:

$$\frac{V_{in} - V_{io}}{R_1} + \frac{V_{ref} - V_{io}}{R_2} - \frac{I_{loop} R_S + V_{io}}{R_3} - I_{io} = 0 \; ; \qquad \Rightarrow$$

$$I_{loop} = V_{in} \frac{R_3}{R_1 R_S} + V_{ref} \frac{R_3}{R_2 R_S} - V_{io} \frac{R_3}{R_S} \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) - I_{io} \frac{R_3}{R_S} \; ; \qquad (2)$$

An additional error source adding to I_{loop} of (2) is the current bypassing the control loop through R_3. All current passing through R_S is inside the control loop. In equation (1) we assumed that $I_{loop} = I_{R_S}$ but a more correct expression is:

$$I_{loop} = I_{R_S} + I_{R3} \quad \text{or} \quad I_{loop(3)} = I_{loop(1)} + I_{R3} \; ;$$

where $I_{loop(1)}$ is I_{loop} given by (1). By ignoring the insignificant effect from the op amp's offset error on the bypass current error: $V_{R3} = V_{Rs} = I_{loop(1)} R_S$ resulting in:

$$I_{loop(3)} = I_{loop(1)} + I_{loop(1)} \frac{R_S}{R_3} \quad <=> \quad I_{loop(3)} = I_{loop(1)} \left(1 + \frac{R_S}{R_3}\right);$$

Substituting $I_{loop(1)}$ with I_{loop} of (1) yields:

$$I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S} + \frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S} + \frac{1}{R_2}\right);$$

By adding the errors contributed by V_{io} and I_{io} in equation (2), ignoring the insignificant effect from the bypassed loop current on these errors, we have:

$$I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S} + \frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S} + \frac{1}{R_2}\right) - V_{io}\,\frac{R_3}{R_S}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) - I_{io}\,\frac{R_3}{R_S}$$

The difference between the worst case $I_{loop(3)}$ at 25°C and the ideal $I_{loop} = V_{in}\,0.16 + 4mA$ is specified in the following error table:

Errors in 4- to 20mA Current Loop Circuit		Worst Case Error		
Error Relative or Absolute	Tolerance Source	Low Level	Full Scale	Unit
R_1, R_2, R_3, R_S	0.1%	12.0	60.1	µA
V_{ref}	0.2%	8.0	8.0	µA
V_{io}	200uV	34.3	34.3	µA
I_{io}	3nA	4.8	4.8	µA
I_{R3}	$(R_S/R_3)\, I_{loop}$	2.5	12.5	µA
Total Worst Case Error in I_{loop}		±61.6	±119.7	µA
Total Worst Case Error in % of Ideal I_{loop}		±1.5	±0.6	%

Note: Low Level = 4 mA, Full Scale = 20 mA.

The worst case untrimmed error of ±0.6% for full scale at 25°C is mainly dominated by resistor tolerances and the op amps input offset voltage. The chance of the individual errors being worst case and contributing in the same direction or adding up with the same sign is unlikely - so typically, the performance will be much better. However, by trimming R_2 for low levels (4 mA) and R_1 for full scale (20 mA) all of the above errors can be eliminated, reducing inaccuracy to drift with time and temperature of the same parameters. Such a trimmed circuit can achieve a similar accuracy as the untrimmed one at 25°C but over a 0°C to 70°C temperature range.

2.8. Low Power Temperature Sensor Amplifier

Most temperature sensors are not linear, and therefore require some form of linearisation. This linearisation can be done via the biasing of the sensor, or via some post signal conditioning linearising.

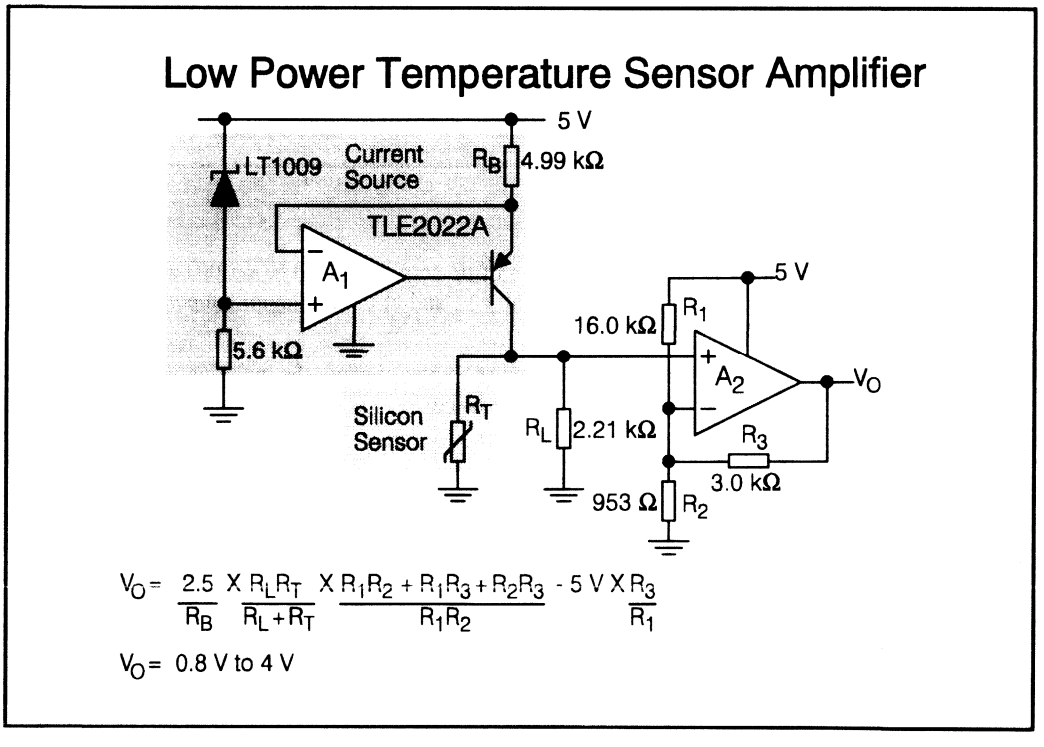


Figure 2.2.08. - Low Power Temperature Sensor Amplifier

The sensor used is made out of silicon and has a non-linear resistance versus temperature characteristic. One way of linearising its characteristic is to bias it with a constant current while placing a linearisation resistor in parallel with it. The value of linearisation resistor is determined by the temperature range over which the device will measure.

The value of the linearisation resistor, R_L, can be determined from the following equation:-

$$R_L = \frac{R_M*(R_4+R_5)-2*R_4*R_5}{R_4+R_5-2*R_M}$$

Where
R_4 = Sensor resistance at minimum temperature point
R_5 = Sensor resistance at maximum temperature point
R_M = Sensor resistance value at the midpoint of temperature range

For an operating temperature range of 0°C to 50°C, the values for R_1, R_2, and R_M are:-

$$R_4 = 813.5\ \Omega$$
$$R_5 = 1211\ \Omega$$
$$R_M = 1000\ \Omega$$
$$R_L = 2210\ \Omega$$

Op amp A_1 is used with the LT1009 and a PNP transistor to set up a current source. The current sourced will nominally be equal to:-

$$I_S = \frac{V_{REF}}{R_B} = \frac{2.5}{4.99} \text{ ..... mA}$$
$$= 501\ \mu A$$

To maximise the output swing at the output the gain of op amp A_2 should be set that at the maximum temperature measured the output of A_2 should be at 4 V, and at the minimum temperature measured the output of A_2 should be close to 0.8 V.

In order to achieve this output swing extra biasing must be placed about the inverting input of A_2. The voltage appearing at the non-inverting input of A_2, is equal to:-

$$V_+ = \frac{2.5}{R_B}\frac{R_L R_T}{R_L + R_T}$$

At 25°C the parallel combination of R_L and R_T is equal to 688.5 Ω, producing a voltage at the non-inverting input of A_2 of 0.345 V. For symmetrical output swing the output voltage of A_2 should be at 2.4 V.

The output of A_2, V_O, equals:-

$$V_O = \left(\frac{R_1R_2 + R_1R_3 + R_2R_3}{R_1R_2}\right)V_+ - 5\frac{R_3}{R_1}$$

Implies $$\frac{V_+}{R_2} = \frac{5 - V_+}{R_1} + \frac{V_O - V_+}{R_3}$$

Yielding $$\frac{0.345}{R_2} = \frac{4.66}{R_1} + \frac{2.06}{R_3}$$

Repeating the same equations for the minimum temperature and maximum temperature yields:-

T_{min} $$\frac{0.298}{R_2} = \frac{4.70}{R_1} + \frac{0.502}{R_3}$$

T_{max} $$\frac{0.392}{R_2} = \frac{4.61}{R_1} + \frac{3.61}{R_3}$$

Solving these three equations to get values for R_1, R_2 and R_3 gives:-

$$R_1 = 16.0\ k\Omega$$

R_2 = 953 Ω

R_3 = 3.00 kΩ

The TLE2022 provides good accuracy whilst maintaining an overall low power consumption, and even when working off a single 5 V rail the offset voltage of the TLE2022A is still below 400 µV. Very few other devices can maintain these levels of accuracy while consuming only 450 µA of supply current.

2.9. TLC2201/2 - Ultra Low Noise CMOS Op Amp

The TLC2201 and TLC2202 are probably the **WORLDS lowest noise** CMOS or JFET input operational amplifiers. Designed using Advanced LinCMOS™ technology, these precision op amps have proved extremely popular in a number of different applications.

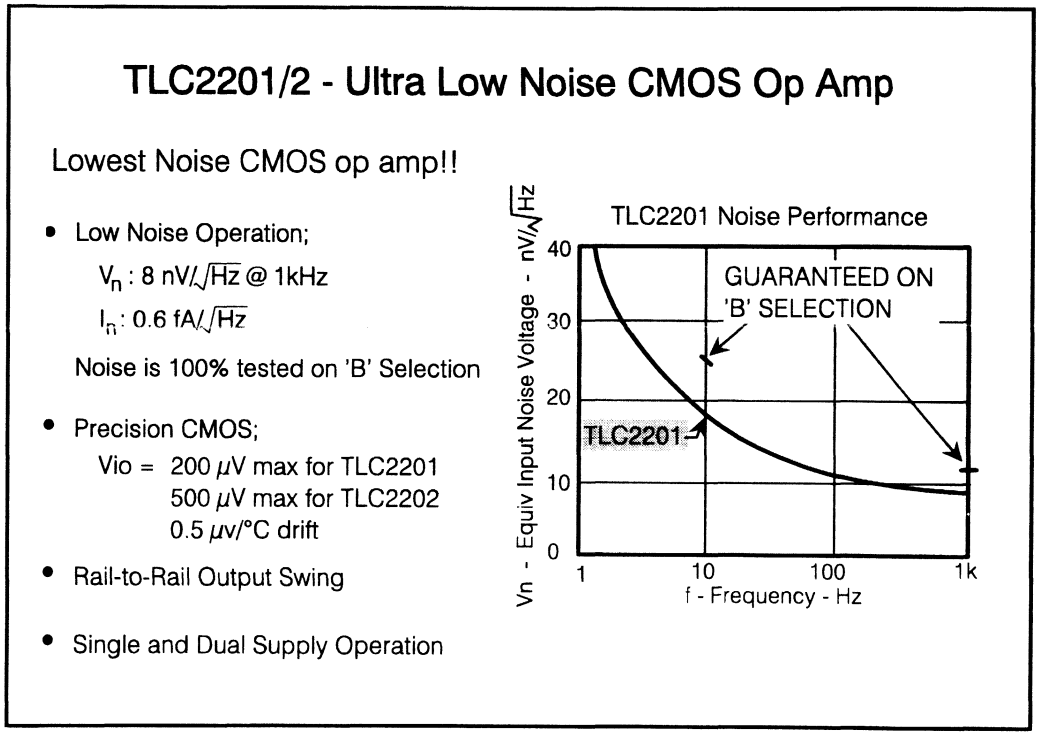


Figure 2.2.09 - TLC2201/2 - Ultra Low Noise CMOS Op Amp

2.9.1. Noise Performance

CMOS devices typically suffer from relatively high noise voltage and high 1/f frequency. Normally performing worse than Bifet op amps, they are typically not used in critical low noise applications. What all FET input devices benefit from, however, is a low noise current specification.

The TLC2201 and TLC2202 are unique because they combine low noise voltage (V_n) with extremely low noise current (I_n). A V_n specification of **8nV/$\sqrt{Hz}$ (@ 1kHz)** easily compares with some bipolar op amps, while I_n equal to **0.6fA/$\sqrt{Hz}$**, matches the very best FET input amplifiers. The result is an op amp which can now be used in a wide range of low noise applications. It achieves outstanding performance when interfacing to even medium impedance sources and can replace discreet JFETs or matching transformers to achieved improved performance and lower costs.

The noise performance is specified with single(5V) or dual supplies (higher supply voltages are more typical) and its performance is guarantied for the 'A' and 'B' selections ('A' by sample test, 'B' by 100% test).

Precision - The TLC2201 is one of the worlds most precise CMOS op amps (non chopper stabilised). A maximum offset voltage of 200µV combined with its obvious low offset and bias currents enables the device to be used in many precision applications.

Rail to Rail Output Swing - Like other LinCMOS^{TM} op amps, the TLC2201 and TLC2202 are ideally suited to single supply applications - under normal conditions the output is guarantied to swing within 50mV of the negative rail. A further benefit of these devices is the ability of the output to actually swing to each rail - With +/- 5V supplies the output will swing to +/-4.7V. In single supply applications dynamic range is often crucial and the ability of these devices to provide an increased output signal significantly improves the performance of single supply circuits.

Applications - Both devices offer a number of benefits to a wide range of applications. Low noise enables the device to be used as an interface to high impedance sensors including piezoelectric transducers, pH meters and pin diodes. The devices are therefore ideal for test and measurement equipment. Rail to Rail output swing increases the performance and capability of single supply circuits, and when combined with its precision the device is ideal as an accurate signal conditioning interface in data acquisition circuits.

2.10. Low Noise PIN Diode Amplifier

When interfacing to a wide variety of sensors the key factors in deciding which op amp will be used in the application are high input impedance, low input offset voltages and low noise voltages. A device perfect for applications requiring these specifications is the **TLC2201**.

No application shows the need for such parameters more clearly than when interfacing to a PIN photo-diode. Once again as in most applications requiring high input impedances it is the bias currents which are of importance, as feedback will multiply the op amp's input impedance by the circuit's loop-gain.

When using a PIN diode a small `dark' current will flow through it. This dark current is the bias current of the PIN diode. In parallel with the dark current is the current which is due to the light shining onto the device. It is the dark current along with the current noise which decides the error floor of the system. So if the dynamic range is not to be severely degraded the input bias currents of the op amp should be smaller than the dark current of the PIN diode. A typical PIN diode such as hp's 5082-4204 has maximum dark current of 100pA (at zero voltage bias and at 25°C). The TLC2201 with a maximum bias current of 20pA (calculated from the maximum bias current specifications over temperature) at 25°C provides a good safety margin.

The PIN diode is a light power to current converter and as such needs to interface to a trans-impedance amplifier. The result is that in order to get the required gain the feedback resistor of the op amp will

normally have to be large. This feedback resistor will form a pole with the shunt capacitance of the diode and the op amp's input capacitance, which can lead to instability. Although this effect may well be reduced by the parasitic board capacitance which is in effect in parallel with the feedback resistor. This 'feedback' capacitor can be increased to reduce the circuit's wide band noise, but this will reduce the application's bandwidth. Hence the required gain decides the value of R_f and the required signal bandwidth decides C_f. As well as converting the signal current to a voltage, the large feedback resistor adds to the offset voltage of the op amp by multiplying the bias currents of the op amp and the dark current of the PIN diode by its value.

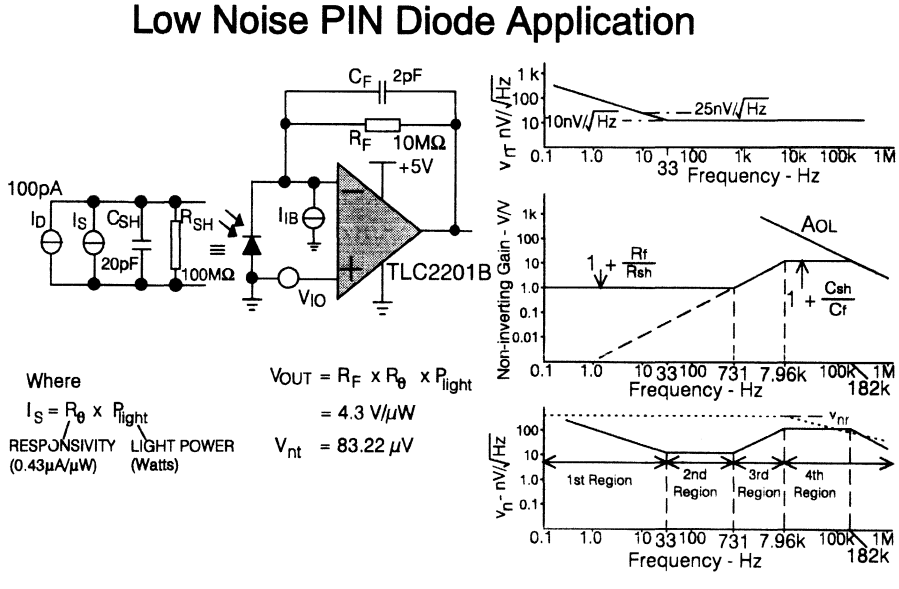


Figure 2.2.10 - Low Noise PIN Diode Application

The equivalent model of a PIN diode contains a shunt resistance, R_{sh}, which coupled to the feedback resistor gives the op amp a non-inverting gain of $1+R_f/R_{sh}$ (which frequently exceeds unity). It is therefore very important to use an op amp with low offset voltages and drift. The PIN diode's shunt capacitor also provides a limit to the range of frequencies over which the diode can be operated. Like all semiconductor barrier capacitances it is very voltage dependent, and can be reduced by placing a negative voltage across the diode.

The overall low frequency output voltage will therefore consist of the following factors:-

$$V_O = R_f * R_\phi * P_{light} + R_f * I_D + V_{io} * \left(1 + \frac{R_f}{R_{sh}}\right) + R_f * I_{ib}$$

where R_ϕ is the responsitivity of the diode to light power (in amperes per watt), and P_{light} is the amount of light falling onto the diode's sensitive area (in watts).

The temperature effects of the PIN diode dominates any drift effects of the op amp's V_{IO}. R_{sh} will tend to halve every 10°C, just as the bias currents will tend to increase. The 0.5μV/°C (typical) drift of the TLC2201 will be swamped by the change in gain due to R_{sh}.

As with all high impedance applications, the input stage is very susceptible to interference and leakage from the board. Any current injection into the input can be converted into millivolts of offset error. For this reason, it is standard practice for guard rings to be placed around the inputs of the op amp, reducing the influence of interference around the board. To decrease leakage of the board a Teflon based board will normally give the best performance.

In addition to offset errors, which are dc, noise errors will be introduced due to the PIN diode's noise and the op amp's noise.

The noise current will be the shot noise due to the dark current of the PIN diode and the bias current of the op amp. The noise current of the TLC2201 is 2.53fA/$\sqrt{Hz}$ while the dark current of the PIN diode would generate 5.66fA/$\sqrt{Hz}$. The feedback resistor will generate noise due to the noise currents of the PIN diode and the op amp and also its own thermal noise. A 10MΩ resistor generates 62nV/$\sqrt{Hz}$ (due to shot noise of the PIN diode and op amp) and 406nV/$\sqrt{Hz}$ (due to thermal noise). At these values the noise voltage of the TLC2201 (guaranteed to 25nV/$\sqrt{Hz}$ at 10Hz) would seem to be negligible, but the shot noise and thermal noise appear directly on the output of the op amp while the op amp's noise voltage will be multiplied by the op amp's gain. The op amp's gain will increase above the low frequency gain to 1 + C_{sh}/C_f. This gain will only be band-limited by the op amp's unity gain bandwidth. The non-inverting gain can rapidly increase over temperature (due to the large variance in R_{sh}, at a faster rate than the current noise, so a low noise voltage device is the best solution.

The non-inverting gain of the TLC2201 is:-

$$Gcl = G_{cl} = 1 + \left(\frac{R_f}{1 + s * R_f * C_f}\right) * \left(\frac{1 + s * R_{sh} * C_{sh}}{R_{sh}}\right)$$

At low frequencies the R_f/R_{sh} ratio will dominate, and at higher frequencies the C_{sh}/C_f ratio will decide the noise and ac gain. The poles of the circuit will be at:-

$$f_1 = \frac{1}{2\pi}\left(\frac{1}{C_{sh} + C_f}\right) * \left(\frac{R_{sh} + R_f}{R_{sh} * R_f}\right)$$

$$f_2 = \frac{1}{2\pi * R_f * C_f}$$

With R_{sh} = 100MΩ, R_f =10MΩ, C_{sh} = 20pF and C_f = 2pF the poles are at f_1 = 731 Hz and f_2 = 7.96kHz. f_2 will also be the frequency when the trans-impedance gain of the TLC2201 starts to roll off.

At low frequencies the noise voltage of the TLC2201 will be amplified by 1.1 but at the higher frequencies it will be amplified by 10. This splits the noise curve into three distinct parts; the low frequency gain, transition gain and the high frequency gain. At higher frequencies the gain bandwidth product will reduce the gain. A further complication to the noise analysis is the flicker effect of the op amp's noise voltage, and so making 4 regions to the curve.

The first region is from virtually dc to the 1/f corner frequency of the TLC2201B which is of the order of 33Hz. Over this region the noise voltage of the TLC2201 follows this approximate equation:-

$$V_n^2 = \left(\frac{v_{n(10)}^2 - v_{n(1k)}^2}{f} * 10\right) = \frac{4810 * 10^{-18}}{f}$$

Where $v_{n(10)}$ is the noise voltage specification at 10Hz, $v_{n(1k)}$ is the specification at 1kHz.

Calculating the noise over the region of 0.01Hz to 33Hz (ignoring the noise below 0.01Hz) and adapting that equation yields

$$V_{n1}^2 = 4810 * 10^{-18} * \left(1 + \frac{R_f}{R_{sh}}\right)^2 * \ln\left(\frac{f_c}{f_a}\right)$$

$$V_{n1} = 69.35 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{\ln\frac{100}{0.01}} \quad \text{..... nV}$$

$$= 231.5\text{nV}.$$

The second region will cover the frequency range 33Hz to 731Hz. Over this frequency range the noise voltage is `white' and so has equal power per unit frequency and so the noise included over this range is calculated as follows:-

$$V_{n2} = v_{nwhite} * \left(1 + \frac{R_f}{R_{sh}}\right) * \sqrt{f_1 - f_c}$$

$$= 12 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{731 - 33} \quad \text{..... nV}$$

$$= 348.7\text{nV}$$

The third region is where the resistances are being shunted out by their parallel capacitances, here the gain is increasing by 20 decibels per decade. By extrapolating this curve down to the 1Hz point the noise produced can be considered as increasing with frequency, simplifying the calculation. The equation of this line is:-

$$V_{n(1Hz)} = \left(1 + \frac{Rf}{Rsh}\right) * \left(\frac{v_{n(1kHz)}}{f_1}\right)$$

The noise content within the f_1 to f_2 band will be the area under this curve, the actual integration will be of the noise voltage squared. Therefore the noise content over this region results in the following equation:-

$$V_{n3} = \left(1+\frac{R_f}{R_{sh}}\right)*\left(\frac{v_{n(1kHz)}}{f_1}\right)*\sqrt{\frac{f_2^3}{3} - \frac{f_1^3}{3}}$$

$$= 1.1 * \frac{12}{731} * \sqrt{\frac{(7.96*10^3)^3}{3} - \frac{731^3}{3}}$$

$$= 7.40\mu V$$

Over the fourth region the noise is flat, but the gain then starts to follow the open loop characteristic of the op amp. This introduces a bandwidth limit of:-

$$BW = \frac{B_1}{1+\frac{C_{sh}}{C_f}} - f_2$$

BW will be multiplied by $\pi/2$ to achieve the noise bandwidth, hence the noise voltage contained in the fourth region has this characteristic:-

$$V_{n4} = v_{n(1kHz)}*\left(1 + \frac{C_{sh}}{C_f}\right)*\sqrt{\frac{\pi}{2} * BW}$$

$$= 12*\left(1+\frac{20}{2}\right)*\sqrt{\frac{\pi}{2}*174*10^3}$$

$$= 69.0\ \mu V$$

In addition to the noise voltage from the amplifier, there will be the noise voltage due to the thermal noise of the feedback impedance and to the noise voltage generated by noise current through the feedback impedance.

Only the real part of the feedback impedance produces noise and just as the signal gain rolled off at f_2 so will the thermal noise. The thermal noise will therefore follow this characteristic:-

$$V_{nr} = \sqrt{4kTR_f}*\sqrt{f_2 *\frac{\pi}{2}}$$

$$= 45.4\ \mu V$$

The noise current will generate a noise voltage equal to:-

$$V_{nc} = i_n * Re\left(\frac{R_f}{1 + s * R_f * C_f}\right)$$

$$= \sqrt{5.66^2 + 2.53^2}*10^{-15}*R_f*\sqrt{f_2*\frac{\pi}{2}}$$

$$= 6.93\mu V$$

The total noise voltage will be the RMS sum of all noise voltages:-

$$Vnt = \sqrt{V_{n1}^2 + V_{n2}^2 + V_{n3}^2 + V_{n4}^2 + V_{nr}^2 + V_{nc}^2}$$

$$= \sqrt{0.231^2 + 0.349 + 7.40^2 + 69.0^2 + 45.4^2 + 6.93^2}$$

$$= 83.22\ \mu V$$

Comparing each of the noise voltages over each region, the overall output noise voltage is dominated by the thermal noise of R_f and the out of frequency of interest bandwidth noise voltage of the op amp.

The signal to noise ratio relative to R_f is $\sqrt{R_f}$, so as R_f increases the output increases, the thermal noise increases but at a much reduced rate.

The noise of the op amp in region 4 can be reduced by increasing C_f, but this reduces the bandwidth of the application, and C_f will normally have been chosen to meet the application's requirements. A better way of reducing this high frequency noise is to reduce the op amp's high frequency gain by reducing the value of C_{sh}. This can be done by applying a negative voltage across the diode. The effect of this is to raise the frequency of f_1 whilst lowering the high frequency gain of the op amp.

In the application shown the common mode range of the TLC2201 is being exploited in a single rail circuit making the application of a negative voltage across the diode impossible.

Another point to note is that the speed of this application is limited by C_f and not the op amp, if a faster application was required the trans-impedance gain would need to be reduced, but this would also reduce the signal to noise ratio of the application.

2.11. Opto Sensor Considerations

An important application for signal conditioning, is to amplify sensor signals from the outside 'real' world; and to generate appropriate signals for conversion to digital processing. In this section are two examples of how light sensing functions can be easily realised by integrated opto sensors. Current-mode light sensors can be combined on a single chip with appropriate operational amplifiers, and then with data conversion elements to make high performance light sensing devices.

In a photo diode, incident radiation is absorbed by the silicon, to generate hole-electron pairs. These in turn give a photo-current across a reverse-biased p-n junction.

For a photo diode current-mode sensor, the current is proportional to the light intensity.

The Texas Instruments' LinCMOS(TM) process, used extensively for low input-offset operational amplifiers, can be easily adapted by the addition of light shields to make integrated photo sensor structures. A photo diode made by this process is responsive from 400nm to 1100nm (visible and short infra-red) when encapsulated in transparent plastic. The TSL250 and TSL220 integrated light sensors respond over this entire spectral range. However, by modified encapsulation a more restricted response (visible only, or infra-red only) can be achieved.

2.12. TSL250 Light-To-Voltage Converter

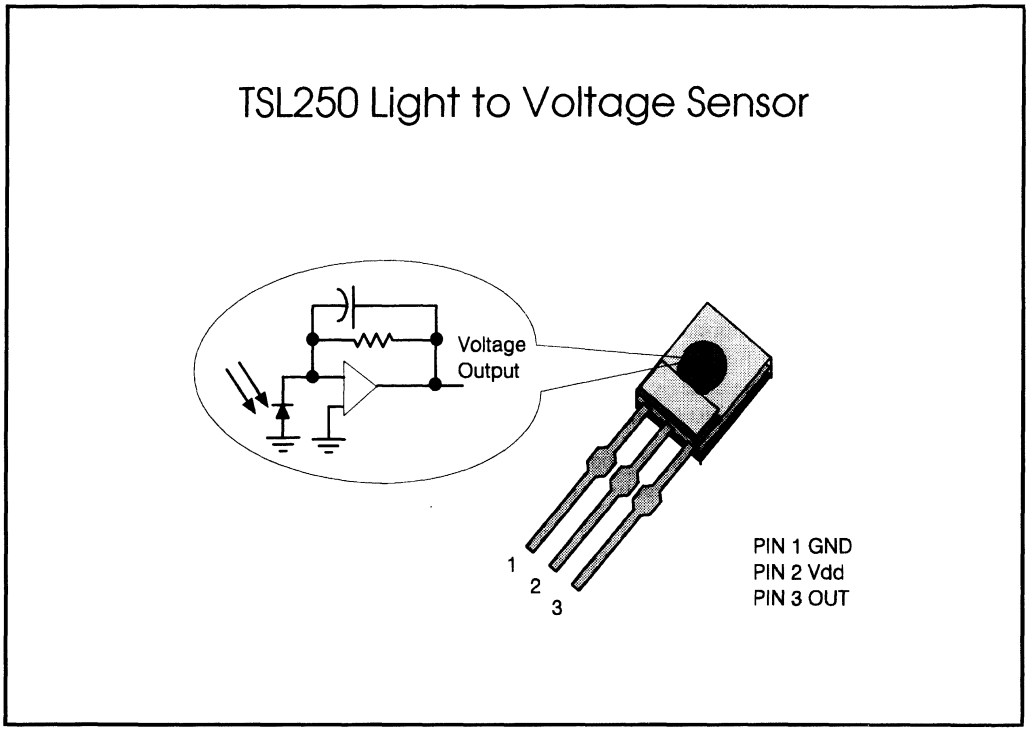


Figure 2.2.11. - TSL250 LIGHT-TO-VOLTAGE CONVERTER

Overview

In this section , we shall describe how a current mode sensor is combined on a chip with relatively simple signal conditioning elements, to make a useful device. The device, the TSL250 light-to-voltage converter, solves some basic application needs. It is particularly suitable for analogue measurement of low light levels in an electrically noisy environment.

In the TSL250, a large area photo diode is combined with a transimpedance amplifier, so the photo diode current output is converted to an output voltage.

Three versions of the device are produced, with different photo diode areas, and internal feedback resistor values.

Sensitivity Variants

TSL250 gives 2V output for 25 microwatts/cm^2

TSL251 " " for 60 microwatts/cm^2

TSL252 " " for 425 microwatts/cm^2

To get some idea of what these incident light levels mean, we can consider a photometric equivalence (for visible radiation) of **90 lux = 14 microwatts/cm^2.**

Dusk, when street lights are turned on, is about 70 lux. The TSL250 gives 2V output at 150 lux. Office lighting at a work surface is typically 300-400 lux, where a TSL251 would give 2V output. The TSL252 would give 2V output in outdoor daylight illumination.

Application

The TLS250 family is appropriate for a wide range of light sensing applications in light level control over a wide range of light levels, for security applications, and for boiler flame control in gas or oil heaters.

Characteristics

The LinCMOS^{TM} transimpedance amplifier (similar to the well-established Texas Instruments operational amplifier TLC272) provides stable low input offset. The TSL250 offers high dynamic range, with linear output up to 3V, with only 3 mV output in the dark.

The TSL250 has a significant advantage over discrete photo diode light sensors under low illumination, since the high impedance output node of the diode is internal to the device. This makes the TSL250 inherently less sensitive to external electrical noise, so a highly stable sensitive detector can be realised without expensive and cumbersome screening techniques. Similarly the TSL250 is inherently less prone to current leakage problems in detector circuit assemblies.

In summary, the TSL250 family has a highly linear, stable, low-impedance voltage output. The TSL250 output is stable with temperature, changing by 1 micro volt per degree Celsius. This is because the temperature coefficient of the polycrystalline silicon feedback resistor compensates the temperature coefficient of the photo diode.

The TSL250 operates off a single supply voltage (it is characterised at VDD= 5V , but will operate between 3V and 9V), and consumes little current (800 micro amps at VDD=5V when illuminated).

The TSL250 family is offered in a high-volume clear plastic sidelooker package.

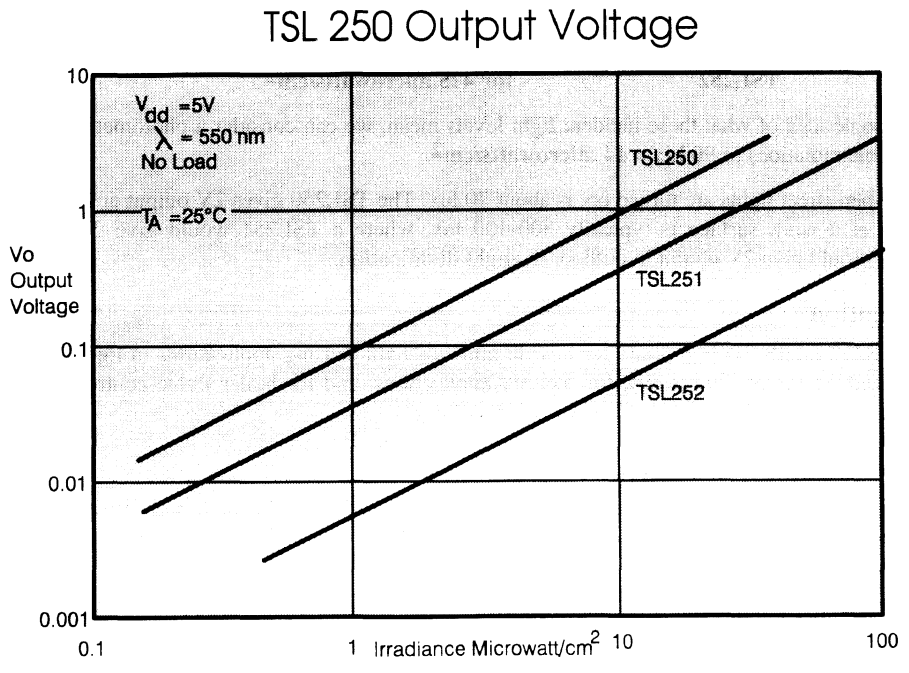


Figure 2.2.12. - TSL250 OUTPUT CHARACTERISTICS.

Speed Vs Responsivity

Figure 2.2.12 shows the linear output characteristics of the TSL250, TSL251 and TSL252. The internal feedback increases from the TSL252 to the TSL250. As the feedback is increased the speed is reduced. The TSL252 output rise and fall times are typically 7 microseconds, for the TSL251 they increase to 90 microseconds, and for the TSL250 they are 360 microseconds. The basic design could be extended to higher speed operation, trading responsivity for speed, by reducing the diode area and the feedback resistor and capacitor values -- the extremely low dark voltage resulting from the LinCMOS (TM) technology would permit this.

2.13. TSL220 Light-To-Frequency Converter

Overview

The TSL220 is a light-to-frequency converter, and combines a large area photo diode with a patented light-to-frequency converter to provide an output that is very convenient for a microcomputer, or indeed any digital technique, to handle.

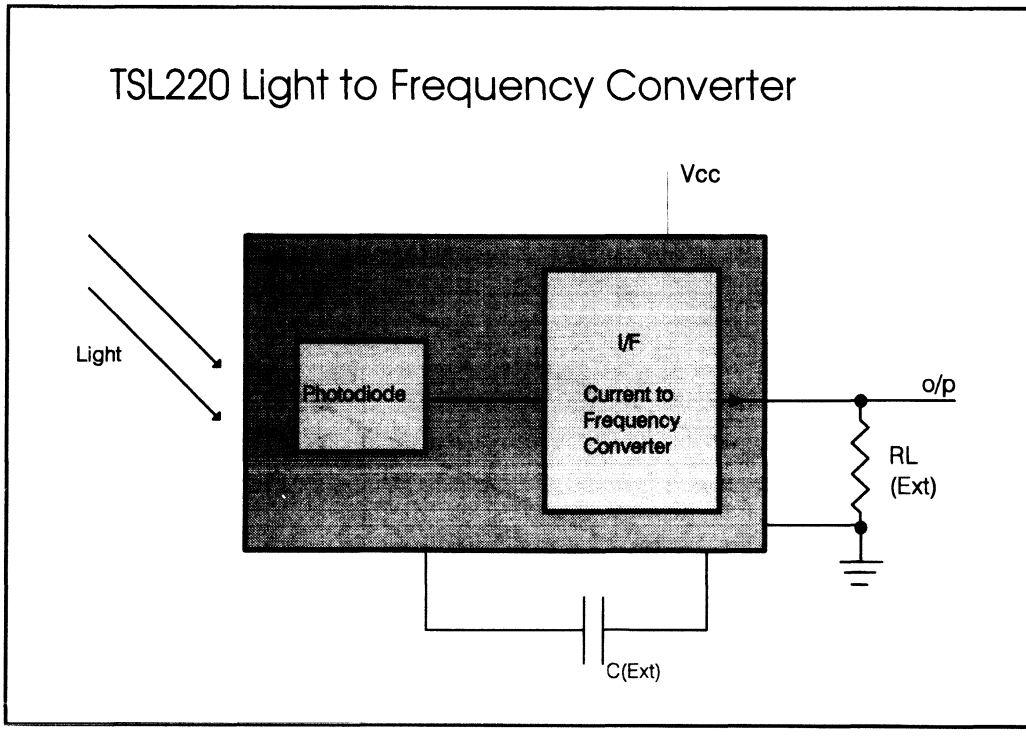


Figure 2.2.13. - TSL220 LIGHT-TO-FREQUENCY CONVERTER

Characteristics

The output of the TSL220 consists of a train of 4-volt pulses, the output frequency being proportional, over a wide range , to the intensity of the light incident on the photo diode surface. The TSL220 is extremely linear from 1Hz to 1MHz, and has an extremely high dynamic range -- under office illumination the output frequency is typically 150 kHz, while in the dark the frequency is typically 1 Hz !

The TSL220 operates off a single supply voltage (guaranteed performance at 5V, operable between 4 and 10 volts) , and the output is CMOS compatible. The TSL220 is offered in a high volume clear plastic 8-pin dual-in-line package.

Applications

The TSL220 is very suitable for precise measurement of light level. Since one can measure how much of the photo diode area is covered, the TSL220 can also be used as a precision (0.2 micron) analogue edge sensor.

The form of the output is very easy to handle, as pulses can be easily counted over a measured time set by a clock circuit.

The TLS220 is thus particularly suitable for applications where precision light or position measurement forms parts of a microprocessor- or digital- control system. Such applications include light metering, mechanical registration, printer paper positioning, smoke and dust detection, vibration detection, and coin control.

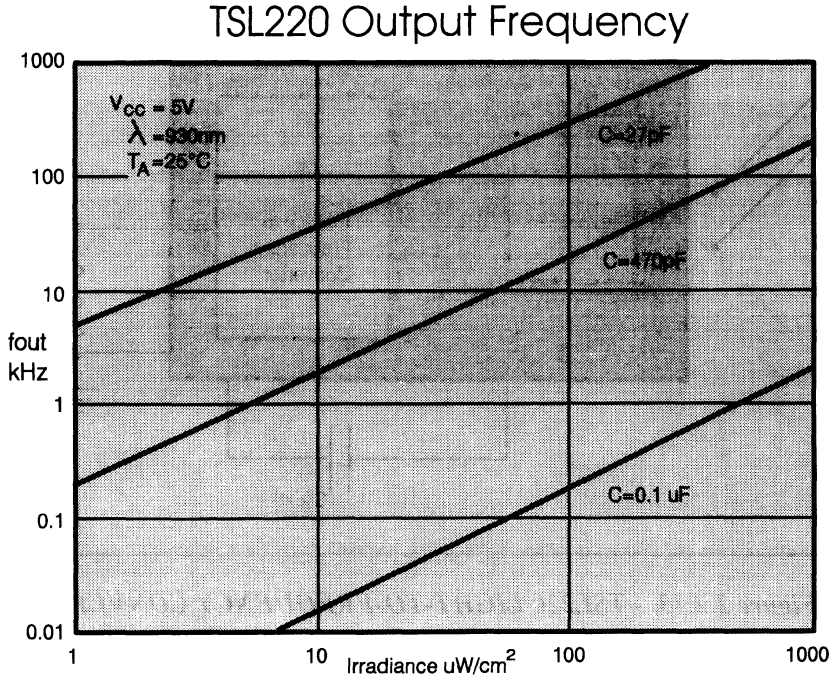


Figure 2.2.14. - TSL220 Output Frequency

Frequency Adjust

Many low cost digital and microprocessor techniques are not capable of being run at the high output frequency rates of which the TSL220 is capable. The frequency range of the TSL220 can be adjusted by means of a single external capacitor.

TSL220 Metering Application

Many simple application examples of the use of the TSL220 are given in the data sheet. A further example of the ease with which the TSL220 output can be handled by a microcomputer is given in Figure 2.2.15

In this example the low-cost Texas Instruments field programmable 8-bit micro controller TMS370C710 is used.

TheTMS370C710 features 4k bytes of program EPROM, 256 bytes RAM, 256 bytes data EPROM, a 16-bit timer and an on-chip watchdog for system integrity. It is supplied in a low cost 28-pin PLCC package.

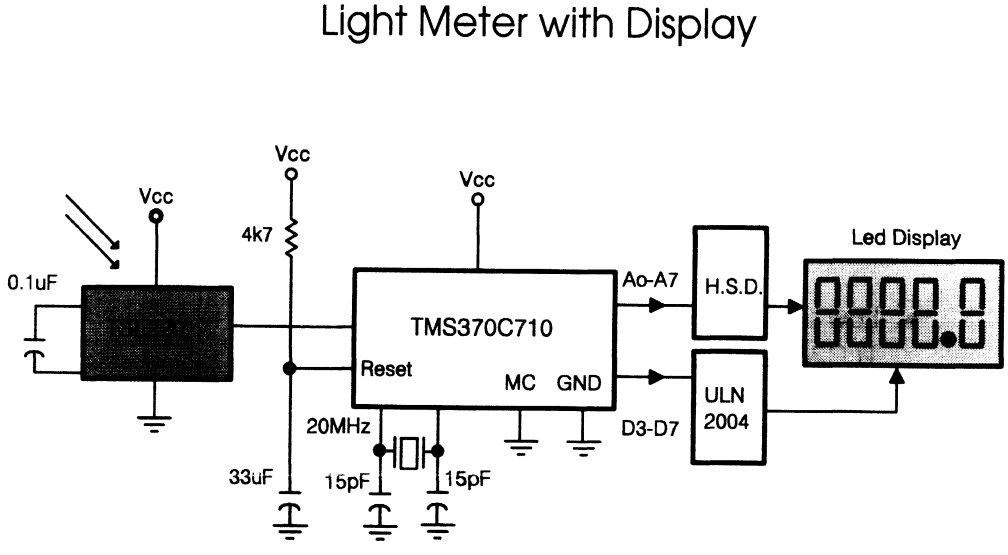


Figure 2.2.15. - TSL220 LIGHT METERING USING A PROGRAMMABLE MICRO CONTROLLER

TSL220 Metering Schematic

In this example of a calibrated light-(lux-)meter, the pulse train from the TSL220 is fed directly to the Timer 1 input capture pin of the micro controller. A 20MHz crystal is supplied to the micro controller, and the external capacitor of the TSL220 is set to 0.1 micro farad. The timer prescale is set to 2ee18 (/4) , giving a 16 bit overflow at 0.052 seconds.

70 lux (20Hz) resolution is 15 bits, and at 3000 lux (1kHz) resolution is 10 bits.

The 5 digit multiplexed LED display is driven by the micro controller. Spare CPU power of the micro controller would allow lux level to be directly displayed and film speed to be entered. Calibration parameters can be stored in EEPROM to make use of the high resolution. A 5 x 3 user keypad can be attached to the system, and strobed using interrupts 1, 2, 3 and the 5 remaining spare I/O's.

2.14. TLC2652 - Chopper Stabilised Op Amp

Chopper stabilised operational amplifiers have been available for many years but when they were first released there was much resistance, by design engineers, to using them. It was felt they were too noisy as an op amp and also generated too much extra noise within a circuit. Recently however, engineers have started to appreciate the outstanding levels of performance that can be achieved by using a 'chopper'. It was realised that the so called noise problems were not such a real issue and that the performance and relative low cost of newer products was just too good to miss!

TLC2652 - Chopper Stabilised Op Amp

The Ideal Precision Amplifier

- Low and Stable Offsets
  TLC2652A : 1μV max
  TLC2652 : 3μV max
- Vio Drift; 30nV/°C max
  20nV/month max
- Low Bias Currents; 100pA max
- High Gains ; Avd = 135dB

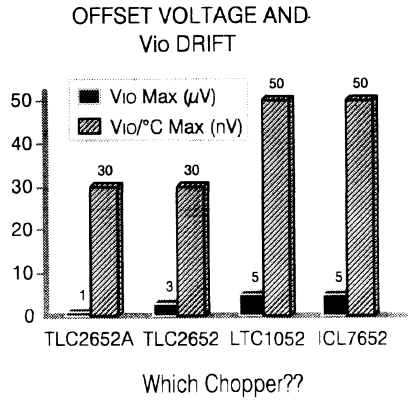


Figure 2.2.16. - TLC2652 - Chopper Stabilised Op Amp

The ideal precision op amp would require; ultra low offset voltages with negligible drift, bias and offset currents as low as those achieved by FET input amplifiers plus open loop gains, PSRR and CMRR would be high and noise would have to be at a minimum. Chopper stabilised op amps *very nearly* achieve the required level of performance to be the ideal precision amplifiers! If bandwidth is limited to reduce noise errors, then the precision of a circuit is determined more by external components and parameters (board layout, temperature gradients etc.) than the op amp itself.

Newer designs in particular are getting closer still to the ideal. The latest choppers released by TI are the **TLC2652/A and TLC2654/A** - both are **world leaders.**

The **TLC2652**, shown above, is a chopper stabilised op amp optimised for precision. The 'A' selection part has a **maximum offset voltage of just 1µV** and maximum drift specifications of **30nV/°C and 20nV/month**. Short and long term errors due to offset voltage are rarely a problem! The device is also CMOS so its bias currents are low causing minimal errors due to currents flowing in external resistors. A further benefit of chopper design techniques (see Figure 2.2.18) , is that they also benefit from extremely high gains, Avd is 135dB, and both the Power Supply and Common Mode Rejection Ratios are 120dB. The device easily meets the requirements of an 18 bit system.

If there is a limitation to choppers then it occurs in three areas: Noise voltage is typically high (although 1/f noise is practically removed) in most designs (see TLC2654, Figure 2.2.17, for something new!) and so care must be taken to limit the circuits bandwidth of operation. It should be noted however that with very low bandwidths, <0.25Hz, the noise from a chopper is often less than the noise of a bipolar op amp (this is because of their almost zero 1/f frequency). Secondly, because the devices are fabricated using CMOS technology then supply voltages are most commonly limited to +/- 8V. Thirdly, they are often just too good! Errors are typically introduced due to external factors, and these must be carefully considered when depending upon the precision available from these parts.

If you are looking for a device that achieves outstanding levels of precision the TLC2652A should be seriously considered.

2.15. TLC2654 - Low Noise Chopper Op Amp

Previous figures have discussed the limitations placed upon chopper stabilised amplifiers due to their relatively high noise voltage - at low frequencies the noise voltage of a typical chopper may be $100nV/\sqrt{Hz}$, significantly higher than most amplifiers. In practice this means that the circuit bandwidth needs to be limited to ensure that dc errors are dominated by the offset voltage of the amplifier and not by the noise of the op amp. When using the TLC2652A with an offset voltage of 1µV the circuit bandwidth needs to be limited to 1Hz.

Realising that this can cause problems in some applications TI has put significant effort into developing a chopper with much lower noise - the TLC2654 was the result. By increasing the chopping frequency from 450Hz (for TLC2652) to 10kHz it was possible to reduce the total noise of the amplifier by a half. This has been tried in the past but has always proved unsuccessful due to the resulting large increase in offset voltage and drift. Patented techniques used in the TLC2654 enabled its offsets voltages to stay at a minimum - 10µV is the maximum for the TLC2654A. Drift is also low at 0.05µV/°C and 0.06µV/month. It is not surprising that the TLC2654 won the "Product of the Year" Award from the US magazine Electronics.

TLC2654 - Low Noise Chopper Op Amp

By Increasing the Chopping Frequency to 10 kHz, Noise for the TLC2654 has been Significantly Reduced. Resulting in:

Increased Usable Bandwidth

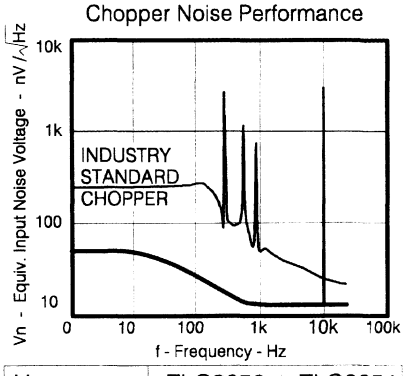
Reduced Intermodulation Effects

Precision Maintained:

Vio..... TLC2654A = 10μV max
TLC2654 = 20μV max

Vio Drift... 0.3μV/°C max
0.02μV/month max

(Still 4 years for 1μV of Vio Drift!!)



Vnpp	TLC2652	TLC2654
DC to 1Hz	0.8 μV	0.5 μV
DC to 10Hz	2.8 μV	1.5 μV

Figure 2.2.17. - TLC2654 - Low Noise Chopper Op Amp

In practice, choppers are often used as much for their low drift as for their absolute offset. By using the TLC2654 precision can be maintained and the usable bandwidth of the device can be increased. In practice this means that precision measurement applications, like weigh scales, can be designed with much improved response times.

2.16. High Performance Low Noise Choppers

Previous figures have discussed the limitations placed upon chopper stabilised amplifiers due to their relatively high noise voltage - at low frequencies the noise voltage of a typical chopper may be $100nV/\sqrt{Hz}$, significantly higher than most amplifiers. In practice this means that the circuit bandwidth needs to be limited to ensure that dc errors are dominated by the offset voltage of the amplifier and not by the noise of the op amp. When using the TLC2652A with an offset voltage of 1μV the circuit bandwidth needs to be limited to 1Hz.

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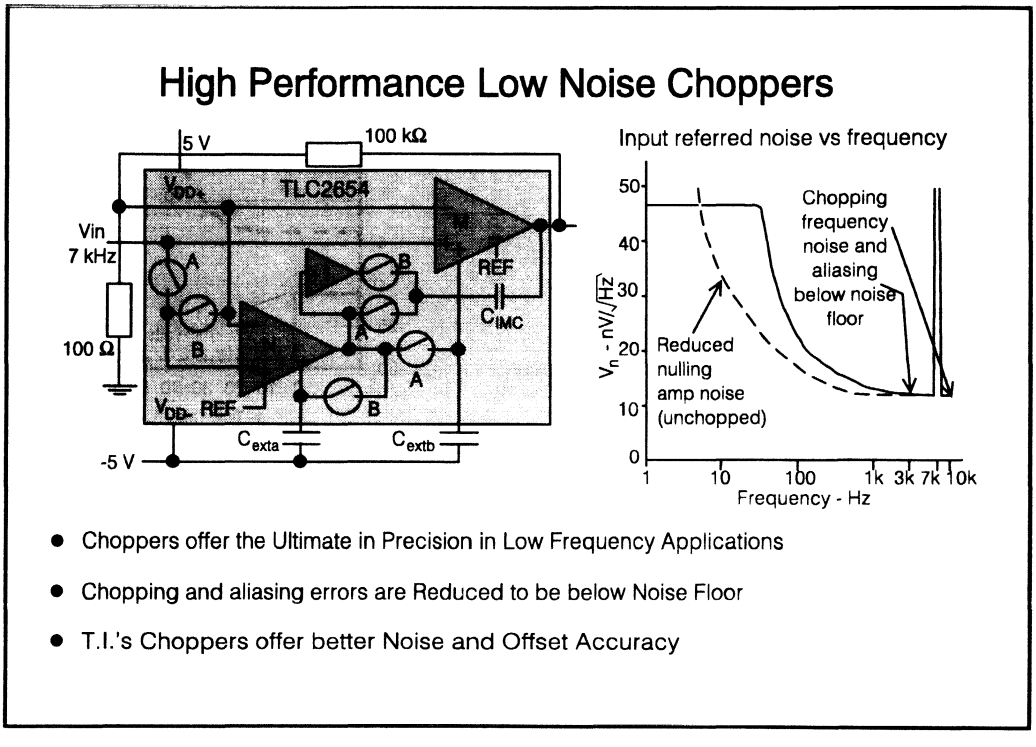


Figure 2.2.18. - Low Noise Choppers

In practice, choppers are often used as much for their low drift as for their absolute offset. By using the TLC2654 precision can be maintained and the usable bandwidth of the device can be increased. In practice this means that precision measurement applications, like weigh scales, can be designed with much improved response times.

2.17. Chopper Design Careabouts

When an application requires the absolute best performance from the chopper stabilised op amp, a number of factors and design considerations should be considered.

Chopper Design Careabouts

Noise

Limit Bandwidth... <1Hz

Intermodulation.... Vin < Fch/2

Variable Chopping Frequency

External Components

External Capacitors
- Low Leakage and Low Dielectric Absorption
- 0.1 μF or 1μF to Vdd- or CR

Overload Recovery
- CLAMP typically not required

Thermoelectric Effects

ESD and Latcup Protecction Circuits included

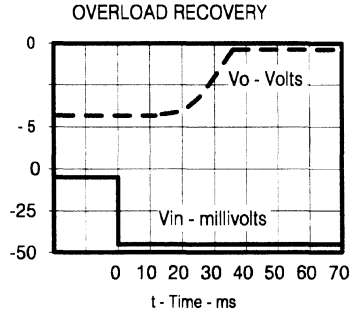


Figure 2.2.19. - Chopper Design Careabouts

Noise

Noise will be discussed in detail in sections 3.3 and 3.4 of signal conditioning, but the key points to remember are;

Limit Bandwidth:

The bandwidth of the op amp should be limited to reduce dc errors associated with the relatively high noise voltage of the amplifier. Take advantage of the device's low 1/f frequency however, as over very small frequencies (<1Hz), the choppers noise are less than many bipolar op amps!

Intermodulation effects:

If an input signal has a frequency component equal to greater than half the chopping frequency then intermodulation errors may be caused. In practice, chopper design techniques have minimised these errors (<70dB down on input signal) but it may be necessary, depending upon the frequency and magnitude of input signal, to filter out these components using an extra filter stage before the chopper.

Chopping Frequency:

The standard selection chopper op amps are available in an 8 pin package and have a predetermined internal clock frequency which defines the noise performance and offset voltage of the op amps. There are however, options available in a 14 pin package which have the capability of changing the clock frequency by the use of an external clock. This external clock signal can be fed directly into the CLK IN input and the INT/EXT pin is attached to V_{DD-}. When operated in a single supply configuration the device can be driven directly by TTL or CMOS logic without the need for extra level shifting. Although not critical, the duty cycle of the external clock should be kept between 30% and 60%.

The advantages of being able to modify the clock frequency of these choppers are essentially two fold. Firstly the noise and offset of the op amp can be optimised for your particular circuit and secondly the clock frequency can be matched to other clock signals present within your circuit.

2.17.1. External Components

Choosing and using the Right Capacitors:

The external capacitors, C_{XA} and C_{XB}, should be carefully chosen to ensure best operation of the amplifier. Specifically, special attention should be given to the leakage and dielectric absorption of these components.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and stand-offs are recommended for operation at T_A = 125°C. In addition, guardbands are recommended around the capacitor connections on both sides of the printed board to alleviate problems caused by surface leakage on circuit boards. Very thorough cleaning of the circuit board using alcohol or similar cleaning fluids is also recommended and errors can be further reduced by guarding the inputs of the amplifier with a ring connected to a low impedance node, normally ground.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset is needed, it is recommended that high quality film capacitors, such as mylar, polystyrene. or polypropylene, be used. in other applications, however, a ceramic or other low-grade capacitor may suffice.

The TLC2652 and TLC2654 have been designed to function with values of C_{XA} and C_{XB} in the range of 0.1µF to 1µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as closely as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that in many choppers, connecting these capacitors to the V_{DD-} pin will degrade the noise performance. This problem has been eliminated with these designs.

Overload Recovery Time/Output Clamp:

When large differential input voltage conditions are applied to the TLC2652 and TLC2654 choppers, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time. Typical recovery times are significantly faster for the TLC2652 and TLC2654 when compared to competitive products; however, if required, this time can be reduced further by using internal circuitry accessible through the clamp pin.

This Clamp circuit stops the output circuit from going into saturation due to a reduction in the closed-loop gain of the device (activated when the output is with 1V of each rail). The CLAMP pin is simply connected to the inverting input of the op amp, and it may, however, cause a slight degradation in the maximum output swing.

Thermoelectric effects:

To take advantage of the extremely low offset voltage drift of any chopper op amp, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius, which are orders of magnitude greater than the 0.003 μV/°C typical drift of the TLC2652).

To help minimise thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of non-soldered connections (such as sockets, relays, switches etc.) in the input signal path. Cancel thermoelectric affects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire wound resistors, is also beneficial. It is also recommended to try and minimise excessive power dissipation and temperature gradients across a circuit board. Large power dissipating devices should be kept well away from precision components and air movement should ideally be kept at a minimum.

Electrostatic Discharge and Latchup avoidance:

Both these topics are discussed in detail in figure 2.6.02, but points to note are;

ESD - Care must be taken when using these devices, but both the TLC2652 and TLC2654 have been designed to withstand ESD voltages up to 2000V without causing functional damage.

Latchup - Both products have been designed to withstand 100 mA surge currents without sustaining latchup.

For more details on both see figure 2.6.02.

2.18. High Precision Thermocouple Amplifier

A thermocouple is a temperature sensor made from two dissimilar metals. When the junction is heated, a small thermo-electric voltage is produced which increases with temperature.

Thermocouples are very small signal devices. For an S-type thermocouple, the average output voltage variation over its 0-1500°C temperature range is only 10.38 μV/°C. Although the linearity is poor, the temperature and voltage relationships are predictable and repeatable, which allows for downstream digital linearisation.

Two thermocouples are always present; a measurement junction and a reference junction. It can be proved that the temperature drift of the reference and the measurement junctions are equal. It is therefore only necessary to compensate for the drift with ambient temperature of the reference thermocouple. This technique is known as "cold junction compensation".

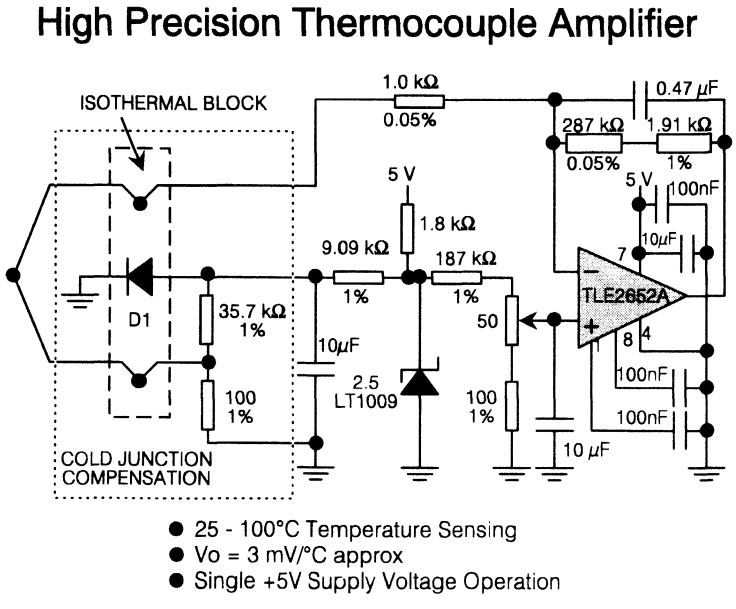


Figure 2.2.20. - High Precision Thermocouple Amplifier

In this example the approximate 2 mV/°C change of a low cost diodes forward voltage is resistively divided down to match the thermocouple's sensitivity (6 µV/°C) at 25°C ambient temperature. This counteracts any change in the reference junction temperature.

The circuit produces an output of 4.5 V for full scale. As the circuit is operating from a single 5 V supply, the op amp cannot swing quite to 0 V, thus limiting the lower end of the measuring range to 25°C. Ideally the 0°C would produce an output voltage of 0 V. The need for very highly accurate resistors can be avoided by using an additional gain setting trimmer.

Signal conditioning at such low levels is not trivial. Careful choice of components, PCB layout, grounding and consideration of thermoelectric effects at all junctions are of utmost importance. Mistakes in overlooking these could lead to external errors swamping any of those introduced by the op amp. When dealing with such small signals low frequency noise can be a real problem. The reference as well as the op amp should be filtered.

Due to the very small signals involved a very high performance op amp offering high open loop gain, low offset and low drift is required. These careabouts, at low frequencies, are best met by chopper stabilised op amps, ideally the TLC2652A.

To take advantage of the extremely low offset voltage drift of the TLC2652A - 30 nV/C maximum - care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with one another. This includes device leads being soldered to a printed circuit board. Dissimilar meal junctions can produce thermoelectric potentials in the range of several μV/°C, which is several orders of magnitude greater than the chopper's offset drift. Special care should also be given to air circulation around the op amp, as they can cause thermal gradients to appear across the PCB and metal junctions.

3. AC Applications

3.1. AC Precision Design

The dynamic range is one way of stating the system's performance. It can also be used as a measure of the system's errors. In most applications the devices having the greatest effect on the performance of the whole system will be those in the input stage, since there is not any way of recovering the errors that these devices introduce.

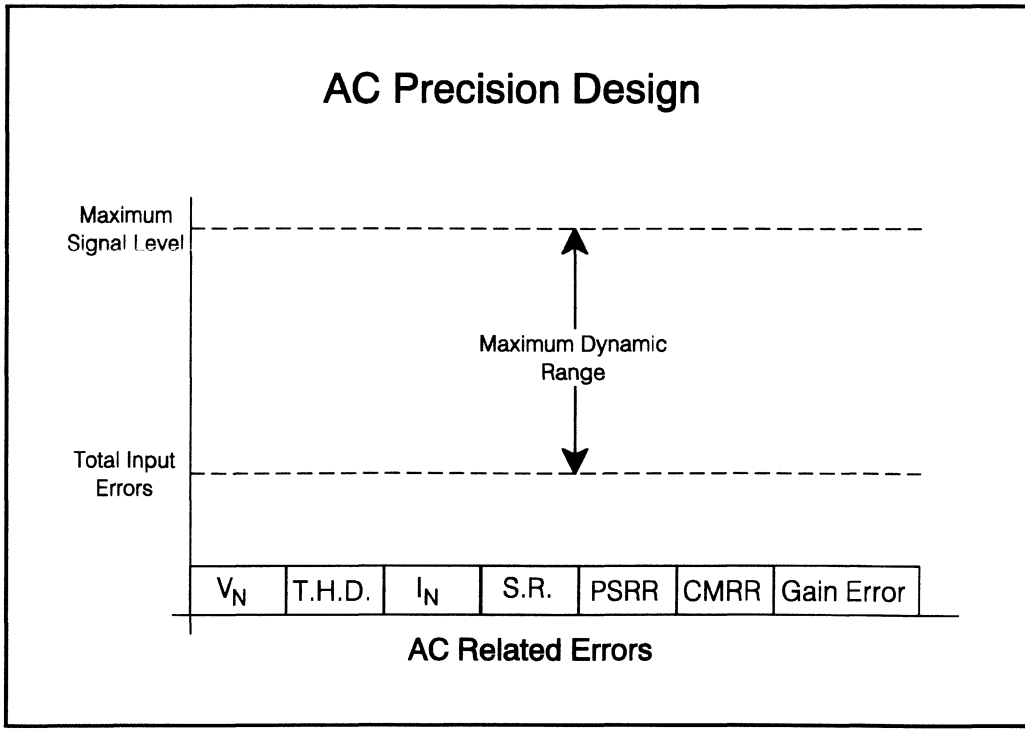
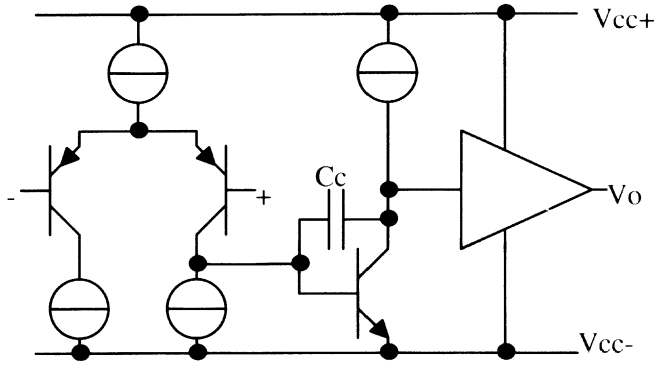


Figure 2.3.01. - AC Precision Design

The most basic internal configuration for an op amp is that shown below:



The transistors in the input stage are not truly linear devices and will therefore introduce distortion as they are driven with sinusoid input signals. The output stage with finite output impedance and output drive capabilities will also introduce distortion.

The current flowing through the input stage transistors will generate noise due to their bias currents and their dynamic resistances, and will appear on the inputs as noise currents and noise voltages. Further input offset voltage errors will arise from the changes in junction temperature of the device and during the lifetime of the device, all these must be taken into account when trying to sum all of the input errors.

To ensure high frequency stability, the open loop gain of the op amp at these frequencies must be reduced to unity before the phase shift exceeds 180°C (for unity gain stability). The most common way of doing this is via dominant pole compensation. This is done by placing a capacitor, C_C, between the output of the input stage and the output of the second stage (see diagram above). This limits the gain-bandwidth product of the op amp, causing its open loop gain to decrease at a rate of 20 dB/decade. This limits the device's accuracy over frequency.

The limited gain-bandwidth product of the op amp also reduces its Power Supply Rejection Ratio and Common Mode Rejection Ratio over frequency. This increases the effect of higher frequency noise on the supplies, as well as the errors due to higher frequency common mode input signals.

The compensation capacitor also limits the rate at which the second stage's output voltage can change, introducing a slew rate limit on the device. This is another possible limit to ac accuracy.

If the output signal's rate of change with time exceeds the device's slew rate capabilities then the output will be tied to the slew rate of the device and can cause the input to go into saturation generating further errors.

3.2. Dynamic Range and BITs of Accuracy

In order to determine the dynamic range of a system all of the effects discussed above should be considered.

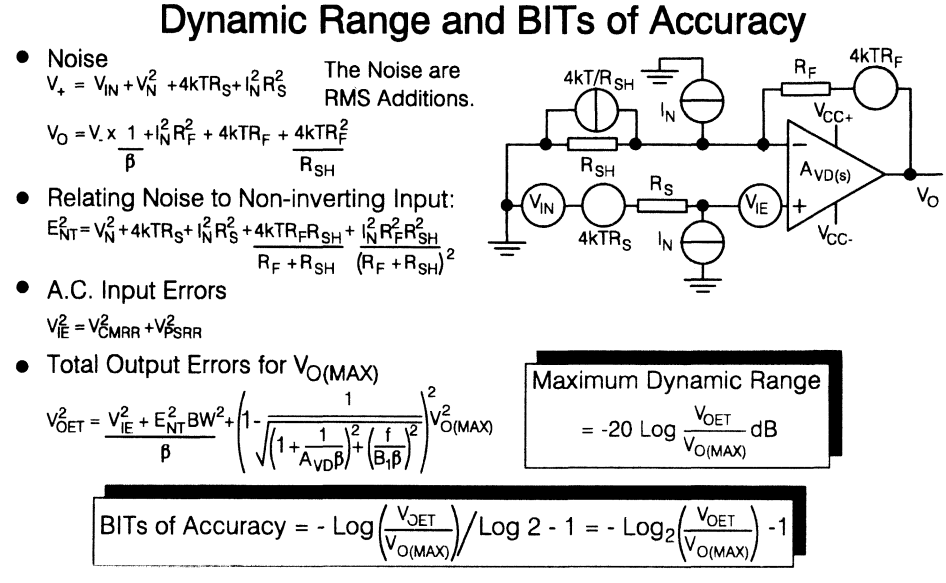


Figure 2.3.02. - Dynamic Range and BITs of Accuracy

3.2.1. Noise Analysis

The noise appearing on the non-inverting will be due to the noise voltage of the op amp itself and the thermal noise of the source resistance plus the voltage produced across the source resistor by the noise current. So neglecting other ac errors the potential at the non-inverting terminal will be:-

$$V_+ = V_{IN} + \left[V_N^2 + 4kTR_S + I_N^2R_S^2\right]$$

Where the noise is an rms addition.

The easiest way of taking into account of the noise appearing on the output which is due to the noise on the inverting input is by considering noise to be noise currents. So the output voltage, V_O, will be:-

$$V_O = V_- * \frac{1}{\beta} + I_N^2R_F^2 + 4kTR_F + \left(\frac{4kT}{R_{SH}}\right)R_F^2$$

Both the noise current, I_N, on the inverting input and the thermal noise current of the shunt resistor, R_{SH}, will generate noise voltage across the feedback resistor, R_F. The noise voltage appearing on the output due to the noise from the inverting input, can be referred to the non-inverting input by dividing it by the non-inverting closed loop gain to give:-

$$E_{NT}^2 = V_N^2 + 4kTR_S + I_N^2 R_S^2 + \frac{4kTR_F R_{SH}}{R_F + R_{SH}} + \frac{I_N^2 R_F^2 R_{SH}^2}{(R_F + R_{SH})^2}$$

$$= V_N^2 + 4kT(R_S + R_F \| R_{SH}) + I_N^2 \left(R_S^2 + (R_F \| R_{SH})^2 \right)$$

3.2.2. AC Input Errors

In addition to the noise there are the errors due to the power supply rejection ratio and common mode rejection ratio. These errors are normally uncorrelated and so should be RMS summed.

$$V_{IE}^2 = V_{CMRR}^2 + V_{PSRR}^2$$

So the total errors appearing on the output of the op amp will be the RMS sum of the ac input errors, total noise errors and the gain errors.

3.2.3. Gain Errors

The gain errors this time will be slightly different to the dc gain errors due to the phase shift in the open loop gain. The open loop gain of an op amp with single dominant pole compensation is:-

$$A_{OL} = \frac{A_{VD}}{\left(1 + \frac{jf}{f_p}\right)\left(1 + \frac{jf}{f_n}\right)}$$

Where f_n is the frequency of one or more other poles in the op amps frequency response.

Assuming that the frequency of interest is at frequencies where the phase shift of the other poles do not affect the op amp the open loop gain gets modified to:-

$$A_{OL} = \frac{B_1}{f_p + jf}$$

Using the op amp with feedback equal to β reduces the closed loop gain to:-

$$A_{CL} = \frac{\frac{B_1}{f_p + jf}}{1 + \frac{B_1\beta}{f_p + jf}}$$

Simplifies to

$$= \frac{1/\beta}{\left(1 + \frac{f_p}{B_1\beta}\right) + \frac{jf}{B_1\beta}} = \frac{1/\beta}{\left(1 + \frac{1}{A_{VD}\beta}\right) + \frac{jf}{B_1\beta}}$$

So the gain error, V_{OGE}, that appears on the output at maximum output swing is:-

$$V_{OGE} = 1 - \frac{1}{\sqrt{\left(1 + \frac{1}{A_{VD}\beta}\right)^2 + \left(\frac{f}{B_1\beta}\right)^2}} V_{O(MAX)}$$

3.2.4. Total Output Errors

This results in the total output errors, V_{OET}, for maximum output swing:-

$$V_{OET}^2 = \frac{V_{IE}^2 + E_{NT}^2 BW^2}{\beta} + \left(1 - \frac{1}{\sqrt{\left(1 + \frac{1}{A_{VD}\beta}\right)^2 + \left(\frac{f}{B_I\beta}\right)^2}}\right)^2 V_{O(MAX)}^2$$

Where BW is the noise bandwidth of the op amp.

Having determined the total output errors the maximum dynamic range and/or the BITs of accuracy can be calculated from the equations defined in dc Applications section.

$$\text{BITs of Accuracy} = -\text{Log}\left(\frac{V_{OET}}{V_{O(MAX)}}\right) \Big/ \text{Log}2 - 1 \quad \text{BITs}$$

$$= \frac{\text{Dynamic Range}}{6.02} - 1 \quad \text{BITs}$$

The total harmonic distortion introduced by the device is another parameter that can be added to the ac input errors. It will normally be at a relatively low level until the loop-gain, $A_{OL}\beta$, about the op amp has decreased to less than 100, when it will start to increase. The level of distortion is very much design and technology dependent with high performance bipolar op amps giving the best performance

The effect of slew rate on the performance of the system is harder to quantify, as it will normally restrict the usable bandwidth, rather than introducing direct distortion at lower frequencies.

3.3. Noise Considerations

There are a number of factors to consider when developing a low noise circuit using operational amplifiers, these are discussed below:

3.3.1. Sources of noise

Johnson (or Thermal) Noise;

A resistor lying on a table will have a particular noise associated with it. Known as "Johnson Noise", this figure is not related to the quality of the resistor and its noise voltage is equal to;

$$V_n = \sqrt{4kTRB}$$

Where

k	=	Boltzmann's Constant	= $1.38 * 10^{-23}$ J/K
T	=	Absolute temperature in Kelvin	= (298 @ 25°C)
R	=	Resistance value	
B	=	Noise Bandwidth in Hz.	

It is often useful to remember that a 100kΩ resistor has a Johnson Noise equal to 40nV rms over a 1 Hz bandwidth.

Johnson Noise is unpredictable but has a gaussian distribution, giving it a flat spectrum over frequency. It must also be remembered that this Johnson Noise is independent and extra to the errors caused by current flowing through the resistor.

In a low noise circuit the Johnson Noise of the external source resistor is often the limiting factor and it is one which can not readily be reduced. An alternative source may be the only solution!

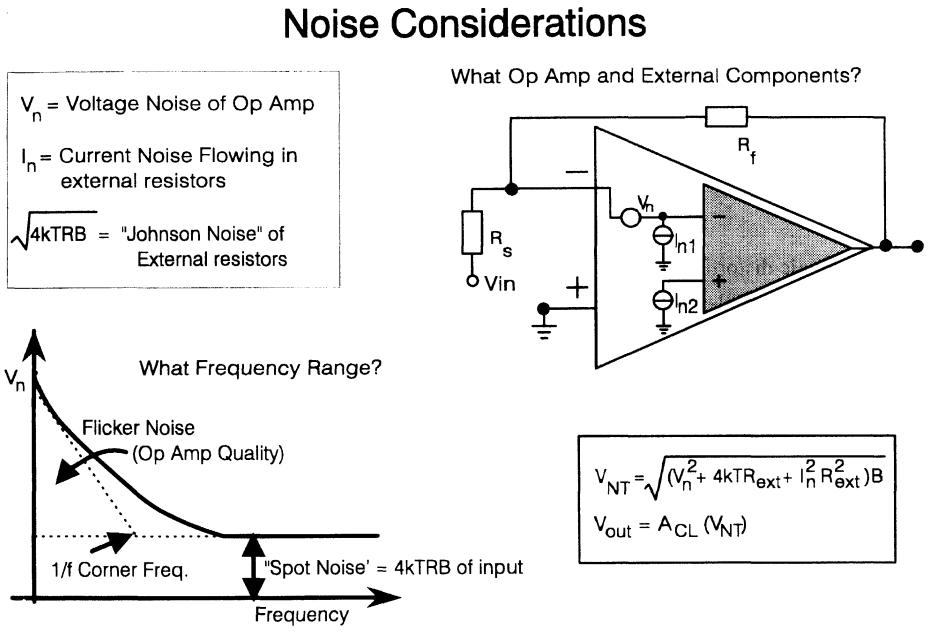


Figure 2.3.03. - Noise Considerations

Shot Noise;

Shot Noise(or schottky noise) is associated with the current flowing through a p.n. junction and is actually due to fluctuations in current. Shot noise becomes more dominant the lower the value of the actual current;

$$I_n = \sqrt{2qI_oB}$$

Where q = Electron Charge = $1.6 * 10^{-19}$ C

Io = dc operating Current

B = Noise Bandwidth in Hz

Like Johnson Noise, Shot Noise is unpredictable and is gaussian in distribution and is referred to as having a 'white' spectrum..

1/f or Flicker Noise;

Both operational amplifiers and resistors have noise characteristics different to what is expected from the Johnson Noise calculations. At low frequencies, noise is significantly increased, and follows a 1/f characteristic - i.e. the noise spectrum has an equal amount of power per decade of frequency. This noise, known as Flicker Noise, is very much dependent upon the quality of both the op amp and resistor. A Wire-wound resistor will have a lower noise than a carbon equivalent.

With operational amplifiers the amount of Flicker noise is very dependant upon the quality of the op amp and the level of care put into the design as well as the actual process being used. The point at which the flicker noise crosses the constant 'Spot Noise' of the op amp is known as the 'corner frequency'.

Popcorn Noise;

Popcorn Noise sounds like noise popping when played through a speaker. It is characterised by "hopping" between different noise levels, and can last from milliseconds to seconds. The source is not clearly understood but is reduced by cleaner processing. Good low noise processes should have no popcorn noise.

Summing Noise Sources

Noise Sources are random and therefore should be geometrically or RMS summed. The most well recognised formula for working out the total noise of an operational amplifier circuit which includes the different noise sources is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B} \quad \text{..... (1)}$$

Where V_n = Voltage Noise of Op Amp

I_n = Current Noise of Op Amp

$4kTR_{ext}$ = Johnson Noise of external Resistors.

3.3.2. Noise Related to an Op Amp

There are typically two parameters specified in the datasheet of an operational amplifier, noise voltage and noise current;

Noise Voltage;

The noise voltage of a bipolar op amp is due to the Johnson noise of the base spreading resistor r_{bb} and the Shot noise of the collector current in the input transistors. There is also an error due to the flicker noise, associated with the input transistors base current flowing through the base resistors. At low frequencies the noise is dominated by the Flicker noise whilst at high frequencies, the Johnson noise is the major factor.

The noise voltage of a FET input amplifier is dominated by the Johnson noise of the channel resistance and is normally significantly higher than a bipolar design.

The noise voltage characteristics for both parts have a 1/f characteristic although the 'corner frequency' of FET input designs is typically much higher than for bipolar. It should also be noted that CMOS

designs have a worse 1/f noise compared with Bifet op amps, but newer products developed using 'cleaner' CMOS technologies such as LinCMOS™ have greatly improved the noise performance and lowered the 1/f corner frequencies.

The 1/f region of the noise curve of an amplifier is particularly critical when designing precision circuits which operate at relatively low frequencies - very common in instrumentation equipment. An op amp with a low 1/f corner frequency is essential.

Current Noise;

For operational amplifiers with a bipolar input stage, the noise current is caused by Shot noise variations of the base current and flicker noise of r_{bb}. FET input amplifiers have a noise current specification caused by the shot noise associated with the gate leakage of the input FETs, this is significantly lower than for bipolar designs.

An op amp's noise current flows through the external resistors of an op amp generating an error source equal to $\sqrt{I_n^2 R_{ext}^2 B}$ - therefore the larger the external source resistors the larger the error due to noise current. Because the base current of a bipolar transistor is much higher than the leakage current of a FET transistor, the noise current of a CMOS or Bifet part is much lower than a bipolar design. FET input amplifiers are therefore normally used if a circuit has a large source resistance. As the bias current of a FET input part doubles for every 10°C increase in temperature, the noise current, I_n, increases by $\sqrt{2}$ for every 10°C increase.

Equation (1) above, shows how these parameters are combined. The result from this equation is in fact an RMS term which is often preferred in its peak to peak form. If the RMS noise voltage is multiplied by 6.6, you have a 99.7% certainty that the peak to peak value will not exceed the result.

Further examination of equation (1) shows that there is a point at which the noise of a system is dominated by the external resistors. A term, of particular use when talking about bipolar op amps is the 'Equivalent Noise resistance', equal to V_n/I_n shows when the errors due to the noise current are than that due to the noise voltage

3.3.3. Noise Bandwidth

It can be seen from equation (1), that the Noise Bandwidth of the operational amplifier circuit is critical - the wider the frequency of operation the larger the amount of noise within that system. A low noise circuit must therefore have its noise bandwidth limited as much as is possible.

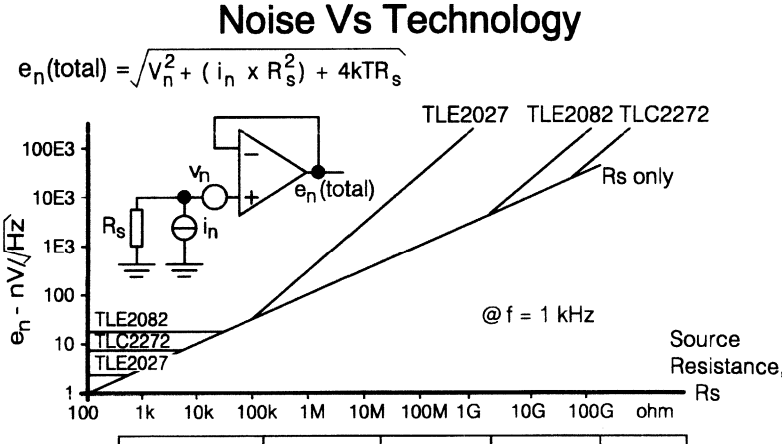
The Noise Bandwidth of an operational amplifier circuit is normally limited by using a filter network. It must be remembered, however, that the Noise Bandwidth is often very different to the RC Bandwidth of the filter which is limiting the noise. If a filter has a slow rolloff then the noise contribution by the signals with a higher frequency than the RC bandwidth can be significant. The Noise Bandwidth of a 1st order low pass filter (butterworth) is 1.57 x f_{3dB} of the filter. This is an increase of over 50%. A filter is of least 2 orders is normally recommended.

FILTER ORDER	NOISE BANDWIDTH
1	1.57 x f_{3dB}
2	1.11 x f_{3dB}
3	1.05 x f_{3dB}
4	1.03 x f_{3dB}
"Brick Wall"	1.00 x f_{3dB}

Noise on Output

Most noise calculations will work out the equivalent total noise on the input of the op amp. Like other errors this noise error is multiplied by the closed loop gain to give the equivalent noise on the output of the op amp.

3.4. Noise versus Technology



Process	BIPOLAR	BIFET	LinCMOS	
Parameter	TLE2027	TLE2082	TLC2272	UNIT
Noise Voltage	2.5	13	9	nV/√Hz
Noise Current	400	2.8	0.6	fA/√Hz
1/f Corner	3	1000	100	Hz

Figure 2.3.04. - Noise Vs Technology

The figure 2.3.03 discussed the relevance of noise voltage and noise current and how depending upon the source impedance each or both may be of importance. The graph and table in the figure 2.3.04 above compares the overall noise performance of low noise op amps from each major technology. The formula to remember is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B}$$

V_n = Noise Voltage of Op Amp

I_n = Noise Current of Op Amp

$4kTR_{ext}$ = Noise of Resistors.

Figure 2.3.04 shows that bipolar amplifiers are the best for a, providing the source resistance is small, low noise voltage. Amplifiers like the TLE2027 have extremely low noise voltage specifications which means that, providing the source resistance is small, they achieve the best overall noise performance.

As the size of the external resistors increase, the Johnson noise of these components begin to dominate the total noise equation. Not surprisingly, the lower the value of the op amps noise voltage, the smaller the resistor needs to be before it begins to prevail - resistor size can prove a severe limitation when designing low noise circuits with low noise op amps.

As the source impedance increases, there comes a point when the noise current, In, flowing through these resistors dominates the total noise equation. Because bipolar resistors have a significantly higher noise current than FET input amplifiers, this error term can quickly cause the largest error. Low noise CMOS designs like the TLC2201 have such a low noise current specification, combined with a relatively low noise voltage, that it is often the best choice even with medium sized external source impedances.

The other specification highlighted by this figure is the 1/f corner frequency of the op amp. Low noise bipolar designs will normally have much lower specifications than FET input designs (3Hz for the TLE2027), although again, the TLC2201 has a very good specification relative to other FET input designs. It is worth noting that the NE5534 has a high 1/f corner frequency and yet it is still recognised as a low noise part - 1/f should not necessarily be used to compare the performance of different amplifiers.

3.5. Low Noise Differential Amplifier

When designing low noise systems the voltage noise of the amplifier is not the only important parameter. The wide variety of transducers, and their resistances, can often make the noise voltage of the op amp negligible when compared to the Johnson noise of these resistances. With very high impedance transducers the noise current of the amplifier dominates the total circuit noise.

In most applications involving the **TLC2201B** and **TLC2202B** operational amplifiers the thermal noise of the source and/or feedback resistors will be the most important. This is due the TLC2201/2 having a maximum noise voltage of only $12nV/\sqrt{Hz}$ and a noise current of $2.53fA/\sqrt{Hz}$ (@25°C), giving it an effective noise resistance (ratio of noise voltage to noise current) of above 4MΩ. This means that only when dealing with impedances above 4MΩ is the effect of the noise current of the TLC2201 going to be larger than its noise voltage. The offset error that this impedance would create would be 80μV.

The 3 op amp instrumentation amplifier is a versatile configuration and can be used to yield the best performance from an op amp; in particular the TLC2201 with its high input impedance, good common-mode rejection ratio as well as its excellent input and output swings.

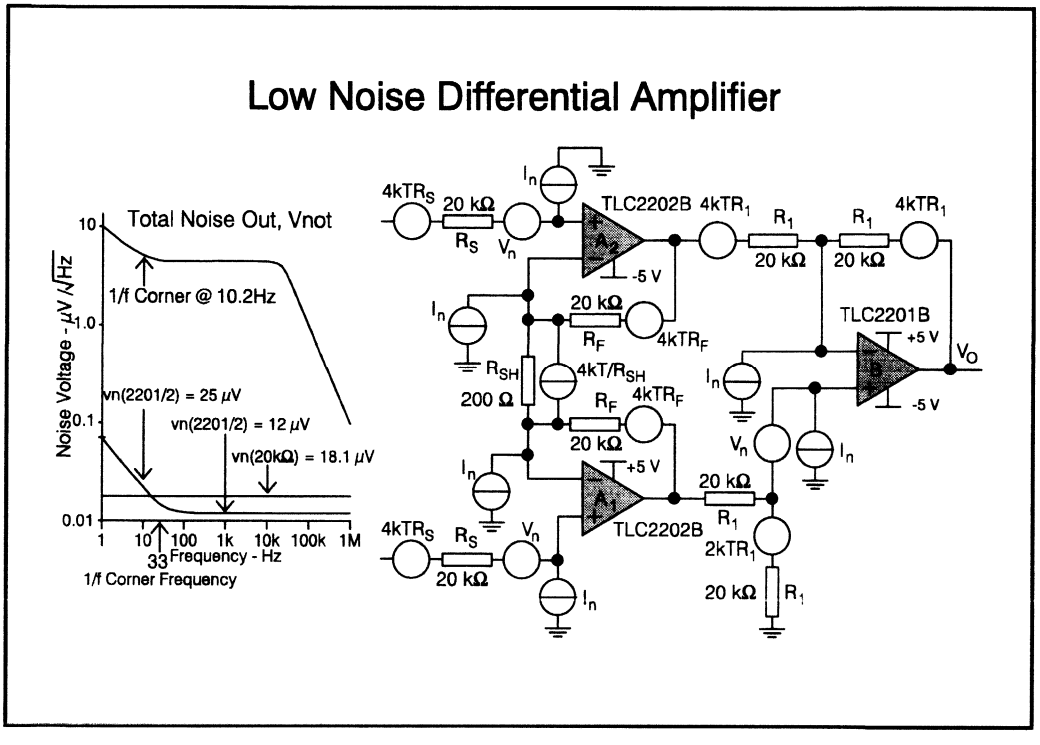


Figure 2.3.05. - Low Noise Differential Amplifier

As in most low noise systems the input stage will have the largest effect on the signal to noise ratio. Using the TLC2202 in the input stage makes use of its very low noise currents and noise voltages as well as its very low offset voltage. The common-mode range down to the negative rail adds further versatility to the application whilst maintaining the accuracy required.

When working out the noise of a system it is best to relate each stage's noise to its input. This will normally make analysis easier, as both the input signal and the input referred noise will be multiplied by the op amp's non-inverting gain, $1+ R_f/R_{sh}$, (signals via the inverting input will be multiplied by $-R_f/R_{sh}$). The instrumentation amplifier configuration adds some further complexity to the analysis; with the input stage sharing a resistor, R_{sh}, between its two op amps' inverting input terminals. The use of R_{sh} is two-fold; A, R_{sh} provides the instrumentation amplifier with its good common-mode rejection characteristics, and B, R_{sh} sets the gain at $1+2R_f/R_{sh}$. With the input stage sharing R_{sh} between the two op amps it is easier to consider the thermal noise of R_{sh} to be in the form of a current ($4kT/R_{sh}$), which adds to the noise current of each op amp's inverting input.

The sources of noise for both input stage op amps will be the same. The non-inverting input will exhibit the noise voltage, v_n, of the op amp itself, in addition will be the thermal noise of the source resistor, $4kTR_S$, and the noise generated by the noise current, i_n, through R_S. These voltages are uncorrelated and will therefore RMS sum together. Due to the virtual short across the op amps' inputs (the very high open loop gain forces the two inputs together) the noise voltage at the non-inverting input will appear at the inverting input. This means that the total noise on the non-inverting input will be multiplied by the inverting gain of the opposing op amp in the input stage. So the noise generated on the non-inverting input, v_{ni+}, of each op amp will be:-

$$V_{ni+} = \sqrt{v_n^2 + 4kTR_S + i_n^2 R_S^2}$$

The noise current on the inverting input will flow through the feedback resistor, R_f, creating a noise voltage at each op amp's output, which sums together with the thermal noise voltage of R_f. The noise current on the inverting input will be the noise current of the device plus the thermal noise current of R_{sh}. As this noise voltage is at the output of the op amp (just as the bias current error is added to the output of the op amp), referring it to the non-inverting input entails dividing it by the non-inverting gain. The resultant is the noise generated by a resistance equivalent to R_{sh} in parallel with R_f. This extra source generates further non-inverting input referred noise. However it will not appear at the inverting input, as the noise is actually being generated at the output.

Therefore the total noise voltage referred to the input, $v_{nri(1)}$, of amplifier A1 will be the noise generated at the non-inverting input summed with the noise due to the parallel combination of feedback resistor, R_f, and shunt resistor, R_{sh}. Therefore:-

$$v_{nri(1)} = \sqrt{v_{ni+(1)}^2 + i_{n(1)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh} + R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh} + R_f}\right)}$$

and the input referred voltage, $v_{nri(2)}$, of amplifier A2 will be:-

$$v_{nri(2)} = \sqrt{v_{ni+(2)}^2 + i_{n(2)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh} + R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh} + R_f}\right)}$$

The third amplifier will have a similar equation except that R_S will be replaced with $\frac{1}{2} R_1$ and $R_{sh}R_f/(R_{sh}+R_f)$ will be replaced with $\frac{1}{2} R_1$, yielding:

$$v_{nri(3)} = \sqrt{v_{n(3)}^2 + 2*4kT(\tfrac{1}{2}R_1) + 2 * i_n^2 * (\tfrac{1}{2}R_1)^2}$$

The output of A1 (*and for A2*) will be $v_{nri(1)}$ ($v_{nri(2)}$) multiplied by the non-inverting gains RMS summed with $v_{ni+(2)}$ ($v_{ni+(1)}$) multiplied by its inverting gain. Assuming all op amps have the same worst case noise voltages and currents, the output noise voltage, $V_{no(1)}$ of A1 will be:-

$$V_{no(1)} = \sqrt{\left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + \left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2}$$

Op amp A2 will have a similar output noise voltage. The third op amp A3 will multiply the noise voltages from A1 and A2 by its inverting gain. It will RMS sum these together with its own noise

voltage (which is multiplied by its own non-inverting gain), yielding a total output noise voltage, V_{not}, of:-

$$Vnot = \sqrt{2*\left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + 2*\left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2 + 2*v_{nri(3)}^2}$$

To maximise noise rejection, the gain of the first stage will normally be large while the gain of the last stage will be small (frequently, as here, unity to minimise any common-mode errors), and so reducing the effect of the final stage's noise. Using bipolar input op amps in the final stage will have a greater effect on the noise level due to their much larger noise currents. These larger noise currents place a compromise on the limit on the range of values for A3's source resistors, smaller source resistors generate less noise voltages, but load the input stage op amps' outputs introducing distortion.

With R_f=20kΩ, R_{sh}=200Ω, R_1=20kΩ, R_S=20kΩ the non-inverting gain of the input stage will be 101 and the inverting gain will be 100. These values coupled with the TLC2201B/2B's maximum noise voltage of 12nV/$\sqrt{Hz}$ (guaranteed at 1kHz) and noise current of 2.53fA/$\sqrt{Hz}$ (calculated for 1kHz) the following values are achieved.

For A1 and A2

V_{ni+} = 21.7nV/$\sqrt{Hz}$ V_{nri} = 21.8nV/$\sqrt{Hz}$

V_{no} = 3.10μV/$\sqrt{Hz}$

and for A3 V_{nri} = 21.7nV/$\sqrt{Hz}$

The resulting output noise voltage, V_{not}, spectral density for the TLC2201/2 instrumentation amplifier will be:-

V_{not} = 4.39μV/$\sqrt{Hz}$.

Referring this value to the input (dividing by the signal gain = 201) implies an input referred noise voltage of **21.8nV/$\sqrt{Hz}$**. This value is dominated by the thermal noise of the source resistor, with a low noise bipolar op amp the noise would be dominated by the noise current of the device. So when interfacing to high impedances the TLC2201/2 provides a very low noise and a highly accurate solution.

3.6. TLC2272/4 Dual and Quad Rail-to-Rail Op Amps

Most op amps will have been designed to work in either single rail or dual rail applications. This will normally limit the common-mode input range and the output voltage swing.

Bifet op amps have been designed for dual supply rails and hence their outputs cannot swing to either rail, while their inputs can only typically swing to the positive rail. High performance bipolar op amps have been designed for dual supply applications, and so will not normally allow their inputs or outputs to go to either rail. Most single supply op amps have had their inputs and outputs designed so that they can swing to ground. This is at the expense of their outputs being able to sink and source current.

To get over the problems of output swing the TLC2272 and TLC2274 use a push-pull output stage. The push-pull output stage enables the TLC2272/4 to swing within millivolts of both rails while

sinking and sourcing current. This capability enables the device to work in both single supply applications (operating in Class A) and dual supply applications (operating in Class AB). This is very important when providing signal conditioning for A-D converters, normal single supply op amps have their outputs clipped 1 V from the positive supply, which reduces the dynamic range of the A-D converter by 20%.

TLC2272/4 Dual and Quad Rail-Rail Op Amps

Specified for SINGLE and DUAL Suppy Operation!

- Output Swing Includes Both Supply Rails
- Common Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Errors
  ...VIO = 950 μV @ 25°C
  ...IIB = 1 pA @ 25°C
- LOW NOISE
  ...Vn = 9 nV/√Hz @ 25°C
  ...In = 2.8 fA/√Hz @ 25°C

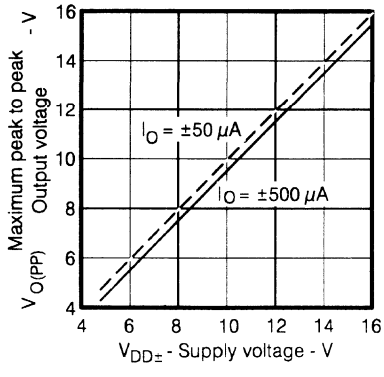


Figure 2.3.06. - TLC2272/4 Dual and Quad Rail-Rail Op Amps

The wide output swing and low input offset errors V_{IO} < 1 mV and I_{IB} = 1 pA (Typ), make it suitable for high impedance transducer interfacing. Its capability for use in these applications is enhanced by its low noise specification.

All these features give it one huge advantage over other general purpose CMOS amplifiers.

3.7. Measure Piezo A.C. Signals with Charge Amplifier

3.7.1. Piezo Transducer Interfaces

When interfacing op amps to piezo transducers, two basic modes are employed; Voltage mode or Charge mode. Both principles require an op amp with very high input impedance and low bias current, which limits the choice to JFET or CMOS input op amps. The dynamic range of such interfaces to

piezo transducers that exhibits ac signals is usually limited by the noise produced by the op amp. The TLC2201 and TLC2272 are Advanced LinCMOS op amps that challenge the input noise of the very best JFET input op amps and are simultaneously capable of operation from low supply voltages.

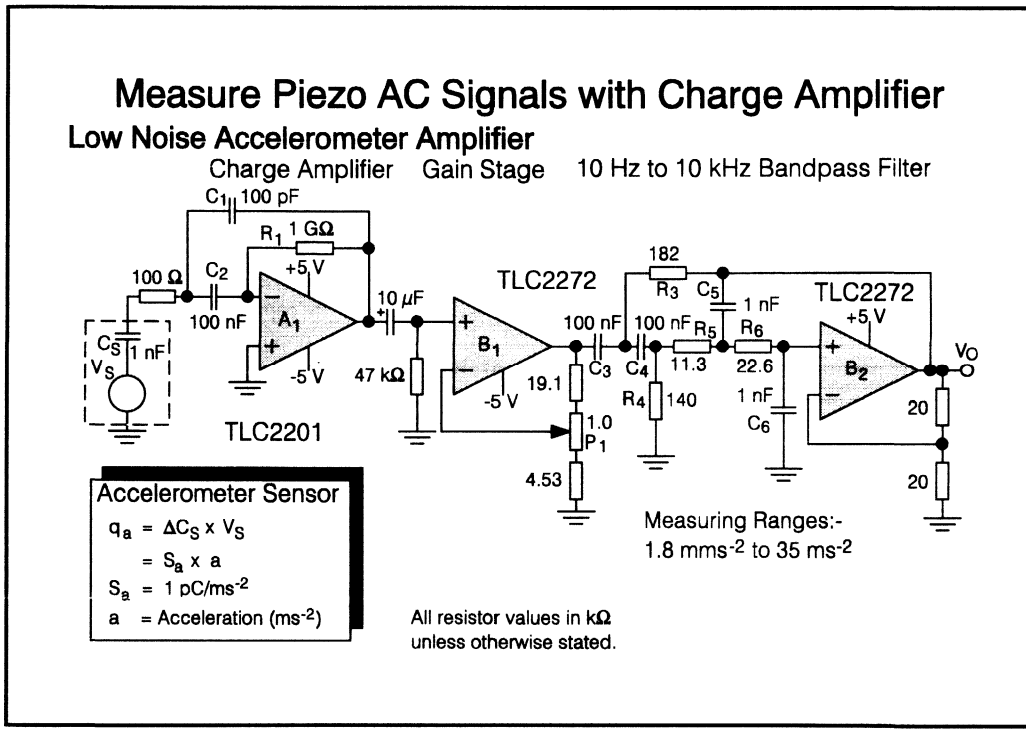


Figure 2.3.07. - Measure Piezo AC Signals with Charge Amplifier

Voltage mode operation requires that the op amp is placed very close to the sensor as parasitic load capacitance on the sensor output will change its sensitivity. A cable between the sensor and the op amp will not only attenuate the sensor's output - but variations in the cable capacitance due to mechanical influence easily modulates the desired signal. When voltage mode configuration is used, the amplifier is usually encapsulated together with the sensor such as in electric microphones.

Charge mode operation is widely used, primarily because the influence from any shunt capacitance across the sensor is eliminated. Consequently, the length of a connected cable will not influence the sensitivity but affect only the maximum bandwidth of the measuring system.

3.7.2. Accelerometer Application

The illustrated application converts an acceleration input, a, measured by a piezo electric acceleration sensor and conditioned by an accelerometer amplifier, to an output voltage, V_{out}, proportional with the sensed acceleration. The circuit provides a wide dynamic range thanks to the very low input noise and

rail-to-rail output swing of the Advanced LinCMOS op amps, TLC2201 and TLC2272 used. Additionally, the entire circuit operates from ±5V supplies, ensuring overall low power consumption.

The accelerometer amplifier consist of three sections, a charge amplifier that converts the sensor output charge to a voltage, a gain stage and a 10Hz to 10kHz bandpass filter, which limits the amplifier's noise bandwidth.

If an accelerometer sensor with a sensitivity of $1pC/ms^{-2}$ is employed, a maximum full scale rms acceleration of $35ms^{-2}$, or approximately 36g can be measured. The lowest acceleration that can be detected is determined by the charge amplifier's noise. Assuming typical system noise with a minimum of 5dB S/N ratio, vibration or acceleration levels down to $1.7mms^{-2}$ corresponding to 0.17mg are theoretical measurable.

Sensor

The equivalent electrical model of a piezo electric acceleration sensor can be thought of as a voltage source, V_S, in series with a small sensor capacitor, C_S. Variations in capacitance due to physical deformation will cause charge, q_a, to be dumped into the charge amplifiers summing junction. Characteristic parameters for such a sensor are the sensitivity, S_a, and the sensor capacitance, C_S.Their relationship to the produced charge, q_a, is given by:

$$q_a = \Delta C_S * V_S = S_a * a \; ; \quad \text{where a = acceleration ;}$$

The sensor (B&K type 4384) used in this application has the following typical parameter values: $S_a = 1pC/ms^{-2}$ and $C_S = 1nF$.

Charge Amplifier

The purpose of the charge amplifier is to transform the high output impedance of the acceleration sensor and amplify its relatively weak signal. A basic charge amplifier consists of a high gain operational amplifier with a feedback capacitor. When charge is dumped into the amplifier's summing junction from the sensor, the amplifier manipulates its output voltage to maintain the charge in the feedback capacitor equal to the charge dumped into the input, so that the voltage in the summing junction tends to be at null. For the actual application, A_1 is acting as charge amplifier and C_1 is the feedback capacitor. Ignoring the effect from R_1, C_2 and the 100Ω input resistor, the transfer function from acceleration input to A_1's output voltage, E_{o1} becomes:

$$E_{o1} = -\frac{q_a}{C_1} = -\frac{S_a}{C_1} * a \quad <=> \quad \frac{E_{o1}}{a} = -\frac{S_a}{C_1} ; \quad (1)$$

By insertion of actual component and parameter values, (1) becomes:

$$\frac{E_{o1}}{a} = -\frac{1pC/ms^{-2}}{100pF} = -10mV/ms^{-2} ; \quad (2)$$

If higher vibration or acceleration levels than 36g have to be measured, C_1 can be increased to reduce the gain of the charge amplifier.

A large feedback resistor, R_1, provides a leakage path for A_1's input bias current and prevents the op amp's output from being driven into saturation. As R_1 together with C_1 forms a highpass filter with a 3 dB frequency, $f_O = 1/(2\pi R_1 C_1) = 1.59$ Hz; the value of R_1 needs to be vary large if low frequencies are of interest. The exceptional large value of 1 GΩ is chosen because the effect of its thermal noise decreases as R_1 increases. This is discussed in the noise evaluation section. An upper limit of R_1 is

given by the offset produced when A_1's input bias current passes through it. With TLC2201's 100 pA maximum input bias current over temperature, a worst case offset of (1GΩ * 100 pA) = 100 mV is generated. However, as the maximum signal output from A_1 is only 500mV peak, no limitations on the op amp's output swing follows. To prevent swing limitations on the succeeding gain stage, the charge amplifier's output is ac coupled.

To avoid A_1's input bias current from contributing to the charging of C_1, a dc blocking capacitor C_2 is placed between the very high impedance ac summing junction and the op amp's inverting input terminal. The effect of C_2 on the transfer function can be ignored with the value chosen. A 100Ω resistor in series with the charge amplifier's input provides some protection, when the sensor is disconnected. A lowpass filter is formed together with C_1 but at frequencies beyond interest. Thermal noise from 100Ω will not affect the overall accelerometer amplifier's noise performance.

Charge amplifiers very high input impedance require carefully layout, PCB cleaning and guarding. The summing junction would benefit from Teflon stands. Both capacitors should be of a low leakage type such as polypropylene, polystyrene or Teflon.

3.7.3. Gain Stage

A simple non-inverting gain stage is implemented by one half of a low noise TLC2272 op amp to boost the charge amplifier's output voltage five fold. Additionally, the gain stage around A_2 allows for ±10% gain adjustment with P_1 to accommodate variations in the sensitivity of the sensor. The gain should be adjusted to yield an overall accelerometer amplifier output voltage, V_{out}, of 100 mV/ms^{-2}. Thermal noise from the potential voltage divider, does not contribute to the total system noise.

TLC2272's output stage features rail-to-rail output swing with the load impedance provided.

Filter

Following the gain stage is a 10 Hz to 10 kHz bandpass filter, implemented around the second half of TLC2272. The purpose of this filter is to remove low frequency excess noise and limit the upper noise bandwidth. In fact, the bandpass filter consists of a combined 2nd order 10 Hz highpass and 2nd order 10 kHz lowpass filters with Butterworth characteristics. Design of this filter section assumes no mutual interaction between the two filter sections. This is only possible because the cut off frequencies are so far apart and that an impedance level has be chosen to minimise interaction.

Design details of the filter are trivial and only covered briefly. Assumptions: $\omega_{OHP} = 1/(2\pi * 10\ Hz)$, $\omega_{OLP} = 1/(2\pi * 10\ kHz)$, a midband gain of two and a 2nd order maximum flat or Butterworth Q factor, $Q = 1/\sqrt{2}$. The transfer function, H(s), can then be shown to be given by:

$$H(s) = \frac{s^2}{s^2 + \left(\frac{1}{R_4C_3} + \frac{1}{R_4C_4} - \frac{1}{R_3C_3}\right)s + \frac{1}{R_3R_4C_3C_4}} * \frac{\frac{1}{R_5R_6C_5C_6}}{s^2 + \left(\frac{1}{R_5C_5} + \frac{1}{R_6C_5} - \frac{1}{R_6C_6}\right)s + \frac{1}{R_5R_6C_5C_6}} \quad \text{..... (3)}$$

$$H(s) = \frac{s^2}{s^2 + \frac{\omega_{OHP}}{Q}s + \omega_{OHP}^2} * \frac{\omega_{OLP}^2}{s^2 + \frac{\omega_{OLP}}{Q}s + \omega_{OLP}^2} \quad \text{..... (4)}$$

Comparing (3) and (4) yield the following design equations and component values:

Highpass: Choose $C_3 = C_4 = C = 100\ nF$;

$$R_3 = \frac{\frac{1}{Q} + \sqrt{\frac{1}{Q^2} + 8}}{4\omega_{oHP}C} = 182.1k\Omega \cong 182k\Omega \text{ (E96 value)} ;$$

$$R_4 = \frac{4}{\omega_{oHP}C} \frac{1}{\sqrt{\frac{1}{Q^2} + 8} + \frac{1}{Q}} = 139.1k\Omega \cong 140k\Omega \text{ (E96 value)} ;$$

Lowpass: Choose $C_5 = C_6 = C = 1nF$;

$$R_6 = \frac{1}{Q\,\omega_{oLP}C} = 22.51k\Omega \cong 22.6k\Omega \text{ (E96 value)}$$

$$R_5 = \frac{1}{R_6C^2\omega_{oLP}^2} = 11.25k\Omega \cong 11.3k\Omega \text{ (E96 value)} ;$$

3.7.4. Why use Advanced LinCMOS TLC2201 and TLC2272 Op Amps?

The charge amplifier requires a CMOS or JFET input op amp with very low input voltage and noise current. In addition, the input bias current should be as low as possible to avoid excess offset that limits the dynamic range.

For the gain stage and filter section, a relatively low voltage and current input noise is still required. But more important is the low distortion rail-to-rail output swing providing output voltage levels, that easily interface to a connected sample & hold plus a/d converter circuitry.

If these essential needs are added to the demand for low cost, low power and low supply operation (±5V), the TLC2201 and TLC2272 are about the only op amps available meeting these requirements. For even higher performance the TLC2272 could be replaced by the TLC2202.

3.7.5. Noise Considerations

If a multi-stage amplifier is constructed such, that the input noise of the first stage multiplied with its gain is larger that the input noise of the succeeding stage etc., the first stage will dominate the noise of

the total multi-stage amplifier. Following this principle, the charge amplifier's gain has been chosen to produce an output noise, E_n, significantly higher than the input noise of the gain stage. Consequently, the noise evaluation is focused on the noise produced by the charge amplifier in the bandwidth limited by the filter section. Wideband noise generated by A_3, (which is only limited by its falling open loop gain), is low and can be ignored.

Three sources dominates the output noise from the charge amplifier:

- $\mathbf{e_n}$, input noise voltage density from A_1, TLC2201; (e_n = 8 nV/$\sqrt{Hz}$ typical)
- $\mathbf{I_n}$, input noise current density from A_1, TLC2201 ; (i_n = 0.6 fA/$\sqrt{Hz}$)
- $\mathbf{R_1}$, thermal noise density generated by R_1 (1 GΩ), and equal to $\sqrt{4kTR_1}$;

Where k = 1.38 * 10^{-23} J/K (Boltzmann's constant; and T = 298 K (absolute temperature @ 25°C).

Assuming that the charge amplifier's input is shorted by the sensor's characteristic capacitance, C_S, and that C_2 and the 100 Ω input resistor does not influence the noise, the charge amplifiers output noise density, $E_n(s)$, is given by:

$$E_n^2(s) = \left(1 + \frac{R_1 \parallel \frac{1}{C_1 s}}{\frac{1}{C_S s}}\right)^2 * \left(e_n^2 + i_n^2\left(R_1 \parallel \frac{1}{C_1 s} \parallel \frac{1}{C_S s}\right)^2 + 4kTR_1\left(\frac{\frac{1}{C_1 s} \parallel \frac{1}{C_S s}}{R_1 + \frac{1}{C_1 s} \parallel \frac{1}{C_S s}}\right)^2\right);$$

$$E_n^2(s) = e_n^2\left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1\, s + 1}\right)^2 + i_n^2 R_1^2\left(\frac{1}{R_1 C_1\, s + 1}\right)^2 + 4kT\, R_1\left(\frac{1}{R_1 C_1\, s + 1}\right)^2$$

The total rms noise measured on the charge amplifiers output can now be calculated from:

$$E_n(rms) = \sqrt{\int_{-oo}^{+oo} |E_n(j2\pi f)|^2 d(f)}\ ; \qquad s = j\omega = j2\pi f$$

To simplify this task, we will analyse the three components of $E_n^2(s)$, and determine which dominate in the frequency band of interest.

$$E_n^2(s) = E_{e_n}^2(s) + E_{i_n}^2(s) + E_{R_1}^2(s)\ ; \quad s = j\omega = j2\pi f \quad \Rightarrow$$

$$|E_n(j2\pi f)|^2 = |E_{e_n}(j2\pi f)|^2 + |E_{i_n}(j2\pi f)|^2 + |E_{R_1}(j2\pi f)|^2\ ;$$

e_n generated noise: $$E_{e_n}(s) = e_n\left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1\, s + 1}\right);$$

$$|E_{e_n}(j2\pi f)| = e_n \sqrt{\frac{1 + \left(\frac{f}{f_{zero}}\right)^2}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Zero frequency: $f_{zero} = \frac{1}{2\pi R_1 (C_1 + C_S)} = 0.14\text{Hz}$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59\text{Hz}$

Noise; $f << f_{zero}$: $e_n = 8\text{nV}/\sqrt{\text{Hz}}$ (typical)

Noise; $f >> f_{pole}$: $e_n\left(1 + \frac{C_S}{C_1}\right) = 88\text{nV}/\sqrt{\text{Hz}}$ (typical)

i_n generated noise: $E_{e_i}(s) = i_n R_1 \left(\frac{1}{R_1 C_1 s + 1}\right)$;

$$|E_{e_i}(j2\pi f)| = i_n R_1 \sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59\text{Hz}$

Noise; $f << f_{pole}$: $i_n R_1 = 600\text{nV}/\sqrt{\text{Hz}}$ (typical)

R_1 generated noise: $E_{R_1}(s) = \sqrt{4kT R_1}\left(\frac{1}{R_1 C_1 s + 1}\right)$;

$$|E_{R_1}(j2\pi f)| = \sqrt{4kT R_1} \sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59\text{Hz}$;

Noise; $f << f_{pole}$: $\sqrt{4kTR_1} = 4.1\mu\text{V}/\sqrt{\text{Hz}}$;

Clearly, the current and thermal generated noise dominates at very low frequencies. The amplitude of the current generated noise, $|E_{i_n}(j2\pi f)|$, is reduced by -20dB/decade above f_{pole}. Consequently, it has shrunken to the same level as the amplitude of the voltage generated noise, $|E_{e_n}(j2\pi f)|$, at:

$$\frac{i_n R_1}{e_n \frac{C_1 + C_s}{C_1}} \frac{1}{2\pi R_1 C_1} = \frac{i_n}{2\pi e_n (C_1 + C_s)} = \frac{600nV}{88nV} * 1.59Hz = 10.8Hz ;$$

Current generated noise has therefore no effect on the total noise in the 10Hz to 10KHz frequency band at 25°C. Note that the 10.8Hz frequency remains constant with changes in R_1.

Similarly, the amplitude of the thermal generated noise, $|E_{R_1}(j2\pi f)|$, equals the amplitude of the voltage generated noise, $|E_{en}(j2\pi f)|$, at:

$$\frac{\sqrt{4kTR_1}}{e_n \frac{C_1 + C_s}{C_1}} \frac{1}{2\pi R_1 C_1} = \sqrt{\frac{4kT}{R_1}} \frac{1}{2\pi e_n (C_1 + C_s)} = \frac{4.1\mu V}{88nV} * 1.59Hz = 74Hz ;$$

Consequently, thermal generated noise as well as current generated noise has little or insignificant effect on the total noise in the 10Hz to 10kHz frequency band. Note that the 74Hz frequency decreases proportionally with increasing value of $\sqrt{R_1}$. The interesting point about R_1 is, that the current generated noise in the frequency range considered is unaffected and that a higher value reduces the thermal noise!

The conducted noise analysis clearly shows, that the charge amplifier's output noise density in the frequency range of interest is totally dominated by the noise voltage, $|E_{en}(j2\pi f)|$, generated by the TLC2201 op amp's input noise voltage, e_n. Calculating the total rms noise, $|E_n(rms)|$, on the output of the charge amplifier now becomes a simple task, as $|E_{en}(j2\pi f)|$ is constant from 10Hz to 10kHz. Integration of the noise density over the frequency band of interest can now be accomplished with a simple multiplication, yielding:

$$|E_n(rms)| = \sqrt{|E'_{e_n}(j2\pi f)|^2 * \text{Noise Bandwidth}} ;$$

Where $|E'_{e_n}(j2\pi f)|$ is equal to $|E_{e_n}(j2\pi f)|$ for $10Hz < f < 10kHz$. Inserting numbers gives:

$$|E_n(rms)| = \sqrt{|88nV/\sqrt{Hz}|^2 * (10kHz - 10Hz) * 1.11} = 9.27\mu V \text{ rms};$$

Re-arranging the transfer function (1) for the charge amplifier can now be used to determine the corresponding input accelerations, a_n:

$$a_n = \frac{E_n(rms)}{S_a} C_1 = \frac{9.27\mu V}{1pC/ms^{-2}} 100pF = 0.927mms^{-2} ;$$

Assuming a minimum 5dB S/N ratio, the typical lowest theoretical acceleration, a_{min} that can be measured is given by:

$$a_{min} = a_n * 10^{SNR_{dB}/20} = 0.927\ mms^{-2} * 10^{5/20} = 1.65mms^{-2} \cong 0.17mg \text{ acceleration} ;$$

However, these figures are reduced somewhat if a worst case calculation is performed. The major additional noise comes from:

- Worst case TLC2201A noise voltage is 50% higher and equal to 12nV/$\sqrt{Hz}$, which raises the flat noise floor.
- Worst case TLC2201 noise current over temperature is much higher than the typical 0.6fA @ 25°C, as it tends to double for every 10°C temperature increase. This temperature dependent effect results in an increasing low frequency noise with increasing temperature.
- Thermal noise from the feedback resistor increases with the square root of the temperature again adding to the low frequency noise.
- Noise sources from the succeeding gain op amp and filter contribute slightly to the total noise with the component values and gain chosen.

3.8. TLE2037 and TLE2237 - High Speed Op Amps

The TLE2037 and TLE2237 are among the most recent op amps to be developed and fabricated using the Excalibur technology. These devices have been optimised for precision and high speed performance. They include a novel output stage that features a 'Saturation Recovery Circuit' which enables much improved small signal response and outstanding levels of distortion.

Precision - The parameters of most importance in a precision application are; Offset Voltage, Drift, Bias Currents and Open Loop Gain. The TLE2037A, single op amp, has a maximum offset voltage of only **25µV** and a maximum offset voltage drift of **1µV/°C and 1µV/month**. While the TLE22237, dual op amp) has an offset voltage of 100 µV, with similar offset voltage drifts to that of the TLE2037.. Both devices have bias current cancellation circuitry to reduce bias currents to typically 15 nA enabling larger external resistors without impacting overall dc accuracy.

An outstanding parameter of both devices is their open loop gain, **Avd; - at 153dB**, it is probably the **highest in the world!** The resulting improvement in the op amps circuits 'loop-gain' causes an increase in overall performance - everything from offset voltage, input impedance and distortion are improved.

AC Performance - The TLE2037 and TLE2237 are decompensated versions of the TLE2027 and TLE2237 respectively. Both should be used with a minimum closed loop gain, Acl, of 5, but the gain bandwidth product for the **TLE2037** is **76 MHz** and **50 MHz** for the **TLE2237**, (compared with **15MHz** and for the TLE2027). Slew Rates for the **TLE2037** and **TLE2237** are **7.5 V/µs** and **5 V/µs** respectively.

Low Distortion - Linked to an increase in ac performance both devices feature a **Saturation Recovery Circuit** which improves the small signal response and enables the device to be used at much higher frequencies with increased output swings - see figure 2.3.09 A further advantage is the extremely low levels of distortion even when driving loads as low as **600Ω,** (see figure 2.3.10) which has enabled the device to be used in low noise applications such as Audio systems.

Low Noise - A large input stage, and clever design and layout techniques has given the device an extremely low noise voltage specification - **3.3nV/$\sqrt{Hz}$ at 10Hz**, and **2.5nV/$\sqrt{Hz}$ at 1kHz.** This is an obvious further benefit to precision measurement systems and audio applications.

Applications - The excellent ac performance and low noise makes the devices ideally suited to Audio and Telecom applications, whilst the low offsets and excellent overall precision has enabled the parts to be used in Instrumentation, Measurement and Test equipment.

TLE2037 and TLE2237 - High Speed Op Amps

Low Noise, High Speed and Precision

- Low Noise Voltage;
  3.3 nV/√Hz @ 10 Hz
  2.5 nV/√Hz @ 1 kHz
- Wide Bandwidth;
  TLE2037 ..... 76 MHz
  TLE2237 ..... 50 MHz
- Low Input Offset Voltage;
  TLE2037A ..... 25 μV max
  TLE2237 ..... 100 μV
- High Open Loop Gain
  45 V/μV or 153 dB!!!
- Output Features Low Distortion and Saturation Recovery

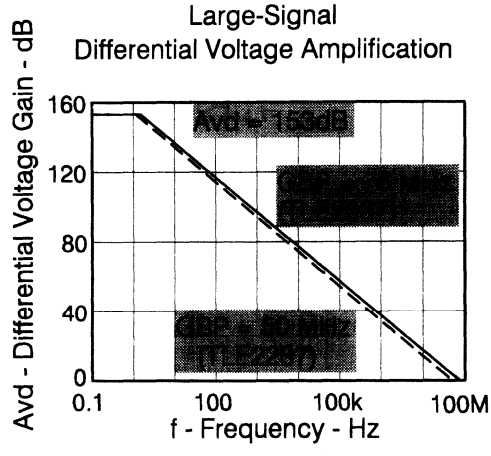


Figure 2.3.08. - TLE2037 and TLE2237 - High Speed Op Amps

3.9. Distortion Measurements

Figure 2.3.09 compares the 'Total Harmonic Distortion + Noise' of 3 different op amps, over frequency, whilst driving 100 kΩ and 600 Ω loads.

The three amplifiers highlighted in the graphs (the NE5534, OP37 and TLE2037) are all bipolar designs and have been chosen because of their specified low levels of noise and distortion. These graphs highlight the superior performance of the TLE2037 Excalibur op amp.

The THD of an amplifier is dependent upon many parameters, specifically the open loop gain, bandwidth, slew rate, load and the input signal magnitude. The circuit used to compare these three amplifiers emphasises many of these points. A non-inverting gain of 40dB has been chosen to highlight the importance of the loop-gain of the op amp. To ensure that noise does not conceal the THD of the op amps a 22kHz noise filter has been introduced - this explains the shape of all curves at high frequencies. This frequency is, however, wide enough to highlight any problems due to slew rate limiting.

Loop gain, Aβ, (approximately the difference between the open loop and closed loop gain curves) is a crucial factor in low distortion circuits. This, combined with the obviously low levels of noise for

bipolar op amps, explains why CMOS or Bifet designs suffer from relatively poor distortion compared to bipolar. The TLE2037 has a typical open loop gain of 153dB (45 million!) and so distortion is significantly reduced. Slew rate is another crucial factor in low distortion circuits as at high frequencies and high gains an op amp may not be capable of operating without clipping or distorting the output signal.

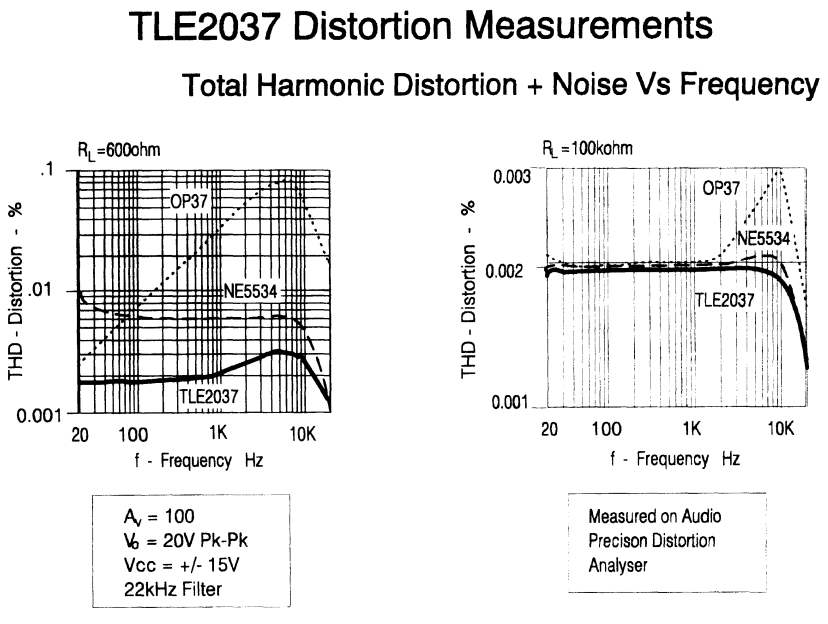


Figure 2.3.09. - TLE2037 Distortion Measurements

The second graph, examines how a load affects an op amps distortion. The impedance used in these measurements is 600 Ω and it shows that the OP-37 device is really not suited for applications with loads as heavy as this. What the graph does highlight is the outstanding performance the TLE2037, it has significantly better distortion than its competitor, the OP-37 and also outshines the NE5534.

The TLE2037 is therefore an ideal op amp in applications driving high impedance nodes and can be used for driving cables as well as multiple paralleled loads. The overall low distortion of this part also makes it particularly useful in audio applications including microphone pre-amps, filters and equalisation circuits.

3.10. Saturation Recovery

In conventional OP-27 type amplifiers the output voltage remains predictable only if it stays within the V_{om} (maximum Vout) specification. If an input signal is applied which tries to force the output voltage beyond the V_{om} limit, the output may not respond correctly to subsequent input signals until after a given amount of time has passed. This time is the "Output Saturation Recovery Time".

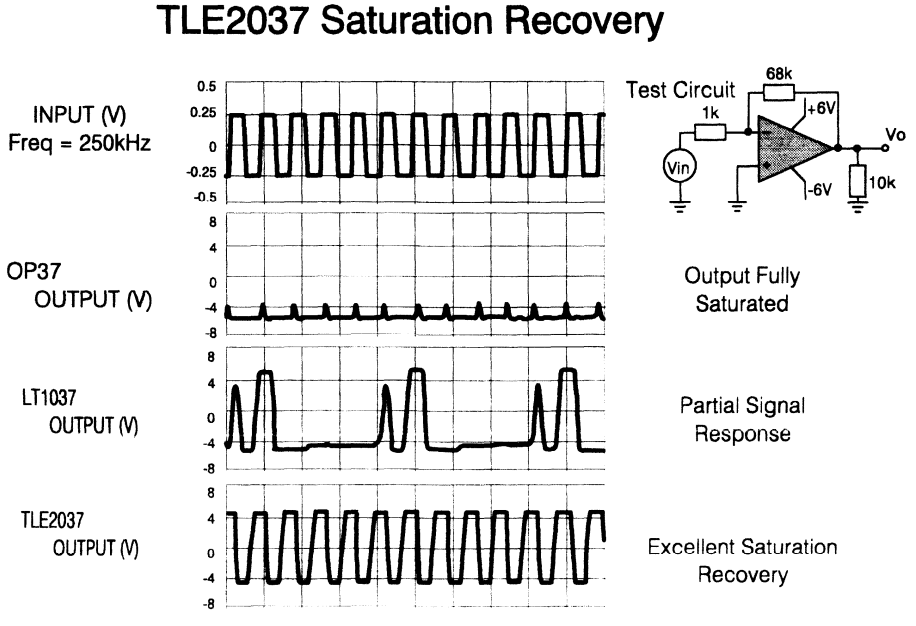


Figure 2.3.10. - TLE2037 Saturation Recovery

There are three things that can cause the OP-27 type amplifiers to exhibit output saturation recovery problems. First, in some of the amplifiers, the final common emitter gain stage is allowed to be driven heavily into saturation. the excess base charge built up on the device can only be removed via a high value pull down resistor. Therefore a finite time must pass before enough charge is removed to assume normal operation.

Secondly, the current sources in the class AB output stage are also allowed to saturate. These are not driven as heavily into saturation, but they still take a finite amount of time to recover.

Thirdly, and perhaps most importantly, the bias generator for the entire circuit can be disturbed from its equilibrium point when the output stage current sources saturate. If disturbed enough, the bias circuit can shut off completely until the start-up circuit engages. If this happens the entire circuit loses power

and the output signals will not become valid again until the bias generator recovers from its equilibrium point. This results in a huge output saturation recovery time.

In the TLE2027/37 and TLE2227/37 devices, special circuitry has been added to keep the final gain stage and the output stage current sources out of saturation. Therefore, no saturation recovery time is needed enabling the devices to continue to operate in their normal, stable and predictable manner.

3.11. High Performance Low Noise Pre-Amp

A system requiring the ultimate in ac performance is audio hi-fi, CD Players, with a dynamic range exceeding 90 dB, are pushing the performance of amplifiers to new levels.

Phonographic recording/replay is still the standard for many good hi-fi and they require the ultimate in high performance amplifiers. The TLE2037 with an open-loop gain of 153 dB, an offset of 25 μV and an 80 MHz gain-bandwidth product of 76 MHz is an excellent choice in audio applications. The low distortion and excellent output saturation recovery, discussed earlier, endorse the TLE2037s audio capabilities.

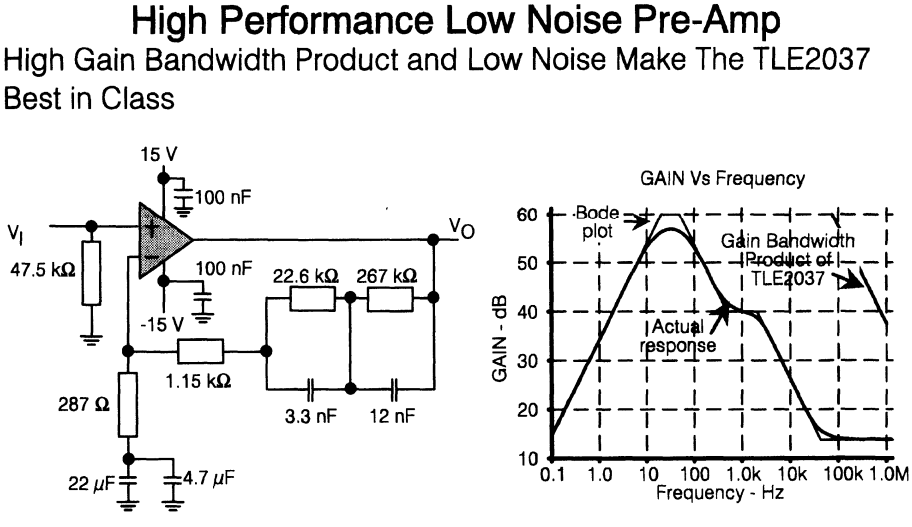


Figure 2.3.11. - High Performance Low Noise Pre-Amp

Record equalisation circuits illustrate the importance of high gain and wide bandwidth in an ac application. The RIAA specification defines the characteristic of the phono replay pre-amplifier, and

takes into account, the frequency response of magnetic pick-ups. The pre-amp must match and cancel out the pick-ups response. The result is roll-offs at 50 Hz and 2120 Hz with a zero at 500 Hz. The circuit incorporates a low frequency pole and a corresponding zero at 20 Hz to remove rumble and low frequency effects.

For a gain of 1000, the op amp needs a large gain-bandwidth product to remove any gain error. The chosen op amp, TLE2037, has a loop-gain in excess of 40 dB at 20 kHz. Equally as important to low distortion is the device's 100 kHz full power bandwidth.

To achieve these levels the op amp has been decompensated. This means, as described in section 3.7 of signal conditioning, that the compensation capacitor has been reduced to allow faster slew rates and higher bandwidth. However, the decompensated op amp should only be used with closed loop gains of greater than 5, preserving the $A\beta$ phase margin. Therefore, the high frequency gain of the circuit has been designed to flatten out with a gain of 5. This is done by introducing a zero at 40 kHz.

The types of components used must also be considered. The circuit has been purposely configured so as not to require the use of noisy, low performance electrolytic capacitors.

Polypropylene capacitors with their very low tan δ, give very good performance and have been used throughout, except for the lowest frequency zero where polycarbonate capacitors have been used.

The resistors used are all metal film, giving high precision and low flicker noise. They are readily available in E96 series values and hence provide a cheap and accurate solution to the pre-amp's requirements.

3.12. High Speed Single Ended to Differential Converter

Differential lines are quite frequently used in professional audio systems. The differential signal will often be used to drive the output stage increasing the available output power when using class AB output stages. However most transducers and pre-amps will only produce single ended signals (they will, however, be stereo; left and right).

So in order to produce the differential signal a high performance single ended to differential converter is required. This converter can also be used to introduce gain into the system.

A single ended-input, differential-output converter can be constructed by parallel coupling of two differential input amplifiers, and a high speed buffer amplifier. However, the single ended-input, differential-output converter shown in figure 2.3.12 is more than just two cross coupled differential input amplifiers - the circuits unique configuration is widely used in professional audio applications. The cross coupled feedback approach ensures that the output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 20dB, This enables the converter to be set for inverting, non-inverting or differential operation. The configuration even allows the device to drive unbalanced load, like a true transformer.

3.12.1. TLE2237 and TLE2027 Op Amps

Similar circuits can be implemented with several different amplifiers, all of which must be capable of driving low impedance loads over the speech or audio frequency range. However if low distortion is to be maintained a large loop-gain must be maintained over the required bandwidth.

Normal unity-gain stable op amps have their bandwidth reduced to ensure stability at unity gain. However if the application requires some gain adding to the system, the true speed of the op amp has been wasted. This where de-compensated op amps come into their element. The TLE2237 is not unity gain stable, but is stable (with a healthy phase margin) for gains greater than 5 and this provides it with a factor of 4 improvement over the TLE2227. An even greater improvement can be attained with using two TLE2037s in place of the TLE2237.

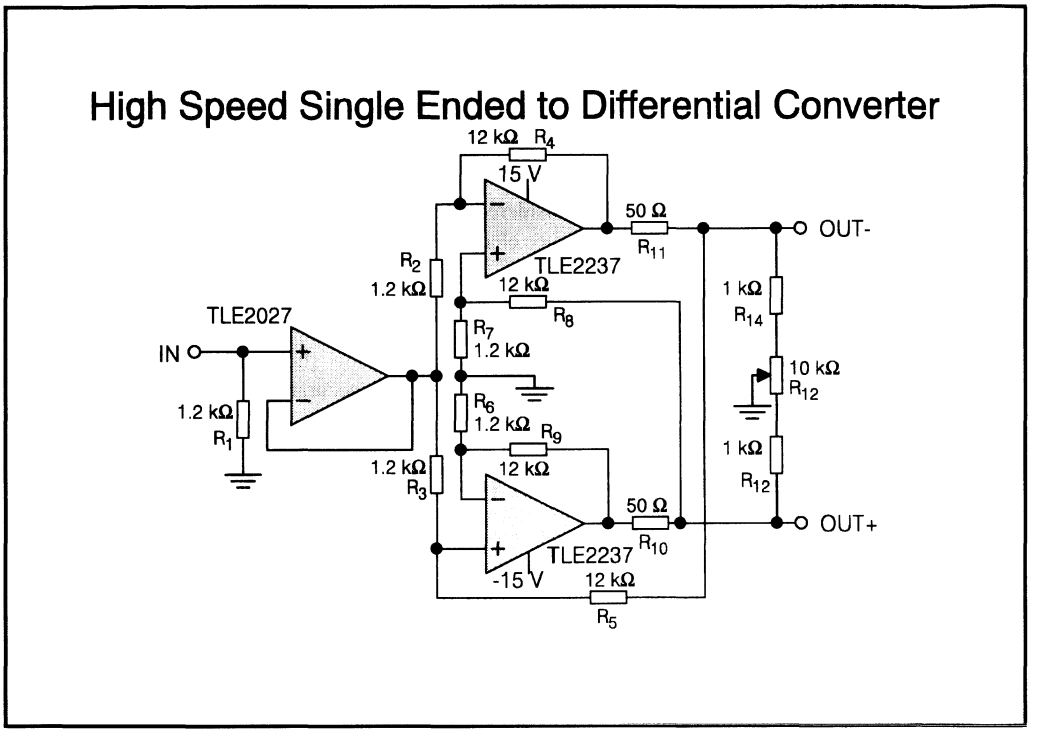


Figure 2.3.12. - High Speed Single Ended to Differential Converter

In order maintain low distortion the excess loop-gain, over the required bandwidth, about the op amp must be kept above 100. The TLE2237, with its 50 MHz bandwidth, at a gain of 10 maintains this level of loop-gain up to 50 kHz, which is well above the audio frequency range. The TLE2227 would only be able to maintain this up to 13 kHz, which clearly shows the benefit of the TLE2237 when used with gains above 5.

The TLE2027 configured as a unity gain buffer keeps its loop-gain above 100 for frequencies up to 150 kHz.

3.12.2. Design Details

Ignoring the influence of R_{10}, R_{11}, R_{12}, $R_{13}$and R_{14} on the differential output voltage, V_{out} (assuming ideal op amps), the voltage transfer function of the circuit can be derived from:

$$V_{out+} = V_{IN}\frac{R_5}{R_3+R_5}\left(1+\frac{R_9}{R_6}\right)+V_{out-}\frac{R_3}{R_3+R_5}\left(1+\frac{R_9}{R_6}\right)$$

$$V_{out-} = -V_{IN}\frac{R_4}{R_2}+V_{out+}\frac{R_7}{R_7+R_8}\left(1+\frac{R_4}{R_2}\right)$$

$$V_{out+} - V_{out-} = V_{IN}\left(\frac{R_5}{R_3+R_5}\left(1+\frac{R_9}{R_6}\right)-\left(-\frac{R_4}{R_2}\right)\right)$$

$$+ V_{out-}\frac{R_3}{R_3+R_5}\left(1+\frac{R_9}{R_6}\right)-V_{out+}\frac{R_7}{R_7+R_8}\left(1+\frac{R_4}{R_2}\right) \quad \text{..... (1)}$$

Assuming $R_3 = R_6 = R_7 = R_2$ and $R_5 = R_8 = R_9 = R4$. Cross multiplying and cancelling out yields:-

$$V_{out+} - V_{out-} = 2V_{IN}\frac{R_4}{R_2}+(V_{out-}-V_{out+})$$

$$V_{out+} - V_{out-} = V_{IN}\frac{R_4}{R_2} = 10\ V_{IN} \quad \text{..... (2)}$$

If one of the differential outputs nodes - say V_{out-} is loaded heavily to ground by an unbalanced load or even shorted to ground, the opposite output amplifier senses the decrease in V_{out-}'s output voltage and compensates by boosting its own output, V_{out+}. The sense feedback ensures that the gain remains as given by (2).

In order to ensure that one output can drive the total output swing, when the other is shorted, the output swing under normal balanced load conditions must be held below half the maximum swing. With an input signal, $V_{in} = 2V_{pp}$, the output swing, $V_{out} = 20V_{pp}$. This level can easily be sustained by one op amp if the other 's output is shorted to ground.

3.13. TLE2082 Dual High Speed Bifet Op Amp

The latest member of Texas Instruments' vast family of Bifets is the TLE2082. This is a high speed, low noise dual Bifet. In common with all the most recent releases of Texas Instruments' Bifets the TLE2082 is constructed using the Excalibur technology.

Texas Instruments was one of the first semiconductor manufacturers to supply Bifets (Fairchild were the first with their 100 mV offset offering). One of Texas Instruments' great strengths in their Linear product range is its family of Bifets. In the mid-eighties, this was reinforced by the introduction of the TL030s and TL050s. The derivation of Excalibur Texas Instruments, has enabled to continue this long history in Bifet op amps with the TLE2060s, and now the TLE2080s.

The TLE2082 has been developed to meet the higher requirements of today's new applications. This covers audio applications as well as high speed control applications. The strength of all Bifets is their very high slew rate. The TLE2082 has taken this a stage further with its 10 MHz unity gain bandwidth

and large 40 V/μs slew rate. The specifications are further added to by its low noise voltage of 13.7 nV/√Hz making it ideal for high speed low noise transducer interface.

TLE2082 Dual High Speed Bifet

High Speed and Low Distortion

- HIGH-GAIN BANDWIDTH PRODUCT
  ..... 10 MHz
- HIGH UNITY GAIN SLEW RATE
  ..... 40 V/μs
- FAST SETTLING TIME ....400 ns to 10 mV
  10 V STEP ....1.5 μs to 1 mV
- LOW VOLTAGE NOISE
  ..... 13.7 nV/√Hz
  LOW CURRENT NOISE
  ..... 2.8 fA/√Hz

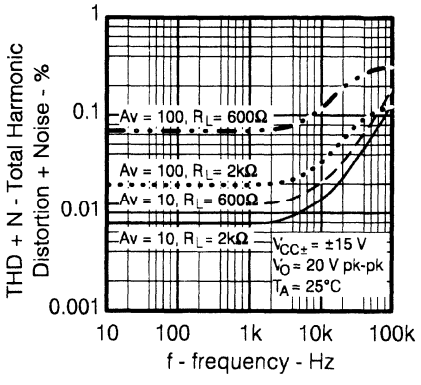


Figure 2.3.13. - TLE2082 Dual High Speed Bifet

The very low Total Harmonic Distortion (THD) figures make it ideal for audio applications, replacing the TL050s and TL070s which had become standard members in many high performance audio systems.

The low noise and high speed make the TLE2082 well suited to industrial control applications. The high slew rate is equally well matched by its very fast settling time. The TLE2082 takes just 400 ns to settle within 10 mV of its final state value for a 10 V, and just 1.5 μs to within 1 mV.

With audio and control applications in mind, the TLE2082 was designed to have a large output current drive capability, exceeding that of the TLE2060s and the TLE2037. This is realised in a minimum output current capability of ±30 mA, enabling the device to drive long cables, and even some heavy and demanding audio loads.

3.14. Fast Logarithmic Converter

The TLE2082 was designed for high speed applications which require high stability or high drive capability. Another application well suited to the TLE2082 is a Log Amplifier.

A log amplifier exploits the logarithmic dependence of V_{BE} on I_C, and produces an output voltage equal to the logarithm of the input voltage.

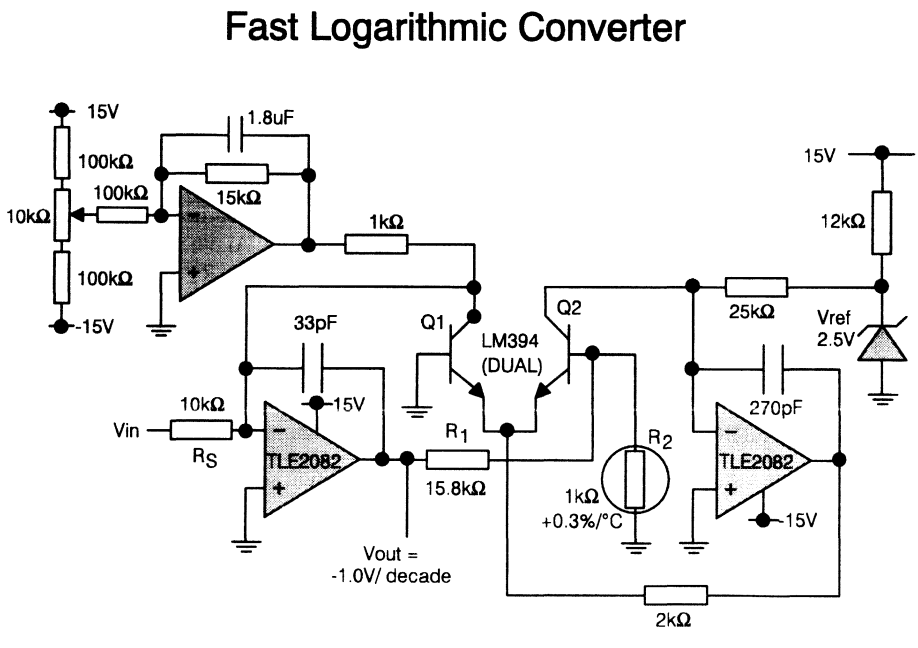
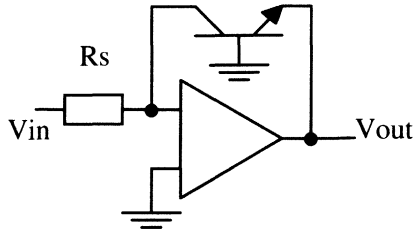


Figure 2.3.14. - Fast Logarithmic Converter



The basis of a log converter is an op amp configured as an inverter that has a NPN transistor as its feedback loop. This results in the input being converted into a current via the source resistor, R_S. The input current then flows through the transistor's collector causing the base-emitter voltage to change with the input voltage.

The base of the transistor is tied to ground so the output will be I base emitter voltage below ground.

Assuming the op amp has a virtual short between its inputs, the collector current will be:

$$I_C = \frac{V_{IN}}{R_s} \quad \text{.....Neglecting } I_{IB}$$

But $$IC = I_{SS}e^{\frac{qV_{BE}}{kT}} \quad \text{..... } V_O = -V_{BE}$$

This establishes the link between V_{IN} and V_O

$$V_O = -\frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\left(\frac{V_{IN}}{R_S I_{SS}}\right)$$

The logarithmic relationship between the output voltage and the input voltage can clearly be seen. The temperature effects can also be seen, first of all in the kT/q factor, but also in I_{SS}.I_{SS} has a negative co-efficient while kT/q has a positive co-efficient. These normally react to give V_{BE} its normal negative temperature co-efficient. This is where the subtleties of log amplifiers come into play.

Figure 2.3.14 shows one way of overcoming some of the temperature drift problems of the log amplifier. This is very similar to the fundamental log amplifier shown earlier except that two very accurately matched transistors are used, instead of just one transistor. Another difference is that the TLE2082 is driving the base of the second transistor (ignoring resistors R_1 and R_2), placing both transistors within the feedback loop. The output of op amp AI will be the base-emitter drop of Q2 minus the base-emitter drop of Q1, this fact will be exploited to reduce the temperature effects.

Once again, the input voltage will be converted into current by R_S, this current flows into the collector of Q1, causing its emitter to drop by 59 mV/decade of collector current. The emitter of Q2 is connected to the emitter Q1.

The LT1009 and the virtual earth of op amp A2 set up a fixed current source of 100 µA. This is used to bias Transistor Q2 setting up a constant V_{BE} (at any fixed temperature). Transistors Q1 and Q2 are part of highly matched transistor pair, which share the silicon and so should be at the same junction temperature. This also means that they should have the same I_{SS}.

The V_{BE1} of Q1 will be as follows:-

$$V_{BE1} = \frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\left(\frac{V_{IN}}{R_S I_{SS}}\right)$$

While V_{BE2} of Q2 will be:

$$V_{BE2} = \frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\frac{I_{C2}}{I_{SS}}$$

The voltage at the output of the TLE2082 is V_{BE2}-V_{BE1}, and so subtracting V_{BE1} from V_{BE2} gives:-

$$V_{BE2}\text{-}V_{BE1} = \frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\frac{I_{C2}}{I_{SS}} - \frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\left(\frac{V_{IN}}{R_S I_{SS}}\right)$$

Factorising: $V_{BE2}\text{-}V_{BE1} = \frac{1}{\text{Log}e} * \frac{kT}{q} * \left\{ \text{Log}\frac{I_{C2}}{I_{SS}} - \text{Log}\left(\frac{V_{IN}}{R_S I_{SS}} \right) \right\}$

$= \frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\left(\frac{R_S I_{C2}}{V_{IN}} \right)$

Or $V_{BE2}\text{-}V_{BE1} = -\frac{1}{\text{Log}e} * \frac{kT}{q} * \text{Log}\left(\frac{V_{IN}}{R_S I_{C2}} \right)$

By using two similar transistors, the effects of I_{SS} has been cancelled out, the effect of kT/q has not. The effect of it, however, can be cancelled by using a ptc (positive thermal co-efficient) resistor for R2.

At 25°C $V_{BE2}\text{-}V_{BE} = -0.059 * \frac{kT}{q} * \text{Log}\left(\frac{V_{IN}}{R_S I_{C2}} \right)$

Setting R_S = 10 kΩ and I_{C2} = 100 µA, $R_S * I_{C2}$ = 1 V. The output of op amp A1 would be V_{BE2} - V_{BE1}, but in order to achieve an output of 1 V per decade of input voltage, potential divider R_1 and R_2 is added. Placing the potential divider between the output and the base of the second transistor increases the gain and is also used to cancel out the temperature drift effects of kT/q, by R_2.

In order to achieve an output to input ratio of 1 V/decade, a potential divider of approximately 1/16.9 is required, this is best achieved by using a 15.8 kΩ resistor for R_1 and a 1.0 kΩ for R_2.

The PTC resistor must be a temperature measurement and control type, and not a temperature sensitive switching type. One suitable resistor is a Tel labs type Q81, which has a temperature co-efficient of +0.3%/°C.

Feedback capacitors must be included around the op amps to ensure stability, as for each op amp, the transistors are adding gain within their feedback loop. For added protection, a diode could be added across transistor Q1 to protect it from being destroyed should negative input be applied to the op amp's input.

The offset of the TLE2082 can be nulled out by an additional op amp, A3, which either adds/subtracts current to/from I_{C1}.

The TLE2082 is well suited to this application because of its very low noise, and its very low bias currents. The log amp can typically deal with currents varying from 1 nA to 10 mA, or over 7 decades. Amplifier A3 can be used to see the zero output voltage point. When dealing with the higher levels of current, it is important that op amp A1 should not go into current limit, the TLE2082 can supply more than 30 mA and so there is not any possibility of this occurring.

3.15. Precision Peak Detector

3.15.1. Basic Peak Detector

Peak detectors measure the maximum value of a fluctuating voltage. A basic peak detector consists of an ideal diode through which a capacitor is charged to a voltage equal to the peak input voltage. As long as the peak input voltage is higher than the stored voltage on the capacitor, the diode conducts and charges the capacitor. When the input voltage decreases, the diode turns off, and the maximum input

peak voltage is stored on the capacitor. To measure a new and lower peak value, the peak-hold circuit must be reset by a switch discharging the capacitor. If defined slopes of the peak detector are required, a resistor in series with the capacitor limits the charge current, and a bleed resistor across the capacitor ensures a defined discharge rate.

A near ideal diode with no voltage drop is implemented using a real diode in the feedback loop of an op amp. To avoid unwanted discharge of the capacitor from loading, this is normally buffered with an op amp with low input bias current.

3.15.2. Improved Peak Detector

The shown low droop precision positive peak detector uses a TLE2082A dual JFET-input op amp to achieve very low dc errors and good holding characteristics. A bootstrapped diode circuit prolongs the holding time. The reset circuit is provided with a simple 5V logic interface. With A_1 configured as a non-inverting follower peak detector, this circuit stores the input voltage's positive peak across C_3. A_2 buffers the output. Note that leakage of the buffer op amp input, charging diode J_1, discharging switch J_2, and storage capacitor C_3, are all potential problem areas when accurate peak voltage levels have to be stored for long time periods.

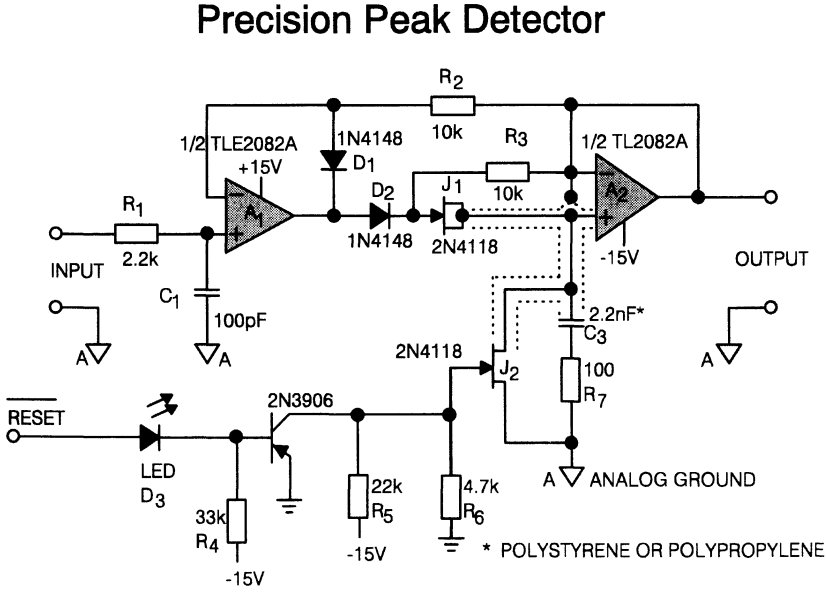


Figure 2.3.15. - Precision Peak Detector

3.15.3. Circuit Features

The actual circuit includes several features that minimise such leakage. J_1 is a low leakage 2N4118 n-channel JFET, that serves as a diode. Its small leakage is further reduced by minimising the voltage across it; i.e. C_3 charges through D_2 and J_1, but because R_3 provides J_1 with a bootstrapped version of C_3's voltage, only D_2 sees a reverse voltage, maintaining the voltage across J_1 at the millivolt level resulting from D_2's leakage current through R_3. As the discharge switch's leakage current also represents a main leakage path for C_3 an n-channel JFET device with a low leakage off-state and low on-state impedance is selected for J_2. The storage capacitor needs to be a low leakage type with a low dielectric absorption specification to prevent recovery errors in the stored voltage. Polystyrene, polypropylene or Teflon are the most suitable dielectrics for this application. The above features used to reduce the leakage of C_3 place the majority of the leakage to come from the buffer op amp's input bias current. TLE2082A has a max. input bias current of 200pA at 25°C. For a 2.2nF capacitor, this leakage level leads to a maximum output voltage decay error given by:

$$\frac{dV}{dt} = \frac{I_{leakage}}{C_3} = 91\ \mu V/ms$$

Because of the overall feedback loop, the circuit achieves a high dc accuracy. A_2's offset and drift errors are servoed out in the peak sample period but do appear in the peak-hold mode. E.g. A_1 determines the peak output offset error in the acquisition period and A_2 in the hold mode. Consequently, dc precision op amps are required for both A_1 and A_2. As a dual op amp is more likely to have a closer offset matching, the output error due to offset shift between the peak sample and peak hold mode is reduced. TLE2082A has a typical offset voltage of 650 µV 25°C.

3.15.4. Design Details

The circuit has an inherent potential to detect unwanted transient peaks, which simply lock out subsequent desired peaks. This characteristic justifies a low-pass filter formed by R_1 and C_1 to remove fast erroneous glitches on the input. The chosen time constant, R_1C_1 = 220ns should not have a major impact on the peak detector's speed. The rate of the voltage rise across C_3 is either,

1 $\frac{I_{max}}{C_3}$ (where I_{max} is A_1's short-circuit output current) or,

2 The slew rate of A_1,

whichever is smaller. With TLE2082A's 40mA typical short-circuit current and C_3 = 2.2nF a maximum voltage rise of,

$$\frac{40mA}{2.2nF} = 18.2\ V/\mu s$$

can be calculated. This is well below the op amp's specified 40 V/µs slew rate, and so the op amp's slew rate exceeds that set by the capacitor. A high value of C_3 minimises error due to parasitic leakage. Diode D_1 clamps the output voltage of A_1 to (V_{in} - V_{D1}) to improve speed and to limit the reverse bias voltage of D_2. If D_1 is conducting under negative input conditions, R_2 ensures that the voltage value held on the capacitor C_3 is still present on the output of the peak detector. To ensure correct and stable operation, the maximum input frequency should be much lower than,

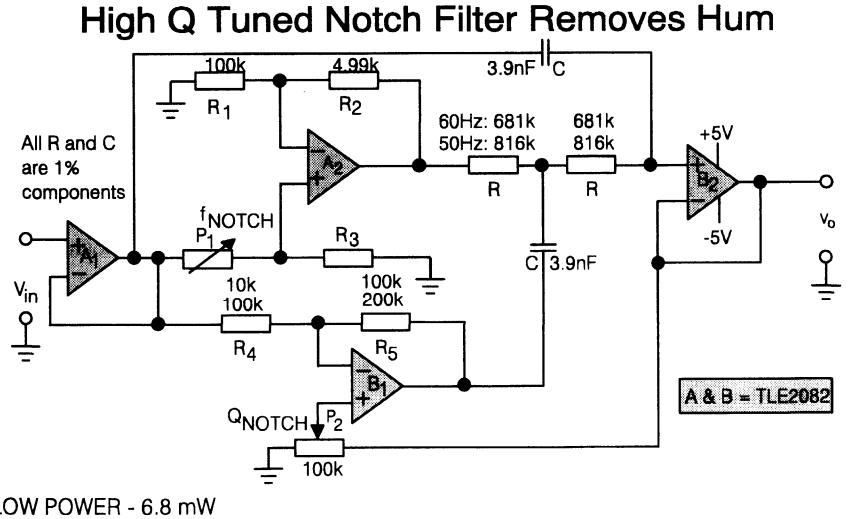
$$\frac{1}{2\,\pi\,R_3\,C_{D2}};$$

where C_{D2} is the shunt capacitance of D_2. If required, a capacitor can be placed across A_1 to optimise stability due to the load effect of C_3. Adjust this capacitor for minimum settling time. The circuit can be modified to capture negative peak values by reversing D_1, D_2 and substituting p-channel JFETs for J_1 and J_2. These alterations need, however, a modified reset circuit.

3.16. High Q Tuned Notch Filter Removes Hum

3.16.1. What is a Hum Notch Filter?

A frequent problem when measuring signals from sensors is the presence of 50 Hz or 60 Hz mains hum in the signal. In severe cases the interference can completely obliterate the signal of interest. When different signal conditioning amplifiers with high common mode rejection ratios fail to solve the problem or where they are not used, filter techniques are often employed.



- LOW POWER - 6.8 mW
- GOOD AC PERFORMANCE
- JFET INPUT - Allows High Inpedance Levels

Figure 2.3.16. - High Q Tuned Notch Filter Removes Hum

A Notch or Band-Stop filter in the signal path - tuned to the hum frequency - effectively reduces or eliminates 50Hz or 60Hz interference. Such a filter must have a linear phase response outside the notch

region to avoid distortion of the desired signal. This is particularly important where ac-signals, such as electrophysiological parameters are measured. The shown high-Q tuned active notch filter implementation uses two dual Excalibur Bifet op amps, the TLE2082, and has a minimum phase distortion.

3.16.2. Basic Hum Notch Filter

Traditional, simple band-stop filters using only a single op amp configured for a parallel-T Notch Filter have the following disadvantages:

1. Even accurate components, say 1%, still give a worst case variation in the notch frequency of a few percent. This variation from the ideal frequency, combined with a deep notch with high-Q, easily results in a filter which is not tuned for the right frequency at the deepest part of the notch. Ageing and temperature drift of filter components cause similar problems. If the notch frequency differs - say 2-3% from the theoretical value - due to component tolerances lower hum rejection can be expected. A maximum attenuation of 20-30 times compared with the desired signal can be achieved nearly independent of the chosen Q value for the notch filter.

2. Trimming of the filter's notch frequency to match the hum frequency is not a trivial task with a simple parallel-T active notch filter as the notch frequency and filter Q usually interact.

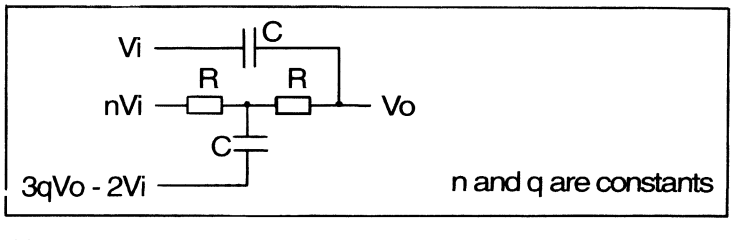
3.16.3. High-Q Tuned Hum Notch Filter

The shown Bridged-T active notch filter configuration overcomes problem 1. and 2. It features independent tuning of the notch frequency, f_{notch} and the notch depth Q_{notch}. Initial trimming of f_{notch} with P_1 to match the mains frequency allows the tolerance of the filter determining components to be ignored. Residual component drift will now only cause minimal shift in the filter's notch frequency. Assuming 50ppm/°C drift of R and C over a ±25°C temperature range gives a minimum 50dB (300 times) hum attenuation compared with the previous discussed 26-30dB (20-30 times) for the simple parallel-T implementation - a ten fold improvement in terms of hum rejection.

In addition, the filter configuration allows for independent Q_{notch} tuning with P_2 if required. However, a fixed Q_{notch} factor is often desired for simplicity and can be set to a maximum stable value using a fixed resistor for P_2. With the TL034 in the shown configuration a Q_{notch} factor in excess of 1000 can be realised corresponding to more than 63dB hum rejection when trimmed exactly to 50Hz or 60Hz respectively.

3.16.4. Filter Design Details

Basic RC Bridged-T Active Notch Filter:



Using superposition technique the transfer function can be derived as:

$$V_o = V_i * \frac{R \| 1/sC + R}{1/sC + R \| 1/sC + R}$$

$$+ \quad nV_i * \frac{1/sC \| (R + 1/sC)}{R + 1/sC \| (R + 1/sC)} * \frac{1/sC}{(R + 1/sC)}$$

$$+ \quad (3qV_o - 2V_i) * \frac{R \| (R + 1/sC)}{1/sC + R \| (R + 1/sC)} * \frac{1/sC}{(R + 1/sC)}$$

$$V_o = V_i * \frac{R^2C^2s^2 + n}{R^2C^2s^2 + 3(1 - q)RCs + 1} \quad \ldots\ldots\ldots\ldots \omega_o = 1/RC \Rightarrow$$

$$\frac{V_o}{V_i} = \frac{R^2C^2s^2 + n}{s^2 + 3(1-q)\omega_o s + \omega_o^2}$$

In the actual notch filter shown in this application n and q are implemented as follows:

$$n = \left(1 + \frac{R_2}{R_1}\right)\frac{R_3}{P_1 + R_3}; \; f_{notch} = f_o\sqrt{n} \; ; \; \omega_o = \frac{1}{RC} = 2\pi f_o \; ;$$

P_1 can be used to set $0.95 < n < 1.05$ placing a variation in f_{notch} of ±2.5% relative to f_o with the shown component values.

$$q = \text{Fractional potentiometer value of } P_2 \qquad Q_{notch} = \frac{1}{3(1 - q)};$$

P_2 can be used to vary the steepness of the notch. To avoid instability when $q = 1$, a 27Ω resistor can be placed in series with P_2.

$$r = \frac{R_5}{R_4}$$

The ratio, r, is chosen to be 2 in this application. If r is exactly 2, a maximum notch depth can be obtained. A notch depth of 70dB was measured using 1% components for the actual circuit. Ultimately, the maximum notch depth is determined by the matching of the two resistors, R, the two capacitors, C, and the op amps open loop gain. If $0 < r < 2$ a pair of complex conjugated zeros appear. If desired, R_5 can be made adjustable, allowing for adjustment of the notch depth. For $r > 2$ the circuit produces sinusoidal oscillations at the frequency, f_o.

A_1 is acting as impedance converter but is really uncommitted - it can be used to provide other sensor signal conditioning functions as required.

3.17. High Performance Band-Pass Filter

When designing bandpass filters it is quite often easier to convert them into a low pass equivalent. This then makes it possible to make a lowpass prototype which can then be converted into a prototype bandpass filter with unity centre frequency. This can then be converted into the required filter.

The filter here uses a TLE2082 op amp, and makes use of its good unity gain bandwidth and high stability. The filter is to be a chebyshev filter and have the following specifications:-

Centre frequency	f_0	=	1 kHz
Pass Bandwidth	BW	=	300 Hz
Stop Bandwidth	SBW	=	3000 Hz
Pass attenuation	α_{MAX}	=	1.5 dB
Stop attenuation	α_{MIN}	=	40 dB

3.17.1. Chebyshev Filter

Chebyshev filters have an equal ripple passband frequency response, and a monotonic stopband roll-off. The location of its poles are based around an ellipse, giving it its equal ripple passband, whereas the butterworth filter has its poles based around a circle. However the location of their poles for similar order filters will have the angle from the y-axis in the complex plane.

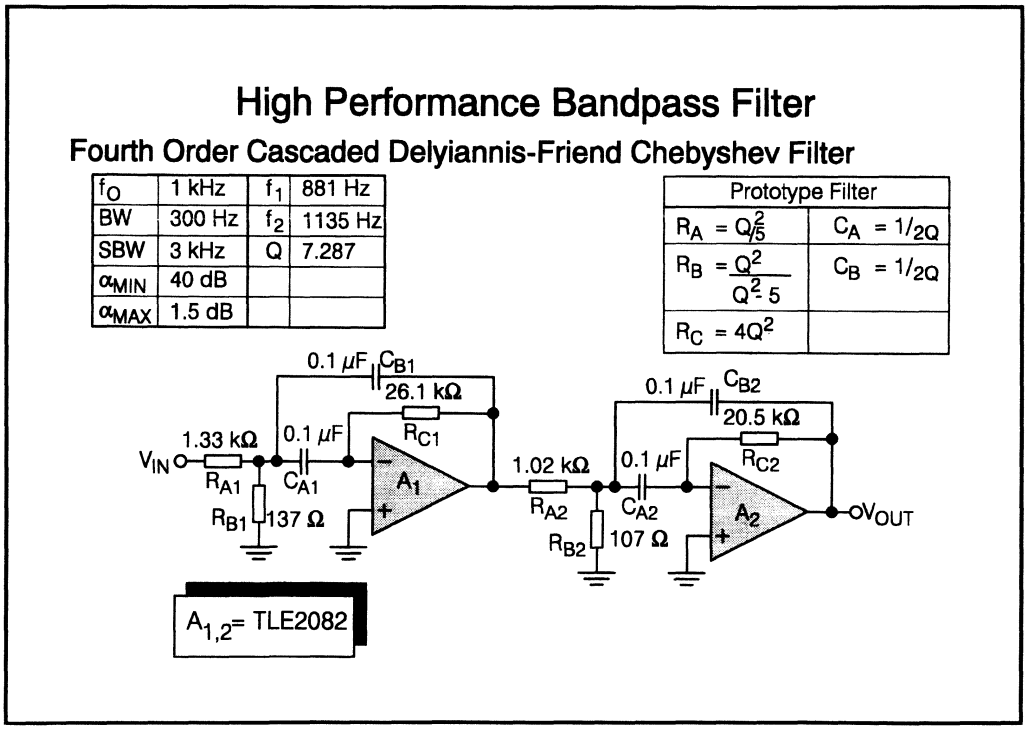


Figure 2.3.17. - High Performance Bandpass Filter

The maximum attenuation in the passband follows Lissajous patterns, giving it the equal ripple. The transfer function of the Chebyshev filter follows this equation:-

$$|T_n(j\omega)| = \frac{1}{1+\varepsilon^2 C_n^2(\omega)}$$

Where $C_n(\omega) = \cos(n \cos^{-1} \omega)$ ..... $|\omega| \leq 1$

And n is the order of the filter and ε determines the depth of ripple. For values of ω greater than 1 the cos functions become imaginary or follow cosh functions.

3.17.2. Determining Prototype

The order of filter required can be determined from nomographs or from the following equation:-

$$n = \frac{\cosh^{-1}\left[\left(10^{\alpha_{min}/10}-1\right)/\left(10^{\alpha_{max}/10}-1\right)\right]^{1/2}}{\cosh^{-1}(SBW/BW)}$$

$$= \frac{\cosh^{-1}\left[\left(10^{40/10}-1\right)/\left(10^{1.5/10}-1\right)\right]^{1/2}}{\cosh^{-1}(3000/300)} = 1.92$$

This should be rounded up to the nearest whole number, to give 2.

The poles of the prototype filter can either found from filter tables, or found using the following equations:-

The ripple in the passband is 1.5 dB, resulting in an ε of:-

$$\varepsilon = \left[10^{\alpha_{max}/10}-1\right]^{1/2} = 0.642$$

The location of the prototype filter's poles will be at:-

real part $-\Sigma_k = \sin\theta_k \sinh a$ ..... and

imaginary part $\pm\Omega_k = \cos\theta_k \cosh a$

Where $a = \frac{1}{n}\sinh^{-1}\left(\frac{1}{\varepsilon}\right)$ and $\theta_k = k\frac{180°}{n} \pm \frac{90°}{n}$ .....for k = 0 to n-1

This set a values for a of 0.613 and θ_k of 45°, and 135° which is greater than 90° and is ignored.

This gives the prototype low pass filter the following poles:- - 0.46 ± 0.844

3.17.3. Bandpass Prototype

The prototype low pass filter's poles form a complex conjugate pair, and using a complex algorithm, they will get converted into two further complex conjugate poles.

Let $q_c = \frac{f_0}{BW}$ .....Where BW is the pass bandwidth

$C = \Sigma^2 + \Omega^2$ ..... Σ and Ω are the real and imaginary

..... parts of the prototype low pass poles

$$D = \frac{2\Sigma}{q_c}$$

$$E = 4 + \frac{C}{q_c^2}$$

$$G = \sqrt{E^2 - 4D^2}$$

$$Q = \frac{1}{D}\sqrt{\frac{1}{2}(E+G)}$$ ..... Q is the quality factor

..... of the new filters

$$K = \frac{\Sigma Q}{q_c}$$

$$W = K + \sqrt{K^2 - 1}$$

$f_{02} = Wf_0$ .....Upper centre frequency of new filter

$f_{01} = f_{0/W}$ ..... Lower centre frequency of new filter

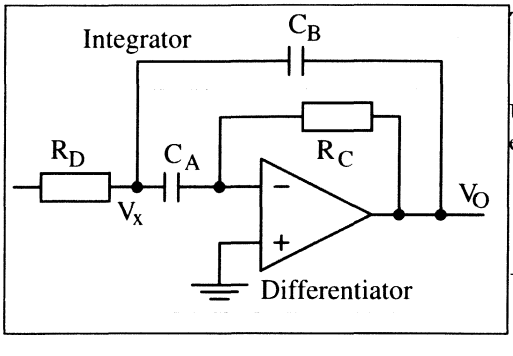
Inserting the values for Σ, Ω, f_0 and BW yields:-

q_c	=	3.33	C	=	0.925
D	=	0.277	E	=	4.08
G	=	4.05	**Q**	=	**7.29**
K	=	1.01	W	=	1.13
f_{02}	=	**1135**	**f_{01}**	=	**881**

So the two second order chebyshev bandpass filters will have their centre frequencies at 1135 Hz and 881 Hz, with a quality factor, Q, of 7.29.

3.17.4. Delyiannis-Friend Bandpass Filter

One accepted way of producing bandpass filters is the Delyiannis-Friend circuit. This circuit can be considered to consist of an inner differentiator and an outer integrator.



The relationship between V_x and V_O is:-

$$V_O = -R_C C_B s V_x$$

Using Thevenin's Law and superposition the equation relating V_{IN} to V_O becomes:-

$$\frac{V_O}{V_{IN}} = \frac{(-1/R_D C)s}{s^2 + (2/R_C C)s + 1/R_D R_C C^2}$$ Where $C_A = C_B = C$

This means that

$$f_0 = \frac{1}{2\pi C\sqrt{R_D R_C}} \qquad Q = \frac{1}{2}\sqrt{\frac{R_C}{R_D}} \qquad BW = \frac{2}{R_C C}$$

This provides the filter with orthogonal tuning; by altering both capacitors together the centre frequency can varied with altering the Q of the filter. So that resistors R_C and R_D can be altered to set the Q or bandwidth of the filter, and then the capacitors can be adjusted to set the centre frequency.

Analysing the actual component values and setting R_D and w_0 to 1 yields:-

$$R_C = 4Q^2 \qquad C = 1/2Q$$

This shows that the gain at the centre frequency is actually equal to $2Q^2$. To account for this and to give the circuit unity gain at its centre frequency a potential divider must be placed on its input. In order to maintain the same relationships between the capacitors and resistors, the potential dividing resistors must have the following relationship:-

$$R_A = Q^2/5 \qquad R_B = \frac{Q^2}{Q^2 - 5}$$

By using orthogonal tuning , the values of the capacitors can be defined, and from these the values for R_A, R_B, and R_C and be set.

The relationship between the prototype capacitor values and the final filter's values is:-

$$C_{NEW} = \frac{1}{2\pi * f_0 * k_M} C_{PROT} \qquad R_{NEW} = k_M * R_{PROT}$$

Setting C_{NEW} to 0.1 µF, defines k_M and so sets R_{NEW}. Using these factors set the resistor values shown in figure 2.3.17.

One important thing to bear in mind is the relatively large closed loop gain used about the op amp. If the device is provide low distortion and gain and signal accuracy over the frequency range chosen then the device must have a large bandwidth. The effective gain around the op amp is close to 100, and so if the op amp is maintain low distortion at its centre frequency then it gain bandwidth product needs to be of the order of 10 MHz. The TLE2082 has a bandwidth of 10 MHz and an equally high slew rate to match its bandwidth, allowing it to perform to its full without it being the limiting factor in the circuit.

3.18. TLE2061/2/4 and TLE2161 Bifets

The first Excalibur Bifets to be released by Texas Instruments were the TLE2061 family of low power, high output drive op amps

The designer's task when developing these products was to produce a family of Bifets with microwatt power consumption but with the ability to drive heavy resistive and capacitive loads. The result is a part which typically consumes less than **300µA** of supply current but can also deliver in excess of **25mA of output current!** The device is guaranteed to drive 100ohm resistive loads and will remain stable when driving capacitances up to 80nF! A further feature of its excellent output performance is its relatively low distortion. Even with microampere supply currents, the **total harmonic distortion is 0.025%,** (Avd=2, f=10kHz, R_L=10kΩ).

The excellent output drive has enabled these devices to be used extensively in low power Telecom circuits - the parts are particularly well suited in the 2 Wire - to - 4 Wire hybrid circuit found in line card and modem circuits which has a typical impedance of 600Ω.

DC wise the TLE2060's also perform outstandingly, the maximum offset voltage for the TLE2061B is **500μV**, with a specified Vio drift of 0.005μV/month and 6μV/°C.

Although achieving a very respectable **2.1MHz bandwidth** and a **3.4V/μs** slew rate, a decompensated version, the TLE2161 is also available to satisfy the more demanding ac requirements.

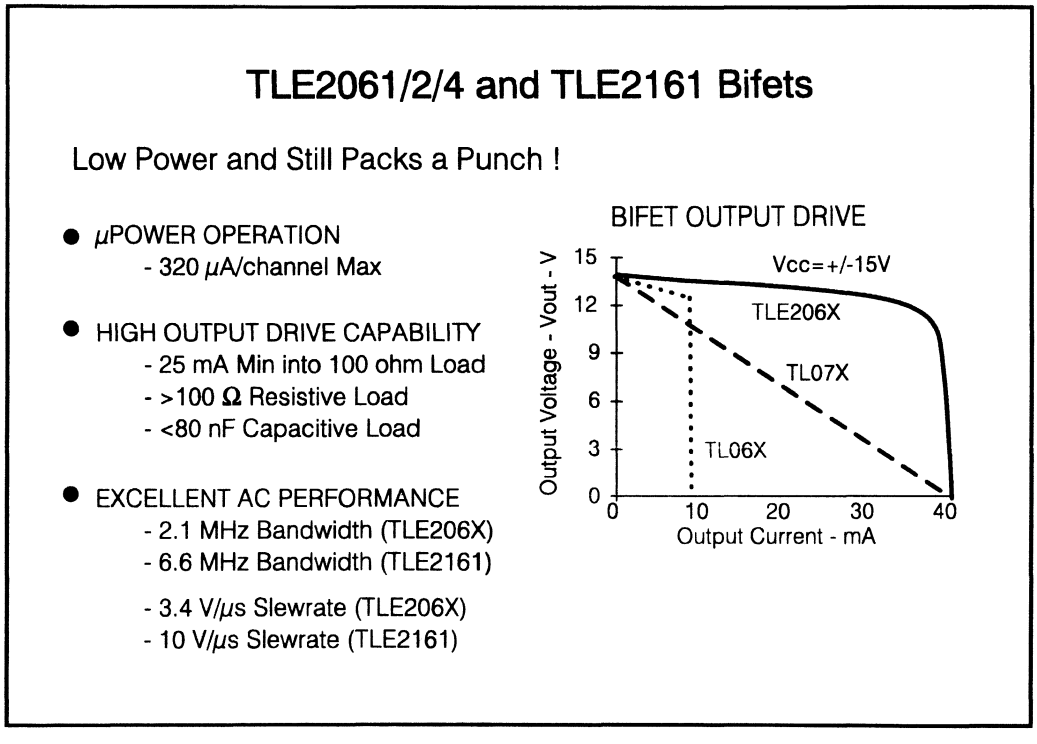


Figure 2.3.18. - TLE2061/2/4 and TLE2161 Bifets

Targeted initially at low power Telecom equipment these versatile devices are finding applications in a number of other systems. Power supplies are making use of their high common mode input range, audio systems from its ac performance and standard low power instrumentation and filter circuits are benefiting from the combination of low offset voltages and low bias currents.

3.19. TLE2064 Dual Supply 2-4 Wire Converter

Driving transmission lines creates extra demands on any operational amplifier. These demands are clearly shown in an application where the op amp needs to drive a 600Ω transformer coupled telephone line with the minimum of distortion.

The schematic shown in figure 2.3.19 shows the TLE2064 being used as a differential telephone line driver. Amplifiers A1 and A2 are used to amplify the differential output, OUT+ - OUT-, while A3 is used for amplifying the received signal. The remaining amplifier, A4, is free to provide other signal conditioning as required by the system, an audio buffer is one example.

The telephone line is used to carry information in both directions, which minimises cable costs. This results in the primary of the isolating transformer acting as both input and output to and from the line. So when the modem is driving the line (via OUT+ and OUT-) some of the signal will be fed back to the input of the modem, Rin, by amplifier A_3. This signal is reduced by the R_1, R_2, C_1 and C_2 network: The output of A1 is fed to the non-inverting input of A2 and is subtracted from the primary voltage. Careful choice of R_1, R_2, C_1 and C_2 minimises any signal from the output of the modem being fed to Rin.

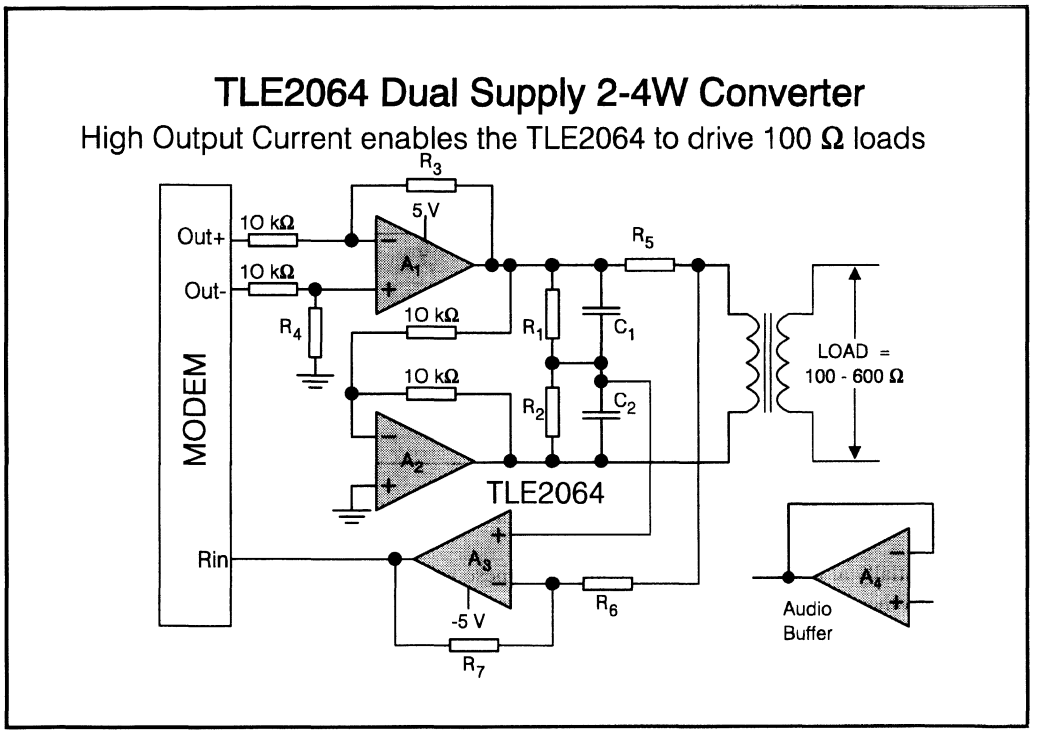


Figure 2.3.19. - TLE2064 Dual Supply 2-4W Converter

To maximise the drive to the line, it is driven differentially. A_1 acts as a differential to single ended amplifier. A_2 is configured as an inverting amplifier thus producing an inverted version of the output of A_1. As the system is duplex the output impedance of A_1 and A_2 must match the impedance of the line and transformer. However, in order to achieve low distortion the output impedance of A_1 and A_2 must be low. The **TLE2064** was designed for applications requiring such a high drive capability and at the same time a low quiescent power consumption. The TLE2064 is capable of operating from ±22V down to ±3.5V, and when driving a 100Ω load from a ±5V supply has a guaranteed minimum output swing of ±2.5V. It provides this output with a very low level of distortion.

Any distortion produced by the op amp will be sent down the telephone line via the transformer and will also be fedback to the receiver at Rin. The limited bandwidth of the transformer' will help to reduce some of the distortion sent down the line, but it cannot reduce the distortion fedback to Rin. The distortion fedback to Rin is difficult to counteract, thus decreasing the quality of the telephone system.

To match the line's impedance, the TLE2064 has to have a series resistor R_5 on its output. R_5 will form a potential divider with the winding resistances of the transformer and the line impedance. Over the frequency range of interest, the matching transformer will add phase shift to the output to the line. So the choice of R_1, R_2, C_1 and C_2 should take this potential division and phase shifting into account. Looking from the line the impedance seen will be the winding resistances in series with R_5, and so R_S should equal the line impedance minus the winding resistances:-

$$R_S = Z_{line} - (r_p + r_s)$$ .....where r_s + r_p are the primary and .....secondary winding resistances ..... of the transformer

The actual impedance of the telephone line can vary enormously from the typical 600Ω, ranging from 1200Ω down to 100Ω. The line impedance is greatly affected by the position of the 2 - 4 wire converter in the system, this will greatly affect the gain of A1 and the values of R_5, R_1, R_2, C_1 and C_2. In this application, assuming ideal impedance of the line, the low output impedance of the TLE2064 means that the series resistor, R_5, will need to be around 510Ω, ($r_s + r_p = 100Ω$).

3.19.1. Echo Cancellation

Any signal from the output of the modem fedback to the input of the modem can appear as an annoying echo. If this annoying echo is to be removed then the signal from A_1 and A_2 that is applied to the line must be removed from the output of A_3. This is normally done by feeding a proportion of the total output to the line back to the non-inverting input of A_3. This is done via resistors and parallel capacitors R_1, R_2, C_1 and C_2.

The absolute voltage at the non-inverting input of A_3 is given by:-

$$V_+ = V_{O+}\frac{Z_2}{Z_1+Z_2} + V_{O-}\frac{Z_1}{Z_1+Z_2}$$

$$= V_{O+}\frac{Z_2-Z_1}{Z_1+Z_2}$$

Where Z_1 and Z_2 are the equivalent impedances of $R_1$and C_1, and R_2 and C_2 respectively. And V_{O+} and V_{O-} are the non-inverting and inverting outputs of the differential line driver.

The voltage on the transformer just after R_5, V_L, is equal to:-

$$V_L = V_{O+}\frac{r_s + r_p + Z_L}{R_5 + r_s + r_p + Z_L} + V_{O-}\frac{R_5}{R_5 + r_s + r_p + Z_L}$$

$$= V_{O+}\frac{r_s + r_p + Z_L - R_5}{R_5 + r_s + r_p + Z_L} \quad \text{.....Where } Z_L \text{ is the line impedance}$$

Amplifier A_3 subtracts V_L and V_+ from one another, via different inverting and non-inverting gains. So the voltage at Rin equals:-

$$V_{Rin} = V_{O+}\left(\frac{R_6 + R_7}{R_6}\right)\frac{Z_2 - Z_1}{Z_1 + Z_2} - V_{O+}\left(\frac{R_7}{R_6}\right)\frac{r_s + r_p + Z_L - R_5}{R_5 + r_s + r_p + Z_L}$$

Letting R_6 = 18 kΩ, and R_7 = 36 kΩ, sets a receiver gain of -2. A value of 18 kΩ reduces any effects of R_5 and Z_L on the gain of A_3. With a line impedance of 600 Ω, and r_s+r_p = 100 Ω, and R5 = 510 Ω, the output voltage of A_3 simplifies to:-

$$V_{Rin} = V_{O+}\left(3\frac{Z_2 - Z_1}{Z_1 + Z_2} - 2\frac{700 - 510}{510 + 700}\right)$$

The ideal value forth output of A3 in this case would zero, this makes:-

$$3\frac{Z_2 - Z_1}{Z_1 + Z_2} = 2\frac{700 - 510}{510 + 700}$$

$$Z_1 = \frac{325}{401}Z_2$$

This sets the resistor ratios for R_1 and R_2. The values for capacitors heavily depend on the frequency response of the line and transformer, and can be best determined via tests. If the frequency characteristics of the line and transformer are known then the reactive component of the line impedance, Z_L, should be taken into account, and this can be used to determine the values for C_1 and C_2.

3.20. TLE2141/2/4 - High Speed Single Supply Op Amps

The TLE214X family of operational amplifiers use Excalibur's high speed PNPs to enable it to achieve extremely high speed - it is probably the **Worlds fastest single supply op amp!** It combines a number of features which make it particularly well suited to high speed, precision applications particularly in control loops for system or process monitoring.

High Speed

The TLE214X uses a double PNP input stage which enables it to operate from a single supply (i.e. its common mode input range includes ground). This technique has, in the past, limited the ac performance operational amplifiers - but by using Excalibur's high speed vertical PNPs and a patented input stage, the device has outstanding ac performance. The typical and symmetrical slew rate for the TLE214X is **45 V/µs** (30 V/µs min) and its **settling time to 0.01%** is typically only **400ns**. These two

parameters combined with a Gain-Bandwidth Product of 5.9MHz highlight just why this device is so well suited to control type applications. It should be noted that the TLE214X is internally compensated.

Low Noise

Another parameter which one does not normally associate with a single supply, PNP input, operational amplifier is low noise. The TLE214X, however, has a noise voltage specification of **15nV/$\sqrt{Hz}$** at 10Hz and, in the audio band, of **10.5nV/$\sqrt{Hz}$** at 1kHz. This combined with the excellent ac performance and resulting low distortion makes the devices particularly well suited to some hi-fi audio applications.

Output Drive

The NPN output stage has been designed to swing almost Rail to Rail (V_{CC-} +0.3 V to V_{CC+} - 1.8 V) without inducing phase reversal, and will happily drive 10 nF capacitive loads. When this is combined with the 20mA (min) short circuit output current, then the device is extremely well suited to driving heavy loads such as long cables or for use in 4-20mA current loops.

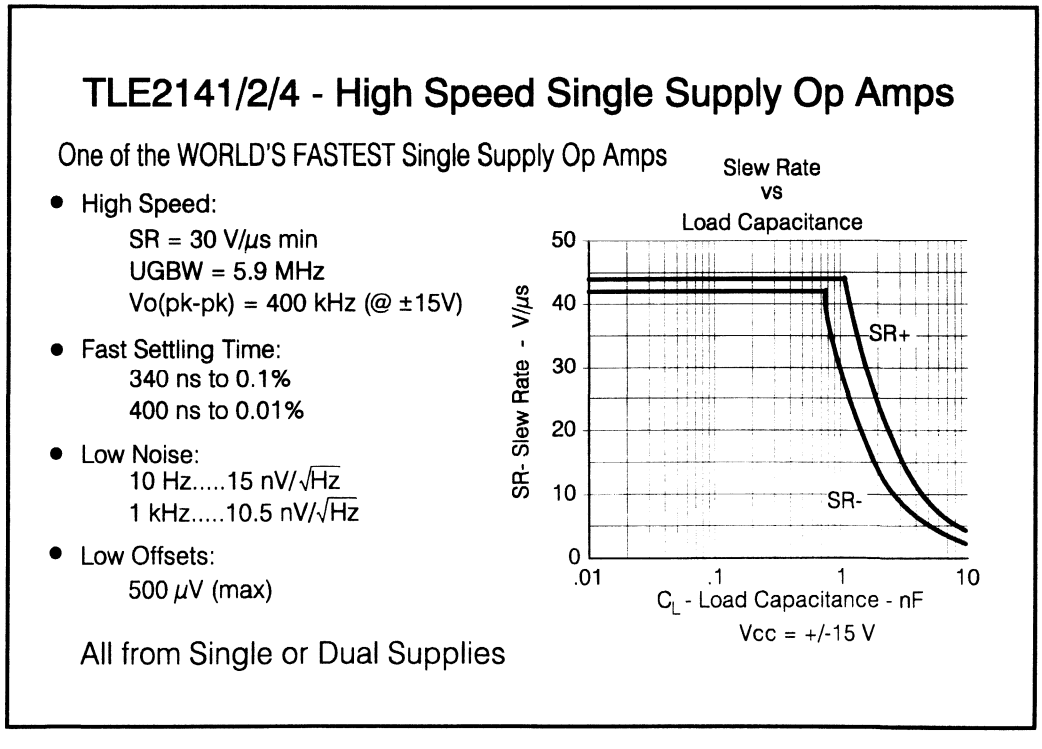


Figure 2.3.20. - TLE2141/2/4 - High Speed Single Supply Op Amps

Precision

This special design also exhibits an improved sensitivity to IC component mismatches that is evident by a 500 µV offset voltage and 1.7 µV/°C typical drift. The device also has the common mode and power supply rejection ratios set at a minimum of 85dB and 90dB respectively.

Applications

These wide range of features make the device extremely well suited to a number of different applications. High speed and fast settling time, combined with precision makes the device an ideal choice in fast actuator/positioning drivers or other control loop applications as well as performance audio systems. The accuracy, single supply operation (with rail to rail output) and low noise makes the TLE214X particularly suitable for instrumentation and measuring equipment.

The device can also be configured as a compactor - both inputs can be maintained at Vcc+/- without damage and the typical open loop propagation delay with TTL inputs is 200ns.

3.21. TLE2144 Single Supply 2-4 Wire Converter

Driving transmission lines creates extra demands on any operational amplifier. These demands are clearly shown in an application where the op amp needs to drive a 600Ω transformer coupled telephone line with the minimum of distortion. This is made even more complicated when only one supply is available.

The schematic shown in figure 2.3.21 shows the TLE2144 being used as a differential telephone line driver. Amplifiers A_1 and A_2 are used to amplify the differential output, OUT+ - OUT-, while A_3 is used for amplifying the received signal. The remaining amplifier, A_4, is free to provide other signal conditioning as required by the system, an audio buffer is one example. The whole operation is made a little more hazardous due to the fact for maximum symmetrical swing the inputs of A1 and A2 must be referred to half of the supply voltage. There two standard ways of providing half of the supply voltage; either a resistive potential divider or with a reference diode. Both of these standard ways can be power hungry due to their compromise between output impedance and current consumption. The best solution to these is the use of the TLE2425 or TLE2426. The TLE2425 provides a 2.5 V reference while the TLE2426 halves the voltage across its input pins. The quiescent supply current of both devices is 180 µA while being capable of sourcing 20 mA.

The telephone line is used to carry information in both directions, which minimises cable costs. This results in the primary of the isolating transformer acting as both input and output to and from the line. So when the modem is driving the line (via OUT+ and OUT-) some of the signal will be fed back to the input of the modem, Rin, by amplifier A_3. This signal is reduced by the R_1, R_2, C_1 and C_2 network: The output of A1 is fed to the non-inverting input of A2 and is subtracted from the primary voltage. Careful choice of R_1, R_2, C_1 and C_2 minimises any signal from the output of the modem being fed to Rin.

To maximise the drive to the line, it is driven differentially. A_1 acts as a differential to single ended amplifier. A_2 is configured as an inverting amplifier thus producing an inverted version of the output of A_1. As the system is duplex the output impedance of A_1 and A_2 must match the impedance of the line and transformer. However, in order to achieve low distortion the output impedance of A_1 and A_2 must be low. The **TLE2144** was designed for applications requiring such a high drive capability and at the same time a low quiescent power consumption. The TLE2144 is capable of operating from ±22V down

to ±3.5V, and when driving a 100Ω load from a ±5V supply has a guaranteed minimum output swing of ±2.5V. It provides this output with a very low level of distortion.

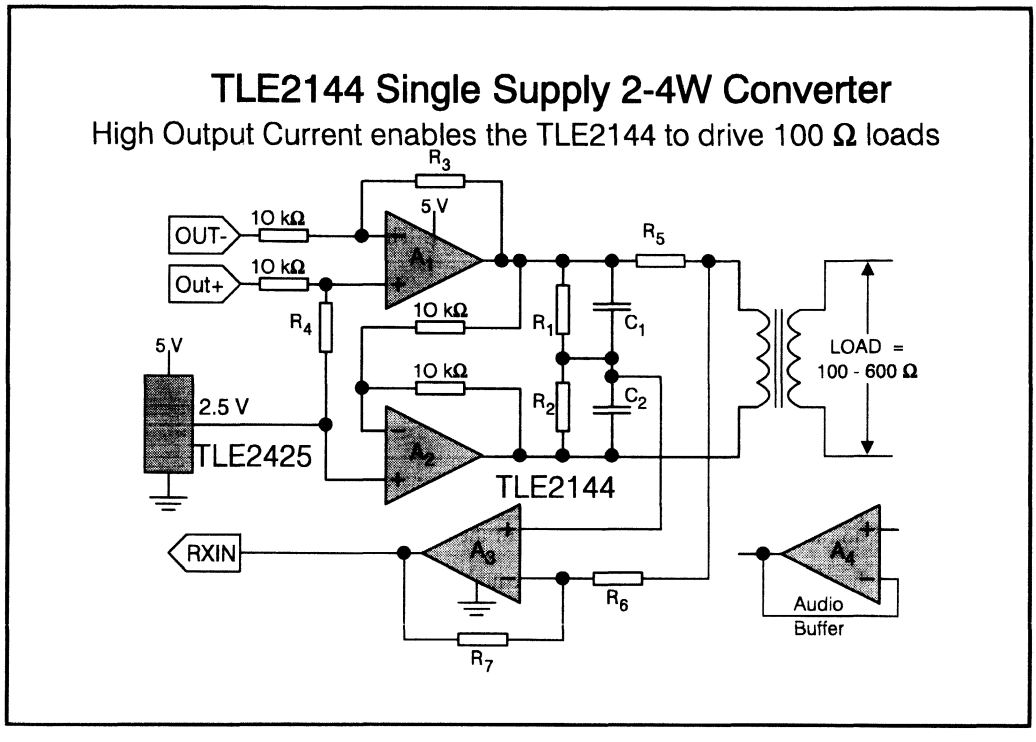


Figure 2.3.21. - TLE2144 Single Supply 2-4W Converter

Any distortion produced by the op amp will be sent down the telephone line via the transformer and will also be fedback to the receiver at Rin. The limited bandwidth of the transformer' will help to reduce some of the distortion sent down the line, but it cannot reduce the distortion fedback to Rin. The distortion fedback to Rin is difficult to counteract, thus decreasing the quality of the telephone system.

To match the line's impedance, the TLE2144 has to have a series resistor R_5 on its output. R_5 will form a potential divider with the winding resistances of the transformer and the line impedance. Over the frequency range of interest, the matching transformer will add phase shift to the output to the line. So the choice of R_1, R_2, C_1 and C_2 should take this potential division and phase shifting into account. Looking from the line the impedance seen will be the winding resistances in series with R_5, and so R_S should equal the line impedance minus the winding resistances:-

$$R_S = Z_{line} - (r_p + r_s)$$

where $r_s + r_p$ are the primary and secondary winding resistances of the transformer

The actual impedance of the telephone line can vary enormously from the typical 600Ω, ranging from 1200Ω down to 100Ω. The line impedance is greatly affected by the position of the 2 - 4 wire converter in the system, this will greatly affect the gain of A1 and the values of R_5, R_1, R_2, C_1 and C_2. In this application, assuming ideal impedance of the line, the low output impedance of the TLE2144 means that the series resistor, R_5, will need to be around 510Ω, ($r_s + r_p = 100Ω$).

3.21.1. Echo Cancellation

Any signal from the output of the modem fedback to the input of the modem can appear as an annoying echo. If this annoying echo is to be removed then the signal from A_1 and A_2 that is applied to the line must be removed from the output of A_3. This is normally done by feeding a proportion of the total output to the line back to the non-inverting input of A_3. This is done via resistors and parallel capacitors R_1, R_2, C_1 and C_2.

The absolute voltage at the non-inverting input of A_3 is given by:-

$$V_+ = V_{O+}\frac{Z_2}{Z_1+Z_2} + V_{O-}\frac{Z_1}{Z_1+Z_2}$$

$$= V_{O+}\frac{Z_2-Z_1}{Z_1+Z_2}$$

Where Z_1 and Z_2 are the equivalent impedances of $R_1$and C_1, and R_2 and C_2 respectively. And V_{O+} and V_{O-} are the non-inverting and inverting outputs of the differential line driver.

The voltage on the transformer just after R_5, V_L, is equal to:-

$$V_L = V_{O+}\frac{r_s+r_p+Z_L}{R_5+r_s+r_p+Z_L} + V_{O-}\frac{R_5}{R_5+r_s+r_p+Z_L}$$

$$= V_{O+}\frac{r_s+r_p+Z_L-R_5}{R_5+r_s+r_p+Z_L} \text{.....Where } Z_L \text{ is the line impedance}$$

Amplifier A_3 subtracts V_L and V_+ from one another, via different inverting and non-inverting gains. So the voltage at Rin equals:-

$$V_{Rin} = V_{O+}\left(\frac{R_6+R_7}{R_6}\right)\frac{Z_2-Z_1}{Z_1+Z_2} - V_{O+}\left(\frac{R_7}{R_6}\right)\frac{r_s+r_p+Z_L-R_5}{R_5+r_s+r_p+Z_L}$$

Letting R_6 = 18 kΩ, and R_7 = 36 kΩ, sets a receiver gain of -2. A value of 18 kΩ reduces any effects of R_5 and Z_L on the gain of A_3. With a line impedance of 600 Ω, and r_s+r_p = 100 Ω, and R5 = 510 Ω, the output voltage of A_3 simplifies to:-

$$V_{Rin} = V_{O+}\left(3\frac{Z_2-Z_1}{Z_1+Z_2} - 2\frac{700-510}{510+700}\right)$$

The ideal value forth output of A3 in this case would zero, this makes:-

$$3\frac{Z_2 - Z_1}{Z_1 + Z_2} = 2\frac{700 - 510}{510 + 700}$$

$$Z_1 = \frac{325}{401} Z_2$$

This sets the resistor ratios for R_1 and R_2. The values for capacitors heavily depend on the frequency response of the line and transformer, and can be best determined via tests. If the frequency characteristics of the line and transformer are known then the reactive component of the line impedance, Z_L, should be taken into account, and this can be used to determine the values for C_1 and C_2.

3.22. TLE2142/4 High Speed Low-Pass Filter

In the past, most filters were built using LCR networks, this is still true for very high speed applications. The op amp, is some ways, led to the demise of the passive LCR filter. This mainly due to op amp active filters not requiring inductors.

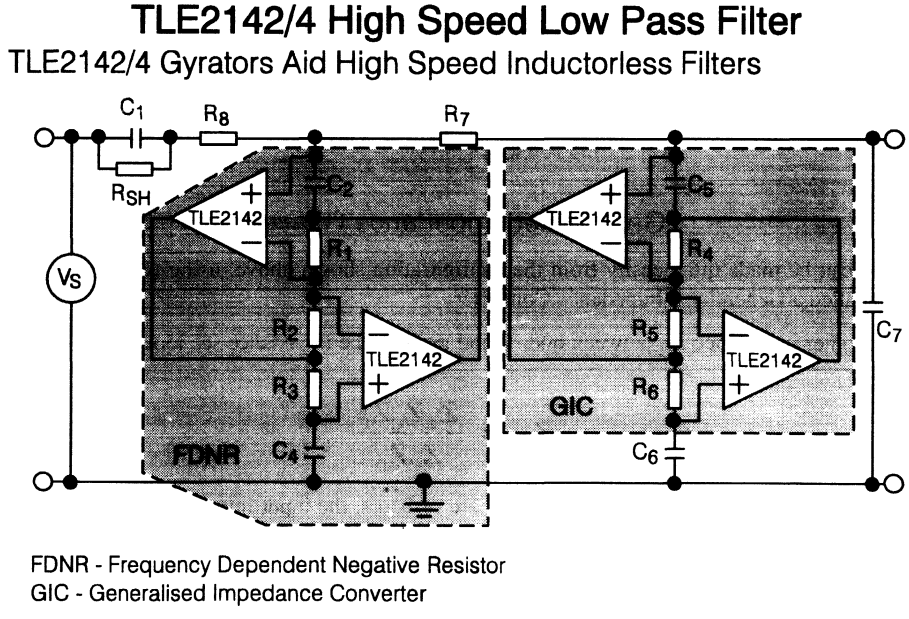


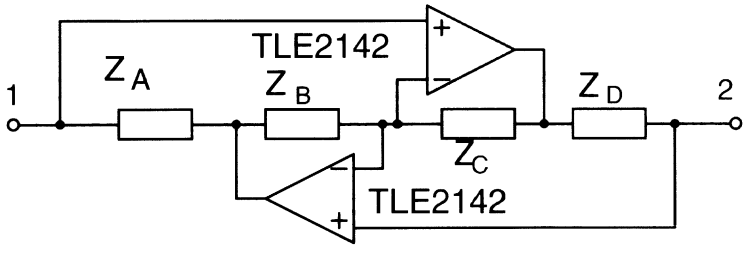
Figure 2.3.22. - TLE2142/4 High Speed Low Pass Filter

In low frequency applications, the size of inductors and capacitors would be very large, limiting their use. Op amp active filters, however, can reduce the size of passive components as well as introducing gain. At high frequencies, the speed of the op amps have always limited the active filter's use. High speed op amps are over coming this.

Passive LCR filter network design is a highly developed field, with several books published on it. Despite this, low order filters can be easy to design, by synthesising them in a ladder form it was relatively easy to build up the filter sequentially. The largest advantage of LCR filters is their very sharp responses, that is due to the parallel LC resonance. Another advantage is their relative low sensitivity to variations of component values.

By far their largest problem is the inductor used in them. For most frequencies the inductors will normally be very large and bulky. These problems are increased by their far from ideal electrical performance, being lousy due to high serial resistance and magnetic losses.

The development of op amp gyrators has led to some interest in gyrator substituted LCR ladder filters. A gyrator, quite simply, converts an impedance to its inverse, that is a capacitor to an inductor. By converting a capacitor into an inductor, the parallel LC resonance can be synthesised without the need for inductors.



Generalised Impedance Converter

A gyrator can be made quite easily from the configuration shown above, using two op amps in what has been called a Generalised Impedance Converter.

Placing another impedance Z_E between node 2 and ground, the impedance see looking into node 1 will be equal to:

$$Z_{IN} = \frac{Z_A Z_C Z_E}{Z_C Z_D}$$

Making Z_4 a capacitor while Z_1, Z_2, Z_3 and Z_5 are resistors, the input impedance looking into node 1 will be:

$$Z_{IN} = \frac{R_A R_C R_E}{R_B \frac{1}{sC_E}} = K_m s C_D$$

Where K_m equals $R_A R_C R_E / R_B$.

This has converted the capacitor into a grounded inductor, and is very useful for high pass filters. For Low pass, band pad and band stop filters, a floating inductor will also be required. The floating inductor can be synthesised from two GICs back to back. Another way is to use Frequency Dependent Negative Resistors, FDNRs, denoted by symbol D.

The equation of a second order LCR low pass filter is:-

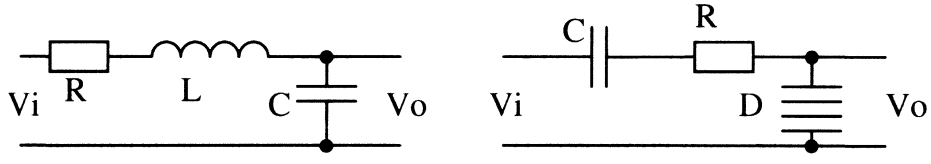
$$T(s) = \frac{1/sC}{R + sL + 1/sC}$$

Where T(s) is the ratio of Vo to Vi. This can be converted to a circuit using FDNRs by dividing the numerator and denominator by s, the complex angular frequency operator.

This transforms T(s) to:-

$$T(s) = T(S) = \frac{1/s^2C}{R/s + L + 1/s^2C}$$

So converting the resistor to a capacitor, the inductor to a resistor, and the capacitor to a FDNR. The circuit schematics are shown below.



LCR Lowpass Filter CRD Lowpass Filter

The advantage of this circuit is that the FDNR is referred to ground and only the resistors and capacitors are floating, The FDNR is made by using the GIC with Z_A, Z_B, Z_C and Z_D as described before, but with a capacitor, C_E placed between node 1 and ground, using node 2 as the input.

The impedance seen looking into node 2 is:-

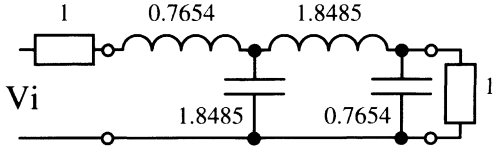
$$Z_{IN(2)} = \frac{R_B \, 1/sC_D \, 1/sC_E}{R_A R_C}$$

Expressing this in angular frequency, jω, this becomes

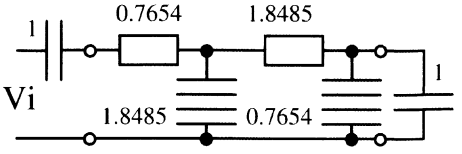
$$Z_{IN(2)} = \frac{-1}{D\omega^2}$$

A negative resistance that decreases with the square frequency. Normalising the component values gives R_B=R_C=1 and C_D=C_E=1, R_A=D.

The figure above uses two FDNRs to make a fourth order Butterworth Low pass filter, both types of 1 Hz prototype are shown below.



LCR 4th order Butterworth lowpass filter



CRD 4th order Butterworth lowpass filter

For a 20 kHz 3dB bandwidth, the resistors and FDNRs must be scaled by km, $2\pi 20000$ (125.7×10^3).

Setting all capacitors to 1 nF means that all resistors must be scaled by k_m:

$$k_m = \frac{1}{(2\pi \times 20000)(1 \times 10^{-9})} = 7958$$

Therefore $C_1=C_2=C_3=C_4=C_5=C_6=C_7=1$ nF

R_n	Prototype	Value/kΩ	Component (E96)/kΩ	R_n	Prototype	Value/kΩ	Component (E96)/kΩ
R_1	1	7.958	7.87	R_2	1	7.958	7.87
R_3	1.8485	14.71	14.7	R_4	1	7.958	7.87
R_5	1	7.958	7.87	R_6	0.7654	6.091	6.04
R_7	1.8485	14.71	14.7	R_8	0.7654	6.091	6.04

Note: A shunting resistor R_{SH} is in parallel with C_1 in order to pass through the dc signal., Although low pass filters using FDNRs have, in theory, the right transfer functions, in reality, there is a dc blocking capacitor on the input of the filter. R_{SH} shunts this capacitor out at dc, and a high value quickly makes its effect on the transfer function negligible.

The TLE2142/2 are well suited to this form of filter due to their high output current drive capability and their excellent stability. This stability shows itself in both the high slew rate and very small settling times, whilst driving 500 pF capacitive loads. For greater dc accuracy, the TLE2141 could be used in place of the TLE2142/4 devices.

4. Single Supply Considerations

4.1. Power Supply Considerations

When choosing the power supply there are several factors that must be taken in to consideration. One thing is the dynamic range.

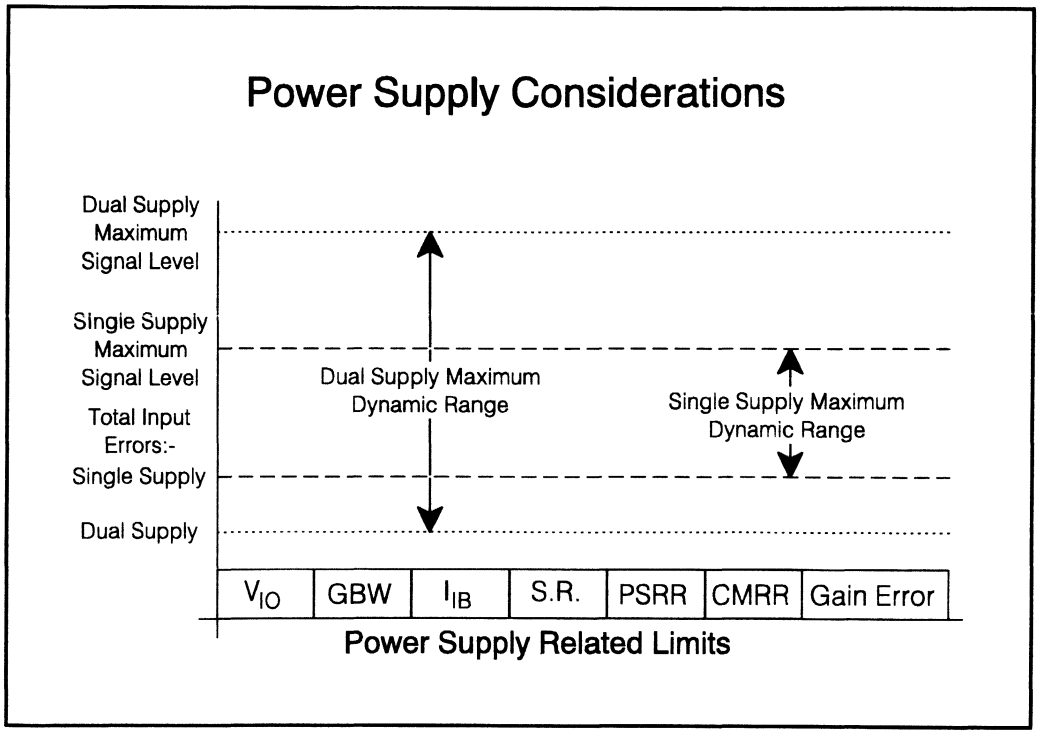


Figure 2.4.01. - Power Supply Considerations

If the supply voltage is reduced from ±15 V down to +5 V, then the available dynamic range has been reduced by about 80%, which is entirely due to the fact that the available output voltage swing has been reduced.

The reduction in power supply will have the greatest effect on devices that have been designed for operation at ±15 V. Reducing the supply voltage will have an impact on the quiescent current of the op amp. This can affect the whole operation of the op amp due to changes in the operating point of the op amp.

An op amp designed for ±15 V operation will have been designed for its inputs to stay around 15 V above its negative rail. If the supply voltage is reduced to +5 V, then its input will now be around 2.5 V above the negative rail, this will subject the op amp to large common-mode and large supply voltage changes which will impact the offset voltage of the device.

The change in supply voltage and quiescent current can also impact its ac performance:- slew rate and gain bandwidth product.

It is, therefore, quite often better to choose an op amp designed specifically for 5 V operation rather than choose an op amp which has very good specifications at ±15 V. The device designed for ±15 V might not even work at +5 V.

4.2. Power Supply Effects

The curves in figure 2.4.02 show some typical characteristics of op amps as their input voltages are changes.

4.2.1. Common-Mode Input Voltage Range

The limiting factor on an op amp's in voltage range is when its input stage starts to turn off. This can be when the current source to the differential input stage cannot provide any more current due to its finite saturation voltage. Or it can be when the input transistors themselves have been driven so hard that they have reached their finite saturation voltage. The latter state can quite often cause gain inversion, because as well as causing the inputs stage to turn off it can cause the next stage to turn off.

The saturation limits of the input stage to an op amp is related to the actual supply voltage, and so as the supply voltage varies the op amp's common-mode input range will also track it. There are ways of overcoming this, and this is particularly relevant for single supply op amps where the inputs must be capable of swinging down to the negative rail.

4.2.2. Peak Output Voltage Range

There are a number of different output stage configurations. For low distortion and dual rail operation a class AB output stage is often used. This often results in the output stage being capable of swinging to within 1.5 V of the supplies. So as the supply voltage varies the maximum output swing will track it.

Single supply op amps will have a different output stage enabling them to swing to the negative rail. However most of these devices still do a limit on their positive output swing. So even though the output can swing to ground (negative rail for single supply systems) the positive supply still tracks the supply voltage with a 1.5 V drop-out.

4.2.3. Supply Current

The biasing circuitry of the op amp will consist of a series of current mirrors, however, these ultimately be controlled by some resistor and reference. These will have some dependence on the supply voltage and so some variance in the supply current will be seen as the supply voltage varies. The variance in

supply current will affect every current mirror and so will affect every parameter of the op amp; dc and ac.

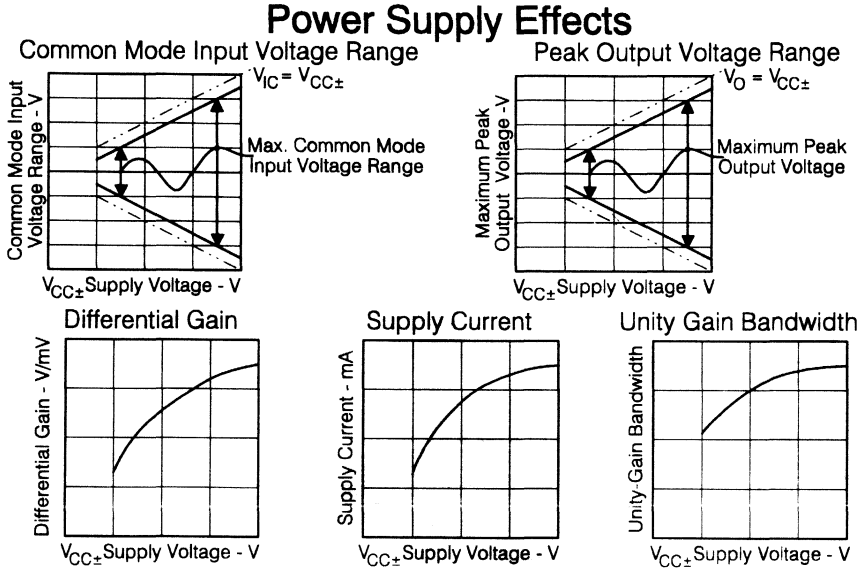


Figure 2.4.02. - Power Supply Effects

4.2.4. Differential Gain

The differential gain of the op amp is heavily dependent on the supply current of the op amp so as the supply current varies the open loop gain will also vary. Most devices show a positive increase in gain with supply voltage increase.

4.2.5. Unity Gain Bandwidth

The unity gain bandwidth of an op amp is dependent on the gain of the op amp and on size of compensation capacitor. As the supply current increase the gain increases, and this will lead to the bandwidth increasing. As will the slew rate of the device

All these parameters and more are affected by the supply voltage, and so when operating devices specified for ±15 V operation special care must be taken if their supply voltage is reduced.

It is for some these reasons that the single supply op amp was developed.

4.3. Single or Dual Supply

4.3.1. What makes an op amp single supply

There are a number of fundamental differences between operational amplifiers that have been developed for either single or dual supply applications. Many design problems are caused by an engineer using an op amp with the wrong configuration of power supplies. By understanding a few basic ground rules, often technology related, it is possible to ensure an op amp is always used correctly. Figure 2.4.03 answers some of these questions.

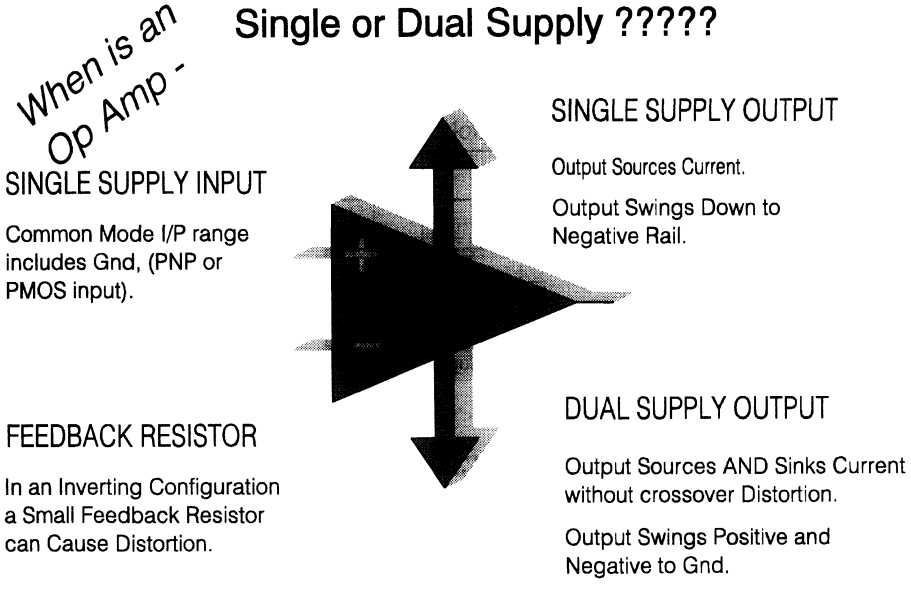


Figure 2.4.03. - Single or Dual Supply?

Transistor Type on Input

A single supply op amp should have a Common Mode input voltage range that includes the negative supply rail (usually ground) and have an output that also swings very close to this rail.

A Common Mode input range that includes the negative rail can be achieved by using the following transistor types on the op amp's input; PNPs, 'P-Channel' Mosfets or 'N-Channel' JFETs. Bipolar op amps can easily be designed with PNPs on the input and therefore single supply performance can be easily achieved from bipolar technologies. CMOS devices make good single supply op amps because they use PMOS transistors on the input stage, but Bifets have a problem! 'N-Channel' JFETs exhibit

very poor stability and high leakage with high drain-gate voltages, and today are rarely used in the input stage of an op amp. Bifets then, use 'P-Channel' JFETs on the input and are therefore not developed for single supply applications.

Bifets and bipolar op amps with NPN input stages do, however, have their benefits. They now have a Common Mode input range that can include, (and in the case of the TLE2061 family actually exceeds) the positive rail. This is useful in various 'High-Side Monitoring applications' such as power supply circuits. NPNs also have the advantage of enabling op amps with lower noise and increased gain and precision.

Output Stage Design

The second requirement for a single supply op amp is that the output must swing very close to the negative rail. In the case of CMOS designs this is easily achieved by using NMOS transistors on the output - developing an output that swings to within a few microvolts of the ground is relatively simple. In this type of circuit the output has been designed to predominantly source current.

Bifet and bipolar op amps can effectively use the same type of bipolar output stage but developing an output that swings down to the negative rail using these technologies is not so simple. In op amps such as the LM324, the output has been designed specifically to source current, and for use in single supply applications. The typical requirement, however, for the majority of amplifiers designed using bipolar or Bifet technologies is that they are able to both **Sink and Source current** - i.e. they are capable of driving a load that is connected to the mid point of their supplies without crossover distortion. This feature, when combined with the capability of the output to swing all the way to the negative rail makes the design of an output stage very complicated. Clever design techniques are therefore needed to realise true single supply bipolar op amps. Devices such as the TLE2141 and LT1013 are examples of products that perform well in both situations - they have an output that swings close to the negative rail **and** they can also sink and source current.

Other newer bipolar op amps are also often termed single supply amplifiers - their common mode input range includes ground and their output swings very close to, if not all the way to the negative rail. An example is the TLE2021 family, these designs are ideally suited to many single supply applications and are very different to products which have been optimised for dual supply applications only.

Newer CMOS designs are also being developed for use with both single and dual supply rails. Op amps such as the TLC2201, TLC2272 and TLC2274 are excellent with a single supply, and their output will swing all the way down to the negative rail. With dual supplies their output will happily sink and source current, and will swing to within tens of millivolts of each rail without causing distortion.

Figure 2.4.04 shows what errors can occur if an op amp, designed for single supply circuits, is used in a dual supply configuration.

4.4. Single Supply Characteristics

Figure 2.4.03 put single supply op amps into two categories;

1) Those whose output can source current only

2) Those that can both sink and source current and have been designed to drive a load which is connected to the mid point of the supplies.

Figure 2.4.04 shows three different output stages.

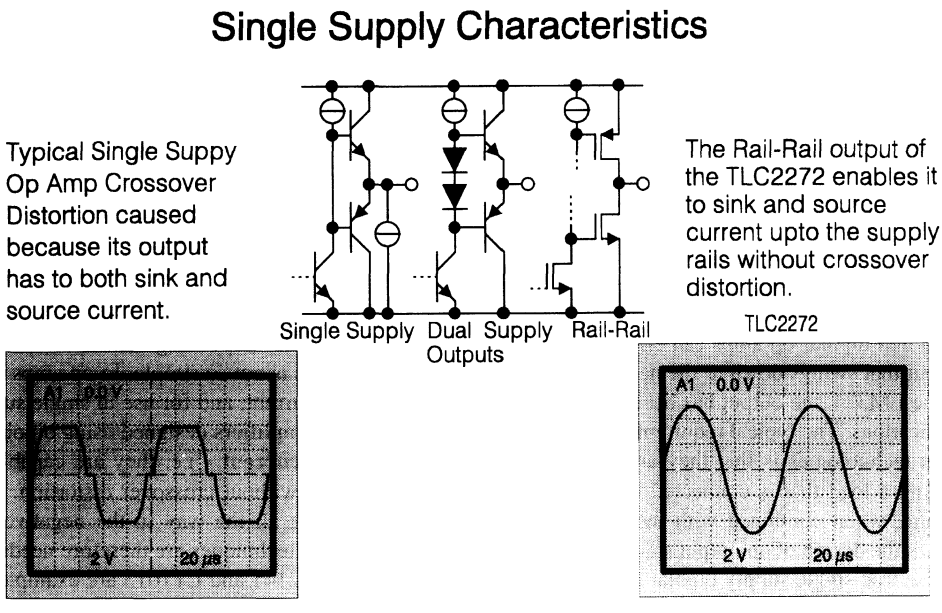


Figure 2.4.04. - Single Supply Characteristics

4.4.1. Dual Supply Output

This output has been designed to sink and source current with minimum distortion. This means that the device has a traditional class AB output swing. It, however, limits its swing to either supply rail to about 1.5 V, as was discussed in 4.2. This due to the fact that the outputs consist of a NPN emitter follower and a PNP emitter follower.

4.4.2. Single Supply Output

Here the device has been designed to mainly source current. Figure 2.4.04 shows this, the NPN transistor in the output stage will source all of the current. This enables it to swing very close to ground. In order to maintain a relatively high performance even for light loads a current load has been placed on the output. This means that the op amp will still have to source current even if the load is in the order of megaohms, which help preserve linearity. However this will limit its swing down to the negative rail.

To allow it to sink current as well as source it, the output stage also includes a PNP transistor. This output stage will introduce distortion when asked to sink and source current due to the two base emitter voltage drop between the NPN sourcing current and the PNP sinking current. This causes the cross-

over distortion shown in figure 4.4.04. It will also introduce output voltage swing limits similar to that of the dual supply output stage due to the fact that its output now consists of two emitter followers.

4.4.3. Rail-to-Rail Output Stage

The rail-to-rail output stage consists of two common source output FETs, which enables the output stage to swing very close to both rails. The only limit on how close the output can get to the supply voltage is determined by the devices output impedance. By using CMOS transistors, when driven into saturation, the output stage will appear as true resistors. They do not suffer from the usual drop-out voltage of bipolar output stages. This allows these devices to swing virtually up to the supply voltage rails with the minimum of distortion due to clipping. This output stage also allows the device to operate from both single supplies and dual supplies.

The latest op amps available from T.I. to offer this type of output are the TLC2272 and TLC2274 (which have already discussed), and the TLC2801 and TLC2872 high temperature op amps (see section 2.5)

4.5. Dual Supplies from a Single Supply

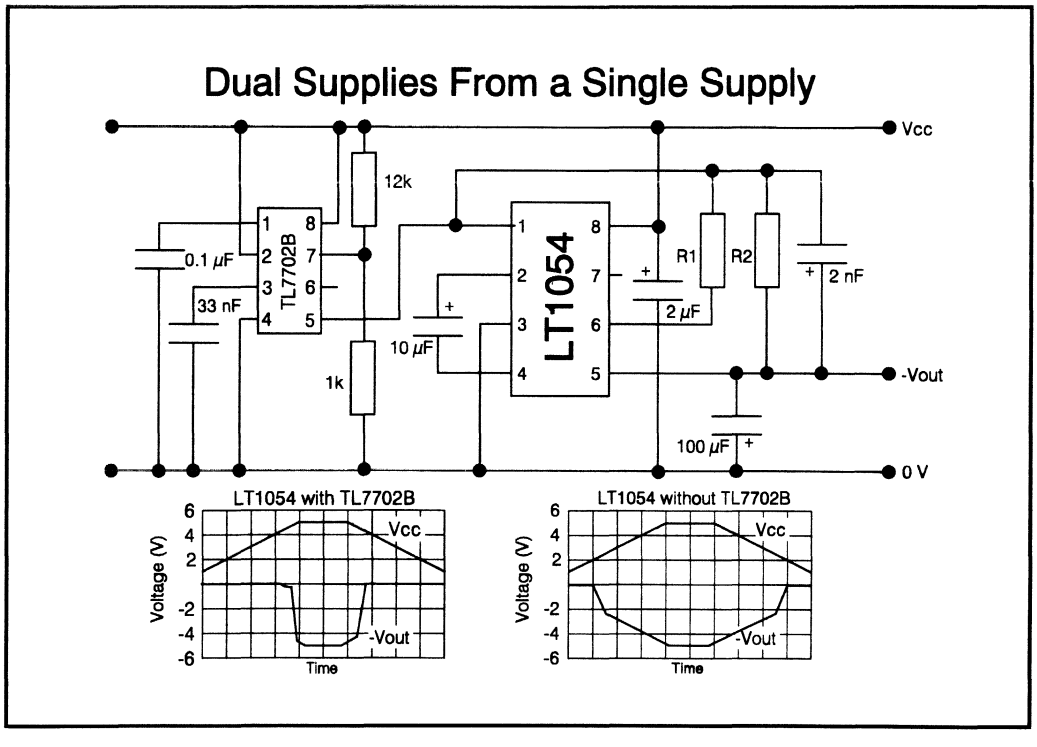


Figure 2.4.05. - Dual Supplies From a Single Supply

The single supply market has increased rapidly over the last few years, due to the introduction of portable and mobile equipment; such note books and palm top computers. However, some of this equipment still requires dual supplies for signal conditioning, data conversion and data communication. This negative supply can be generated by using the LT1054.

4.5.1. LT1054

The LT1054 operates on the switched capacitor technique to obtain the negative output voltage. The internal switching speed of the LT1054 has been designed to run in the frequency band where voltage losses are minimum and therefore have the highest possible efficiency. The clock frequency for the LT1054 is typically 40 kHz.

In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull down to keep the device in shutdown until the output capacitor (Cout) has fully discharged. For most applications where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start-up before the output capacitor has fully discharged, a restart pulse must be applied to the FB/SD of the LT1054. the restart signal can be either a pulse of duration longer than 100 µs or a logic high.

4.5.2. Feedback resistors R_1 and R_2

$$R_2 = R_1\left(\frac{V_{OUT}}{\frac{V_{REF}}{2} - 40\ mV} + 1\right)$$

Let $V_{REF} = 2.5\ V$ $R_1 = 20\ k\Omega$,

$$R_2 = 20\ k\Omega * \left(\frac{-5\ V}{\frac{2.5\ V}{2} - 40\ mV} + 1\right) = 102.6\ k\Omega$$

4.5.3. TL7702

The feedback/shutdown of LT1054 (pin 1) can be controlled via the TL7702 supply voltage supervisor. Due to the power up and power down characteristics of the LT1054, the addition of the TL7702 will ensure that the output voltage of the LT1054 will be between -5 V ±5% at all times. This is accomplished by setting the reference of the TL7702 to approx. 4.5 V, thus when the supply voltage is below this threshold voltage, the output open collector of the TL7702 is held low. This in turn will hold the FB/SD pin low. This places the LT1054 into the shut-down mode. When the LT1054 is in the shutdown mode, the reference/regulator is turned off and the switching stops. The quiescent current in the shutdown mode drops to approximately 100 µA. When the system supply voltage increases above 4.5 V. the output of the TL7702 is driven high (or in this case open circuit) and the LT1054 fires up to produce the -5 V supply that is required.

A minor modification can be made to the circuit so that the negative rail can be powered up independently when required. This can be accomplished by connecting the $\overline{\text{RESIN}}$ to a micro

controller for instance instead of to the positive supply rail. This will then enable the designer to power up the negative supply rail when required, thus potentially saving on system power.

4.6. High Performance Dual Bifet Op Amp from 5 V

There are a lot of applications where it would be nice to have the performance of Bifet operational amplifiers, but only a single 5 V supply is available. The TLE2662 device from T.I. combines a TLE2062 dual op amp with a charge pump, thereby providing you with a Bifet op amp capable of operating from a single 5 V supply.

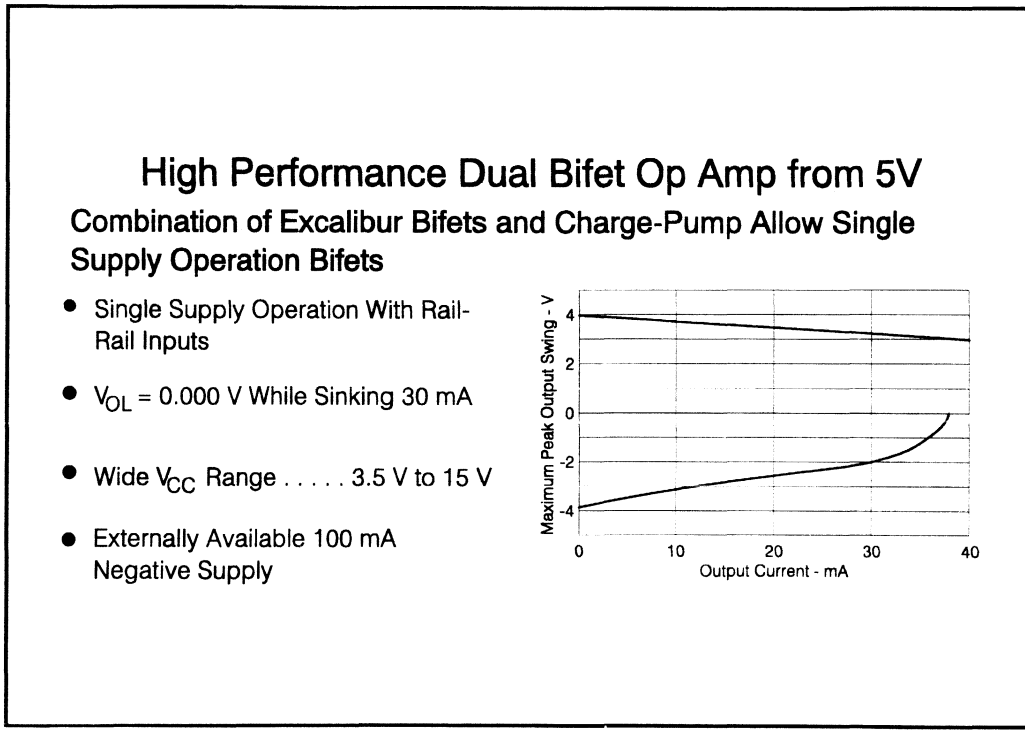


Figure 2.4.06. - High Performance Dual Bifet Op Amp from 5V

One advantage of most Bifets is that their inputs will typically swing beyond the positive supply voltage. This has, in the past, made them useful for current sensing applications. By combining the TLE2062 with a charge pump you can now get an op amp with an effective common mode input range that includes both applied supply rails.

The inclusion of the charge pump also allows it to sink current beyond the applied negative supply voltage, that is the output can sink in excess of 30 mA whilst maintaining an output voltage of less than 0 V.

The on-chip charge pump can also be used to supply current, around 100 mA, to other circuitry. This makes the device well suited to portable systems where board space and weight are of premium importance.

4.7. Dual Rail operation from Single Supply

Figure 2.4.07 shows an ideal application for the TLE2662. The TLE2662 is being operated from a single 5 V supply, is therefore supplying its own negative supply. In the mode of operation no direct feedback is being applied and so to some extent the charge pump is in free or open loop operation. The regulation of the negative supply could be improved by using feedback. This is covered in more detail in the application information section of the datasheet on the TLE2662, which is included in the seminar databook.

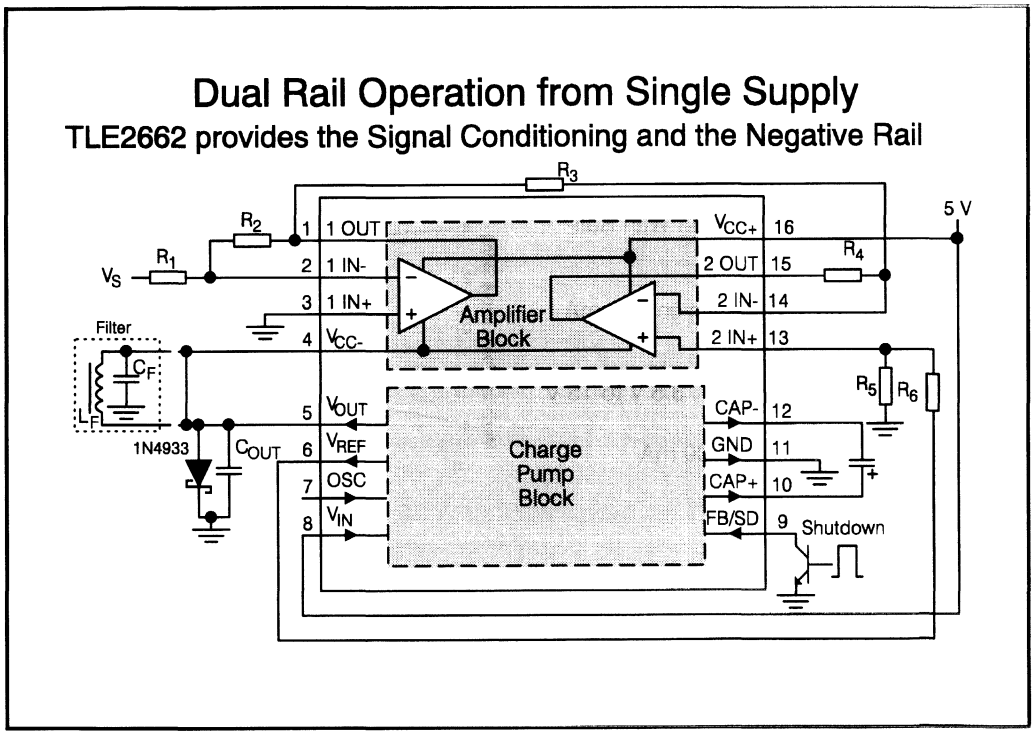


Figure 2.4.07. - Dual Rail Operation from Single Supply

The first amplifier of the TLE2662 is used to amplify the output of a ground referred transducer. The high input impedance of the TLE2662 make it ideal for interfacing to high impedance transducers. In single supply applications where the sensor is referred to ground half of the output signal could be lost due to the output being limited to only positive swings.The charge pump included in the TLE2662 allows the op amp's output to swing below ground, making it ideal for interfacing to transducers that are referenced to ground.

The second amplifier, of the application, makes use of the TLE2662's reference voltage output, and level shifts the output voltage of the first amplifier. The second amplifier could, therefore, be used as the interface to an ADC.

With an increase in single 5 V systems the dual supply capability of the TLE2662, and its increased output swing capability, can be used to increase the dynamic range available from a single 5 V supply. Another benefit is that the TLE2662 could be used to supply the negative rail to the rest of the system requiring a negative rail. It could be used to used to provide the negative rail for an ADC as well as the ADC's reference.

4.7.1. Charge Pump

The negative output of the charge pump of the TLE2662 is connected to the substrate of the device, this means that the device can be susceptible to start-up problems if the negative output of the device is brought above its ground pin. This can quite often happen driving loads that are not directly connected ground.

One such example is an op amp; no general purpose op amp has a low impedance 0 V connection, so the charge-pump of the TLE2662 will see the op amp as a load referred to the positive rail. Whether or not this creates a problem depends on the load the op amp is trying to drive.

One way of removing any likelihood of problem is to use a fast recovery schottky diode to clamp the output of the charge-pump close to ground during start-up.

4.8. Single Supply Operation

There are applications where operation from a single 5 V supply is mandatory. If this is the case, careful consideration needs to be paid to the voltage at which the inputs of the op amp is biased.

Normal dual supply op amps in an inverting configuration will have their inputs biased around 0 V, this allows its output to swing symmetrically around 0 V.

However if an op amp operating from a single 5 V supply has its inputs biased around 0 V, then positive input voltages will drive its output into saturating just above 0 V. While negative input voltages (if possible from the system) will drive the output into its normal positive output swing.

So if an op amp operating from a single supply voltage is to operate properly then its inputs must be biased at around half of the supply voltage. Figure 2.4.08 shows the effects of biasing the inputs at 0 V and at half of the supply voltage.

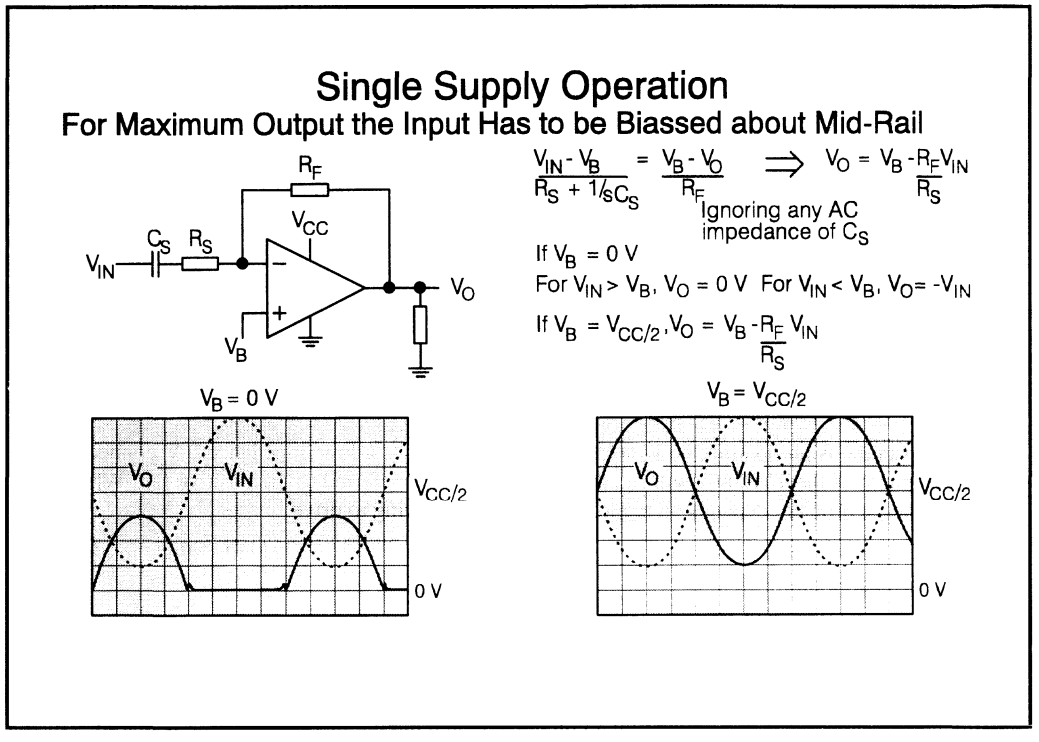


Figure 2.4.08. - Single Supply Operation

However whenever biasing the single supply op amp with its input at half of the supply voltage the loading of the feedback resistors must be taken into account. The feedback resistor will be treated as a load by the op amp, and if the loading is too great crossover distortion similar to that shown in figure 2.4.04 could be introduced.

4.9. TLE2425/6 - Virtual Ground Generators

The number of systems requiring some form of accurate reference voltage can be quite staggering, one example was discussed above. Just about all single supply applications require an accurate reference, which will need to be able to supply varying amounts of current.

It is for those reasons why Texas Instruments developed the TLE2425 and TLE2426 series of "Analogue Grounds".

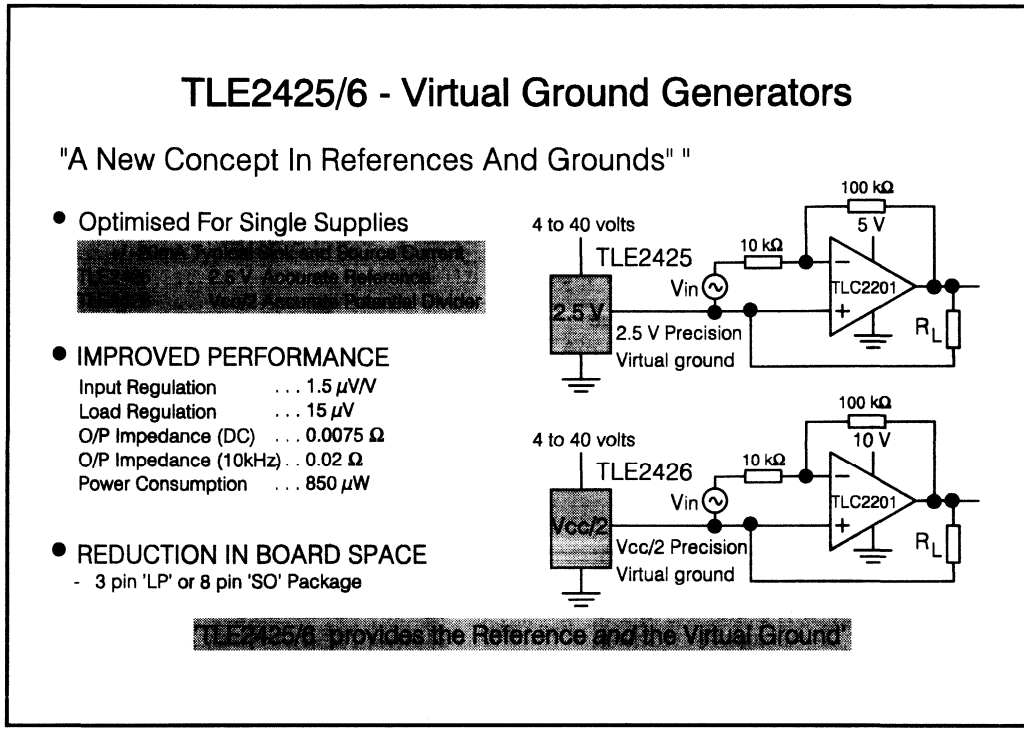


Figure 2.4.09. - Virtual Ground Generators

The TLE2425 contains an accurate low power 2.5 V reference that is buffered by a low power high output current capability op amp. This makes it ideal for 5 v supplied applications where either a low power reference is required, or a low impedance artificial ground is required. The TLE2425 requires only 170 μA of quiescent current while being capable of sourcing more than 20 mA of output current. No other integrated circuit can match this performance, and even discrete arrangements find it virtually impossible to meet the output current to quiescent current ratio, especially when the TLE2425 has been designed to drive capacitors of up to 100s of micro farads. No op amp can drive these orders or capacitors over this range without extensive compensation.

The TLE2426 is very similar to the TLE2425 except that it contains a high impedance potential divider. This provides an "Analogue Ground" equal to half the voltage applied across its IN and COMMON terminals. This makes it particularly useful when trying to maximise the output swing of dual supply op amps (see later on for definition of dual supply op amps), whose outputs have not been designed to swing to either rail, but about the middle of the supplies.

The diagram above shows many different ways of providing the functions that the TLE2425 and TLE2426 provide in one integrated circuit.

4.10. Unbalanced Power Supply Correction

The TLE2426 can introduce great benefits when used as an analogue ground in an unbalanced supply system.

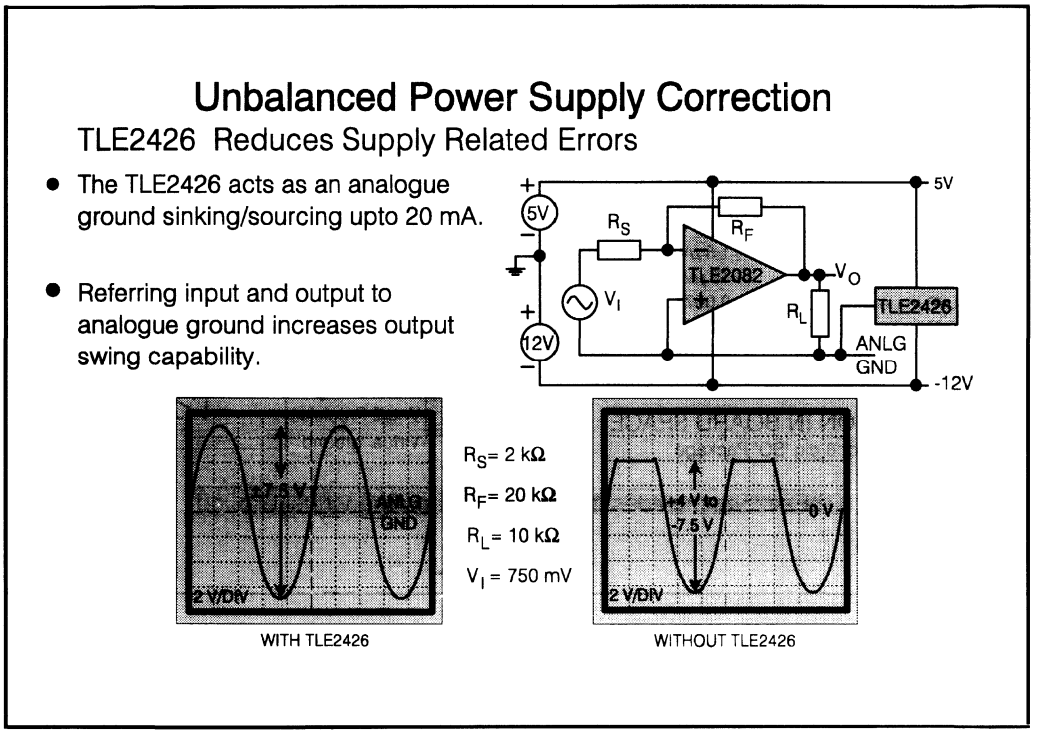


Figure 2.4.10. - Unbalanced Power Supply Correction

All op amps are 5 terminal devices; the positive and negative (ground) supply pins, the two outputs and the output. The op amp itself has no ground pin and therefore has no direct relation to the system ground, but only to half of the total supply voltage. Most op amps have been designed for their inputs to work in the middle of the supplies, hence their database parameters tested and specified at mid-supply. So when operating op amps with unbalanced supplies, the actual specified performance can differ from what is actually achieved in the application. Typical errors seen will be increased common-mode errors, loss of symmetry in output swing or even clipping.

The TLE2426 by halving the total power supply, can be used as a half supply analogue ground. Referring both the inputs and loads to this ground reduces the common mode errors as well as the loss of symmetry in output swing.

An unbalanced supply will have one supply greater than the other, in the figure shown below the positive supply is a 5 V while the negative supply is at -12 V. This means that any op amp connected to these supplies whose input is referred to ground will have a much greater negative output swing than

on the positive. This can quite easily lead to clipping on positive excursions of the wave form, as shown in figure 2.4.10.

The use of TLE2426 in providing a true low impedance ground, allows both the inputs and outputs of the op amp to be referred to the new ground, and provide a symmetrical un-distorted wave form.

A potential divider could have been used to bias one or both of the inputs, which requires ac. coupling, but the input signal generator and output load would still be connected to ground. The loading of the op amp would still be unbalanced, with the positive excursions going up to 4 V and the negative excursions going down to -11 V, resulting in the op amp having to supply approximately 3 times the current to negative swings than positive swings. This itself can lead to distortion when driving heavier loads. The TLE2082 is specified to drive a minimum of 30 mA, resulting in this having little effect on its performance.

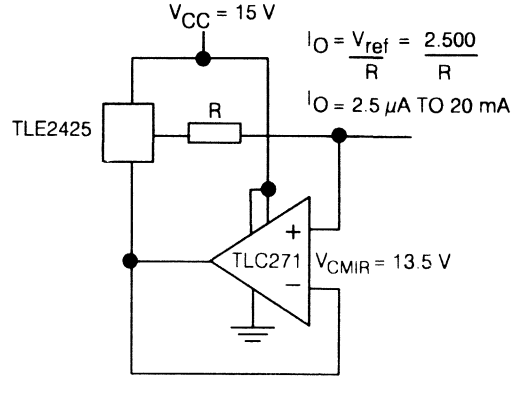
The TLE2426 can have further applications with dual supply rails where the application might call for isolation from other grounds.

4.11. TLE2425 Current Source

TLE2425 Current Source

More Than 3 Decade Current Source

- OUTPUT CURRENT PROGRAMMED OVER 1000 TO 1 RANGE
- UNTRIMMED PRECISION:-
  - 0.75% ACURACY
  - 70 PPM/°C TEMP Co.
  - (R = METAL FILM, 0.25%)
- HIGH OUTPUT VOLTAGE SWING
  - 11 V to 0 V



TLE2425 : Enables precision and wide ouptut current range

TLC271 : CMIR includes GND low power consumption

Figure 2.4.10a. - TLE2425 Current Source

Due to is versatility, the applications of the TLE2425 are numerous. Although being ideal for maximising the performance of single rail 5 V applications, its accuracy and high output current make it well suited to function as a high performance current source.

The usual principles of making a current source are to fix a voltage across a resistor and either mirror that current or to buffer it. This can have problems in referencing the current source and finding op amps that can deliver the currents sometimes required.

The diagram above shows one simple way of doing this. The TLE2425 with its accurate reference and high output drive capability greatly simplifies the design.

The minimum drop-out voltage of the TLE2425 is 1.5 V placing the maximum voltage on the out of the TLE2425 at 13.5 V. This means that the maximum voltage on the common terminal of the TLE2425 will be 11 V. The feedback loop around the op amp means that the voltage at the inputs of the op amp will also be at 11 V.

The common mode input voltage range (V_{CMIR}) of the TLC271 extends from ground up to 1.5 V from the positive supply. Which means for a 15 V, the voltage swing of the current source is well within the common mode input range of the TLC271. To minimise the quiescent current of the whole current source, the TLC271 has its bias select pin (8) tied to the positive rail.

The accuracy of the system is limited by the accuracy of resistor, and by the input offset voltage of the TLC271 which will also be effected by its common mode rejection ratio. Both of the limitations due to the TLC271 could be improved by using the TLE2021, this, however, would limit the lower voltage range of the current source.

4.12. TLC2272Single Supply Sensor Interface

The increase in use of electronics in the automotive industry has brought about the need for single supply op amps, capable of operating from a +5V supply. The TLC2272 was designed for these applications, using a PMOS input stage gives the common-mode range down ground, while a push-pull CMOS output stage gives it an output swing includes both rails.

This application below, utilises all these features: interfacing to a piezoelectric pressure sensor used to sense knocking in an internal combustion engine. The first op amp is in a non-inverting configuration, making use of its high input impedance and its common-mode range down to the negative rail.

The piezoelectric sensor is an ac sensor and can be modelled by a voltage source in series with a capacitor. The sensor can be considered as working in two modes one as a sensors which produces charge or as a sensor which produces ac voltages. In this application the TLC2272 is amplifying the voltage produced by the sensor.

Interfacing to the sensor is a 1 MΩ resistor and a calibrating capacitor, this capacitor can be used to alter the high pass cut-off frequency of the sensor as well as affecting its gain. The shunt resistor is included to provide both a current path for any bias currents of the op amp and to provide a current path for any current flowing out of the sensor. In order not to load the sensor this shunt resistor needs to have a large resistance, and for this reason, the TLC2272 is ideal. No bipolar op amp has a high enough input impedance and more importantly, low enough bias currents to be able to interface with these resistors.

The first op amp acts as the sensor interface, and also doubles as a wideband filter amplifying the input signal plus filtering out signals which are not of interest. The second op amp in the TLC2272 is connected in a Delyiannis-Friend configuration producing a band pass filter, which is used to filter out all other signals.

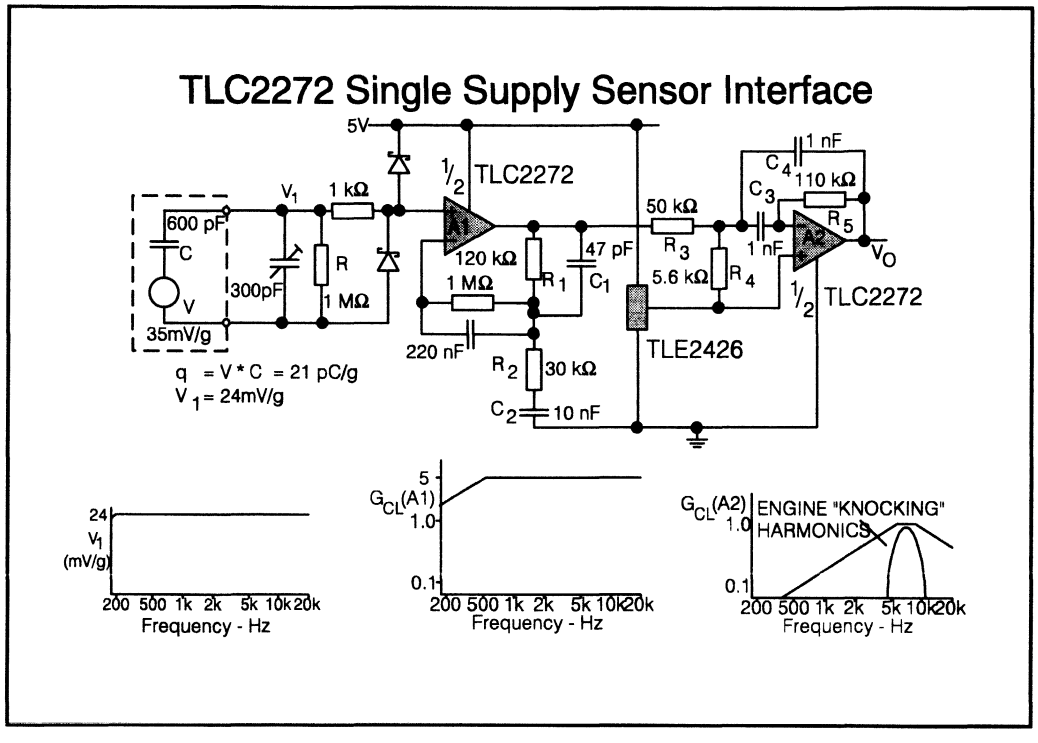


Figure 2.4.11. - TLC2272 Single Supply Sensor Interface

The advantages of this circuit is that all the filter's key parameters can be designed and decided sequentially, simplifying the design process. The input resistors act as attenuators bringing the gain of this filter to unity. The centre frequency of the circuit is determined by the feedback resistor, R_5, and the Thevenin equivalent of the input attenuation resistors R_{TH}

$$\omega_o = \frac{1}{C * \sqrt{R_5 R_{TH}}}$$

and

$$R_{TH} = \frac{R3 * R4}{R3 + R4}$$

The quality factor Q, (a measure the reactance to resistance ratio at the natural frequency of the filter, roughly speaking it is a measure of how steep the initial roll-off is) of the filter depends solely on the ration of the feedback resistor to the Thevenin equivalent of the input resistors.

$$Q = \frac{1}{2}\sqrt{\frac{R5}{R_{TH}}}$$

When engine knock starts to occur, the sensor will generate a range of signals, whose frequency is not present when the engine is running properly, which the second op amp is used to exclusively amplify. The characteristic knock frequency of the engine will change depending on the size of the cylinders and the cylinder block's material. To meet all these changes in frequency, a wideband sensor and a versatile op amp are required; most of these sensors have bandwidths into the tens of kilohertz, meaning that one form of sensor should suit almost all applications. The TLC2272 with a unity gain bandwidth of 2 M/Hz and an input offset voltage of 950 μV provides the accuracy and speed required by the system, without using capacitive coupling.

The rail-rail output swing also increases the system's dynamic range by enabling the TLC2272 to drive A-D converters to their full input range. This is helped by the TLE2426 virtual ground, which enables the TLC2272 to drive symmetrical loads. This example typifies a usual LinCMOS^{TM} op amp application requiring low bias currents and low quiescent currents whilst providing accurate signal conditioning.

4.13. Battery Powered Applications

A major problem with using batteries for power supplies is that the output voltage varies with the amount of current being removed from the cell; the series resistance of the battery is comparatively large. In order to have a minimum 5 V supply, 5 NiCAD batteries have to be used. From the initial full charge, the total battery voltage could be as high as 7.5 V. However, the nominal voltage for NiCAD batteries in use is 1.2 V which would equate to a 6 V supply. This is too high for 5 V digital electronics where the max. supply is specified at 5.25 V. Therefore, a fixed voltage regulator must be used to achieve the 5 V output.

Designers of portable, battery powered systems such as cellular telephones, laptop computers, hand-held voltmeters and portable sensor instruments for example have two main problem areas. These are extending the battery life of the equipment and reducing the products physical dimensions.

The battery life can be extended by three ways;

4.13.1. Low Drop-out voltage

For a linear voltage regulator, the drop-out point is reached when the voltage provided by the battery has degraded to such a low level that the regulator can no longer provide the correct regulated voltage. Reducing the drop-out point of the regulator extends the life of the battery by allowing the regulator to function longer from a lower input voltage. When the regulator enters its drop-out condition, the regulators quiescent current will increase due to the reduced current gain of the pass transistor. This is another reason for using regulators with an even lower drop-out voltage.

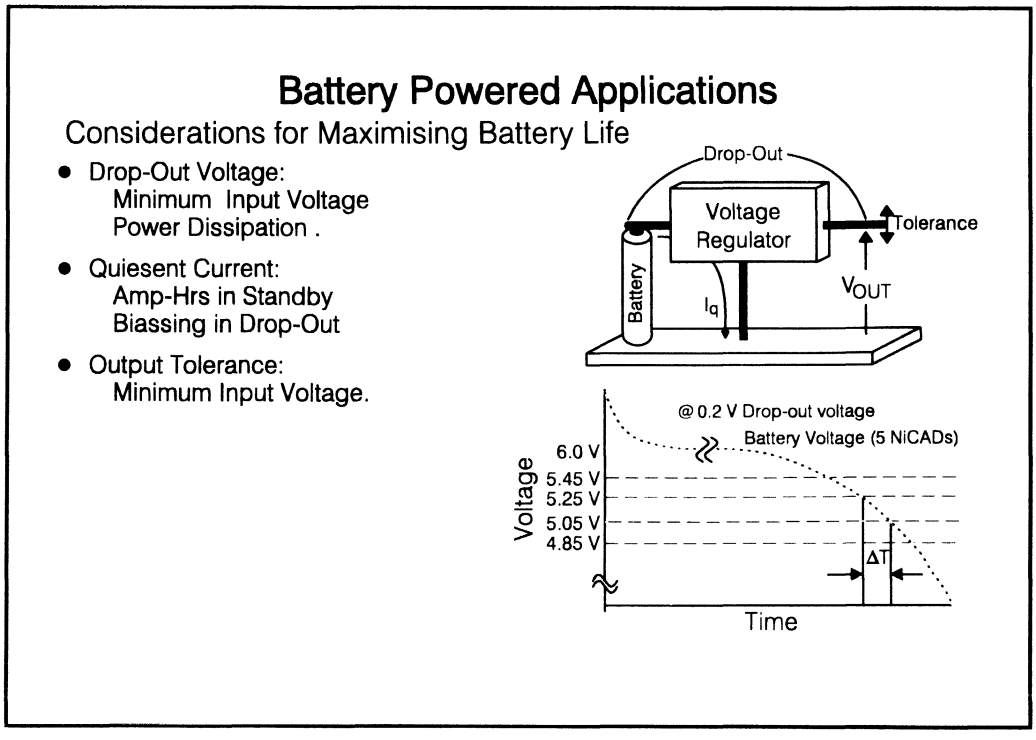


Figure 2.4.12. - Battery Powered Applications

4.13.2. Low power stand-by mode

To further extend the battery life of a portable system, the device should have a TTL or CMOS compatible enable pin that can be used to switch the device into a standby operating mode. This facility can be used to automatically power down the system when it is not in use so that battery power is conserved.

4.13.3. Lower supply voltage

Using an output voltage of 4.85 V instead of 5 V for a regulator can add to the battery life of a system. This is due to the TTL tolerance being between 4.75 V - 5.25 V. If the supply is operated at 4.85 V, the battery voltage can fall to a lower level while the regulator maintains a regulated output to the system.

4.14. Texas Instruments Low Drop-Out Regulators

In the past, all linear regulators were designed with a serial NPN pass transistor. The technologies used were developed to enhance the performance of the NPN transistor at the expense of the PNP transistor. This meant that the NPN transistors were very much faster and had very much higher current gains than their PNP counterparts. So for low noise and good line and load regulation NPN transistors had to

be used, but this meant that quite often minimum drop-out voltages of 2-3 V had to be allowed for. So a device providing an output current of 1 A had to be capable of withstanding a minimum power dissipation of 2-3 W. The drop-out voltages used would normally have to be much larger than this to allow for the poor regulation of the source, which means that the devices had to withstand a much larger power dissipation than 2-3 W.

The increase of low supply voltage applications and the increase of battery powered applications led to the development of serial voltage regulators that have much lower drop-out voltages. This has also come about with improvements in PNP transistors.

Normal voltage regulators have NPN transistors which require the base drive circuitry to be above the output voltage. It is fact that increases the drop-out voltage. The Low Drop-out Regulators using PNP transistors have the base drive circuitry below the output voltage, thus allowing a much smaller drop-out voltage.

Texas Instruments released its own family of Low Drop-out voltage regulators in the late eighties. These were aimed primarily at automotive applications, which was one of the driving forces behind low drop-out regulators. This is why the TL750/1L and TL750/1M families have 60 V load-dump protection specifications.

They can, however, be used in many other applications.

However one problem of LDO regulators is that large increases in quiescent currents can be observed at start-up or when the device is in its drop-out region.

4.15. TL75LPXX Family of Voltage Regulators

The increase of battery applications has made the low drop-out regulator essential for maximising battery lifetime. All batteries exhibit relatively large output resistance's, which increase with battery life span. Low drop-out regulators help to increase the lifetime of the battery by reducing the output impedance of the battery. The Low drop-out regulator's small drop-out voltage adds to this further by allowing greater voltage drops within the battery than what standard serial regulators were capable of.

Texas Instruments has recently introduced a family of fixed voltage regulators which have been specifically designed for battery powered applications. The key features of these devices are low drop-out and low power standby mode. Another key feature ot the TL75LPXX family is that all devices are available in the latest 20 pin TSSOP package. The TSSOP package is comparable to the SOIC package in surface area but only has a height of just 1.1 mm, and so allows high density applications to be achieved on the PCB.

The drop-out voltage for the TL75LPXX family is typically 220 mV @ 300 mA of output source current. This drop-out voltage falls to a typical of just 120 mV @ 100 mA of output current. The absolute maximum drop-out of the TL75LPXX family of devices is just 400 mV sourcing 300 mA This is the lowest drop-out voltage that Texas Instruments at present manufacture.

The TL75LPXX has an enable/disable pin which places the output part of the voltage regulator into a high impedance state. In this condition, the voltage regulator will only consume a typical current of 100 µA. The absolute maximum that Texas Instruments will guarantee is 150 µA The standby mode is TTL and CMOS compatible which makes it suitable to be controlled by virtually any digital system.

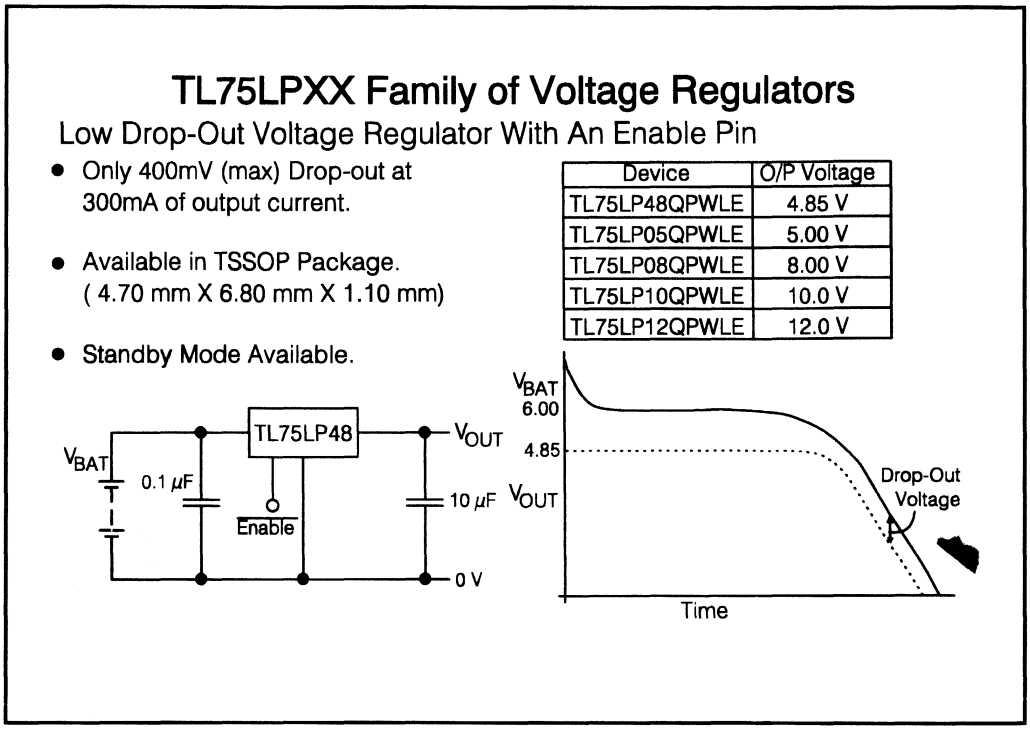


Figure 2.4.13. - TL75LPXX Family of Voltage Regulators

4.15.1. 4.85 V

There is a voltage option of 4.85 V available in the TL75LPXX family of voltage regulators. This increases the battery life of the system by letting the input voltage drop further before the regulator goes out of regulation The TL75LP48 is specified at 4.85 V, and the 2% (max.) tolerance of the voltage regulator gives a minimum output voltage of 4.75 V which is the minimum supply voltage for TTL.

4.15.2. Decoupling Capacitance

The input and output capacitance loading is important to the performance of any low drop-out voltage regulator. The capacitance values and equivalent series resistance (ESR) affect the control loop of the device and therefore must be defined for the load and temperature range

The TL75LPXX Family of voltage regulators only require a minimum input capacitance is 0.1 µF, and a minimum output load capacitance of 10 µF. This saves both board space and height compared to the more common 100 µF load capacitors required by most other similar voltage regulators. The reduction in the load capacitance value will also benefit in a reduction in component cost.

Texas Instruments is committed to designing new voltage regulators for the battery market with even lower drop-out voltages and standby currents

4.16. Moving from 5 V to 3 V Supplies

"The World is moving to 3V" but is it really? The majority of analogue designers are actually asking themselves what the benefit is of this new 3V World, and in reality it is only one thing - power consumption.

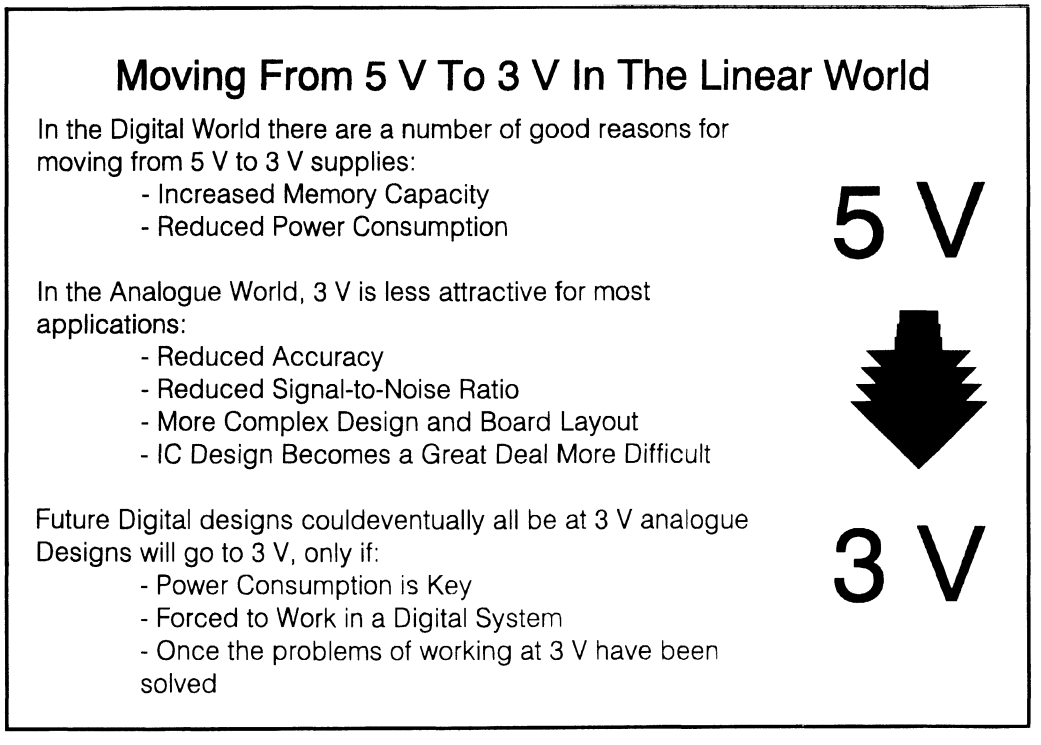


Figure 2.4.14. - Moving from 5 V to 3 V in the Linear World

There are a number of reasons why moving to 3V is attractive for the digital system. From a technology standpoint, low voltages enable smaller transistor geometry's which permit higher density technologies (particularly for 64 MByte DRAMS and beyond) and faster circuits. When combined with lower power consumption it is obvious what digital systems such as portable computers have to benefit form moving to three volts.

Analogue Designers see only problems with this new power supply standard. Many designs still have yet not progressed to single +5V supplies as dual +/-15V offers many advantages. Linear circuits are essentially used to capture and condition a signal, to convert it into or from a digital signal and provide output drive into loads such as motors and audio speakers. Moving to lower voltages merely makes these tasks more demanding, as the accuracy of a systems is reduced due to less dynamic range (1mV is 12 bits in a 5V systems, and is 11 bits in a 3V system) and a reduced signal to noise ration (the noise floor remains the same). In amplifiers, the common mode input range is reduced, making it more

difficult to interface to a sensor, and the output needs to deliver the same power (if not more) from a reduced supply.

As systems demand higher accuracy, reducing supply rails merely makes life more difficult. There are a number of system design issues which need to be overcome before analogue designs can achieve the same levels of performance as they do today.

4.17. 3 V Implications for Op Amps

Not only is system design more difficult at these lower supplies, lower voltages also place extra demands on the IC designer.

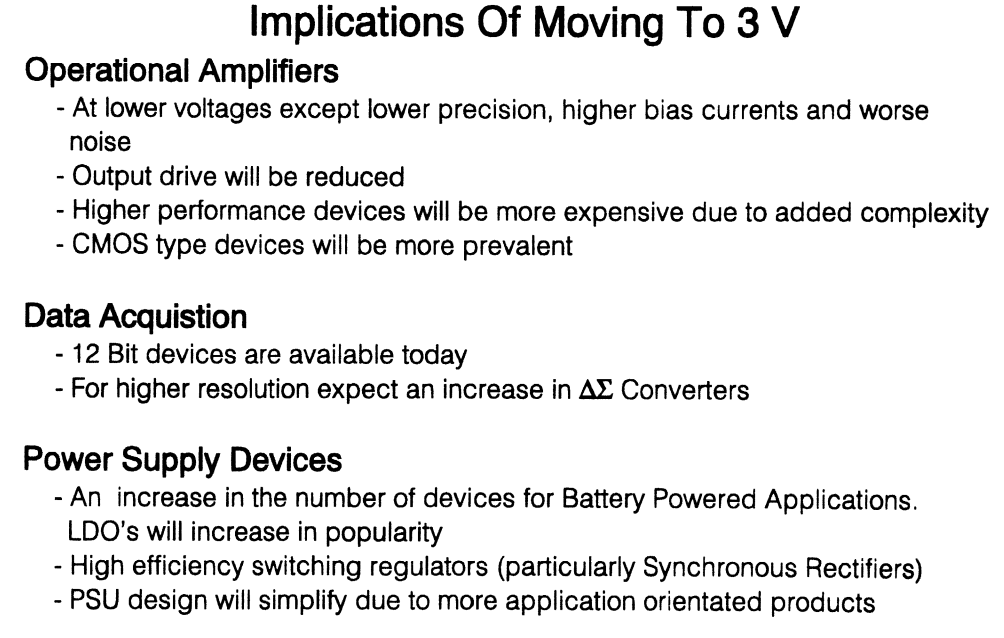


Figure 2.4.15. - Implications of Moving to 3 V

If we consider bipolar technology, one 'Vbe will always one Vbe'. With a typical value of 0.7V (even higher at lower temperatures), there is not much headroom to design complex functions. Most bipolar op amps share common design techniques to achieve certain characteristics, and reducing the supply voltage prohibits using these methods. For instance, the most common technique for implementing 'bias-current-cancellation' in an op amp simply will not operate from a 3Vsupply. Similar problems occur in achieving low offset voltages without trimming, in attaining high gains and low noise figures

and also in realising an output stage with high drive. IC designers need to so some work to achieve the same performance at 3V as they do today at 5V and above.

There are in fact a handful of bipolar amplifiers that are designed to operate at 3V (and even below). These devices offer a combination of low voltage and low power, but they are very complex designs. Multiple transistors have been used to achieve the required performance and as a result the parts are expensive.

CMOS is a much better technology for low voltage operation. Because Vt's can be 'tweaked' for optimal operation, there is much more flexibility in the design. CMOS though has inherent trade-offs for Linear applications, and has a long way to go before it can achieve the noise and offset voltage of precision bipolar part.

In areas other than operation amplifiers, there are some circuits that are more designable at lower voltages. Digital type circuits such as data acquisition devices are already available at 3V, and for D/A converters, lower supply voltages do not cause as big a problem. For higher than 12 bit resolution, more ADC's will be using Delta-Sigma techniques to meet the low voltage requirements of low frequency applications.

Three volt design has really spurred the growth of power supply products. The drive for battery operation has forced designers to look for ways to increase the operating time of their system - a problem which has been passed directly onto the power supply designer. The 3V revolution has caused a significant increase in both Linear (specifically low drop out), and switching regulator circuits to improve the system efficiency. IC manufacturers are also offering ready-made solutions to the often difficult design problems facing a typical switching power supply designer.

More complex battery powered systems also contain 'Power Supply Management' circuits. Load management is used to switch on and off different loads to conserve power, and special battery charges and monitoring devices help ensure maximum operating life from the battery. All this effort in the power supply area is good for the end user as more alternatives will be available and circuit design will hopefully simplify.

Wide spread three volt design is imminent for digital circuits and will one day happen for analogue. To speed up the arrival of this Linear design, it is necessary for both the IC and System Designer to overcome some inherent difficulties. Both groups are actively working in this area

4.18. 3 Volt Linear Product Family

In 1983, to meet the growing need for low voltage operation op amps T.I. introduced its TLC range of op amps. These devices are specified for 5 V and 10 V supply voltage operation. However as discussed above, with growth of portable equipment powered from batteries and to meet the needs of lower supply voltage logic there is now a need for op amps (and comparators) capable of operating from +3 V.

To meet this need, T.I. has introduced its Texas Linear Low Voltage (TLV) range of LinCMOS op amps. These are devices specifically aimed for low voltage operation. It is for this reason that they have been characterised for operation at both 5 V and at **3 V**. All members of the family are capable of operating from a minimum supply voltage of 2 V over the whole industrial temperature range of -40°C to +85°C, so increasing their versatility further.

As with all T.I.'s LinCMOS op amps their common-mode input range extends down to the negative rail as do their outputs.

3 Volt Linear Product Family

TLV23XX Family of 3 V Operational Amplifiers and Comparators

- Fully Specified and Characterised at 3 V and 5 V Supplies
- Minimum Supply Voltage of 2 V
- Common-Mode Input Range Extends From 0 V to V_{CC}-1 V (25°C)
- Output Swings Down to 0 V
- Available in DIP, SOIC and TSSOP

3 V Comparators				
Device		I_{CC}(μA)	V_{IO} (mV)	Response Time (ns)
Dual	TLV2352	120	5	640
Quad	TLV2354	250	5	640

3 V Op Amps					
Device		I_{CC}(mA)	V_{IO} (mV)	SR (V/μs)	UGBW (MHz)
Single*	TLV2341	0.017, 0.25, 1.5	8	0.02, 0.4, 2.1	0.03, 0.3, 0.8
Dual	TLV2322	0.034	9	0.02	0.03
	TLV2332	0.5	9	0.4	0.3
	TLV2342	3.0	9	2.1	0.8
Quad	TLV2324	0.068	10	0.02	0.03
	TLV2334	1.0	10	0.4	0.3
	TLV2344	6.0	10	2.1	0.8

*Programmable

Figure 2.4.16. - 3 Volt Linear Product Family

Figure 2.4.16 contains a table showing their capabilities. The LinCMOS op amps, as usual, offer a good speed-power compromise over the entire product range, from the micro-power devices to the higher speed devices. - Even when operating from a 3 V supply, the speed of the TLV234X is still comparable to that of the uA741 which is incapable of operating at 5 V let alone 3 V.

The versatility of these devices is expanded yet further by the choice of 3 plastic packages. All members are available in the standard dual-in-line packages as well as the standard small outline package. However all members are available in the new Thin Shrink Small Outline Package (TSSOP), which is attracting wide interest due to its extremely large savings in terms of board space area and its very small height, nominally just 1 mm. This makes the devices even better suited to portable systems.

4.19. 3 V Micro-Power Sensor Interface

One of the major application areas for 3 V op amps will be in the handheld or remotely powered sensor/metering areas. In these applications battery lifetime will be of prime consideration.

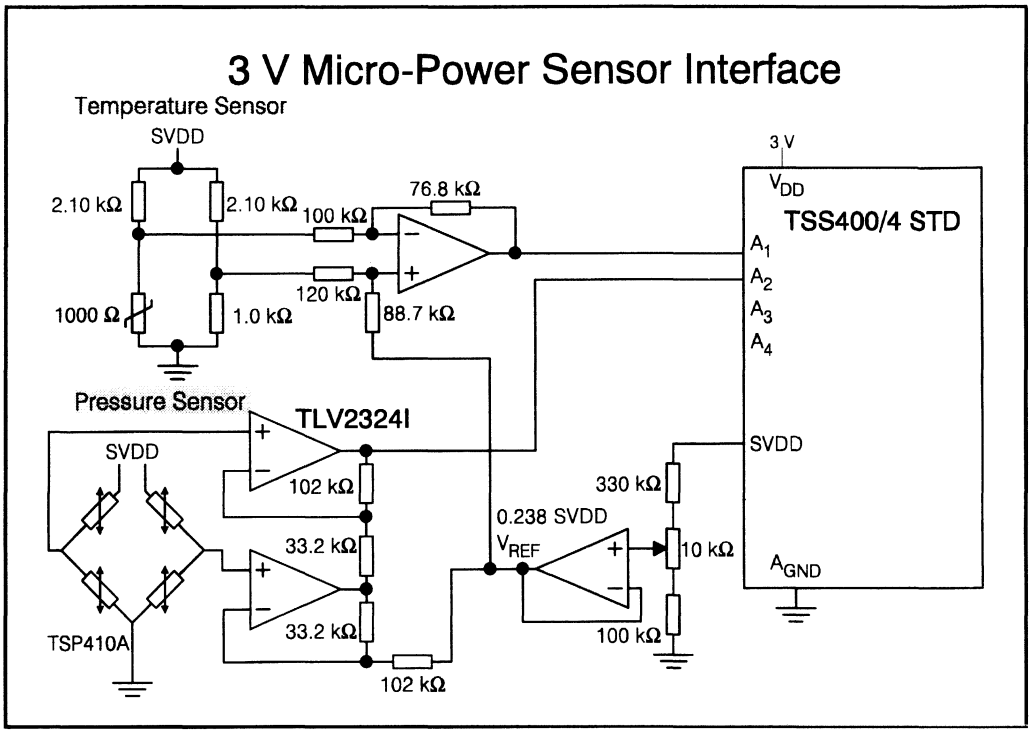


Figure 2.4.17. -3 V Micro-Power Sensor Interface

The application shown in figure 2.4.17 shows the TLV2324 amplifying the output voltage of a temperature sensor and a pressure sensor. This could be used in a an application where the volume of gas would want to be measured.

The output of the op amps is then fed to the TSS400/4 , Texas Instruments Sensor Signal Processor. The TSS400 contains its own CPU and 4 multiplexed analogue inputs which feeds to an on-chip 12-bit ADC.

The ADC of the TSS400 makes ratiometric conversions based on its output voltage SVDD. By turning on SVDD only when measurements are to be taken the overall power consumption of the whole system can be significantly reduced.

The first op amp is used to act a reference buffer, which buffers a proportion of SVDD. This is used to set the minimum input voltage of the analogue inputs to the TSS400's ADC. Which in this case is equal to 0.2380*SVDD.

The second and third op amps are used to amplify the output of the pressure sensor, which is powered by SVDD. This results in the output of the pressure sensor being relative to SVDD, so that any variance in SVDD will be cancelled out by the ADC.

The gain of the two op amp differential amplifier configuration is set to give a maximum output voltage of 0.4008*SVDD. This is equal to the maximum input range of the TSS400's ADC.

The fourth op amp is configured as single stage differential amplifier, the high input impedance and low input bias currents enable the TLV2324 to use large feedback and source resistor without increasing the offset voltage of the op amp while minimising the loading on the temperature sensor bridge.

The sensor bridge uses a 2.1 kΩ biasing resistor to cancel out the exponential temperature-resistance characteristics of the silicon sensor. This gives the output of the fourth op amp a near linear output voltage versus temperature characteristic.

Once again the resistor values and the reference voltage has been used to set the voltage range of the fourth op amp to the ADC's input range.

The ideal gas law relates the volume, pressure and temperature of a gas as:-

$$\text{Constant} = \frac{n * P * V}{T} \quad \text{..... Where n is a constant relating to the gas.}$$

This can be a more accurate way of measuring the amount of gas consumed in domestic applications.

4.20. Texas Instruments Switching Regulators

One early monolithic form of switching regulator to be released onto the market was Texas Instruments' TL497. This is a simple and easy to design-with Pulse Rate Modulation (PRM) Controller Integrated Circuit, and as a result, has proved very successful. It, however, suffers from the problem, common to all PRM controllers, of enormous variation in oscillation frequency with load. At light loads the frequency can drop into the audible frequency range. More modern Switching Regulators use Pulse Width Modulation (PWM) Control.

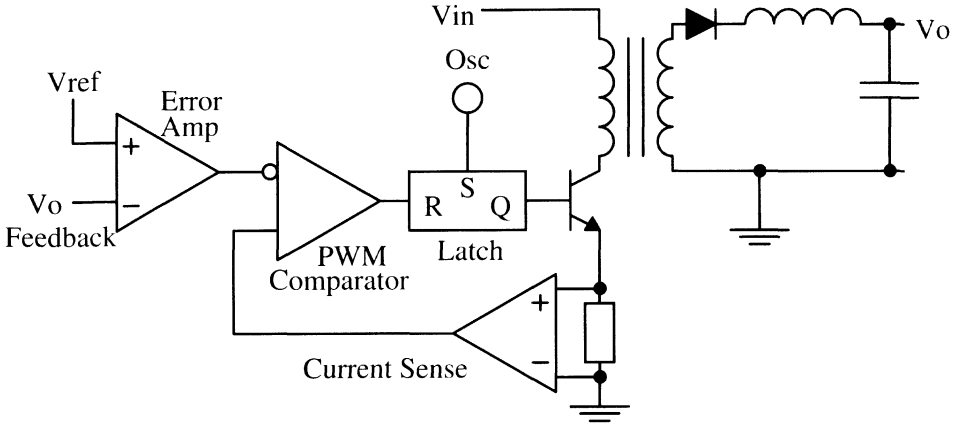
One of the first monolithic switching regulators to be released onto the market that used PWM was Silicon General's SG3524 family. Texas Instruments introduced its own version of that popular regulator along with its own TL493/4/5 family. These allowed higher switching frequencies and greater drive capabilities. The TL493/4/5 family was superseded by the TL594/5 family of switching regulators which had the added feature of under voltage lockout.

Both families could be used to switch the load inductor (transformer) directly, or for heavier loads provide pre-drive for power switches. The TL594/5 family has recently had a new addition with the TL598. This uses two Totem-Pole output stages. whereas the previous members had two un-configured output stages. This enables the TL598 to act as a better pre-driver for the power switches.

4.20.1. Current Mode Control

A more recent innovation in Switching regulators is to use current mode control. This still uses PWM techniques, but now the current flowing through the power switch is also monitored and used to modulate the on-time of the switching regulator. This in effect uses a dual control loop, with the inner loop being the current control. The current flowing from the input through the inductor and the output power transistor, when it is switched on, is converted to a voltage by a low valued sense resistor. This provides direct feedback of the current flowing through the inductor.

This signal is fed back to the PWM comparator, where it is measured against the error signal generated by the outer loop. This loop compares a fraction of the output voltage to an internal reference and provides an error signal in proportion to the difference between the desired and actual output voltage. This error signal is the same as is used in normal voltage mode converters.



In this way, the drive to the output switch from the latched flip-flop is turned off when the sensed inductor current reaches the limit set by the V_{ERROR} signal. Hence, the error signal controls the inductor current directly to provide inherent pulse by pulse current limiting.

Benefits of current mode control

Direct sensing of load current - Because the load current is measured directly and not just the load voltage, the current mode controller can respond very quickly to variations in the load. This is also true for changes in the input voltage.

Current compared to error signal - Measuring the current directly shuts off the output in a short circuit condition or if the inductor saturates.

Parallel Operation - Since both current and voltage are monitored, power is shared equally between any number of modules operating in parallel. This makes efficient use of a series of devices operating in parallel to provide additional current capacity.

Feed Forward - Variations in the line voltage are automatically corrected for by the current sense amplifier, as explained above. Therefore, the dynamic range of the error amplifier is used to maximum effect to measure load variations.

The range of current mode controllers are listed below:-

Without Power Switch	With Power Switch
UC3842	LT1070
UC3843	LT1071
UC3834	LT1072
UC3844	

4.21. LT1072 Fly-Back Converter

The LT1072 is a monolithic, high efficiency switching regulator. It can be operated in most standard switching configurations including step-down (buck), step-up (boost), fly-back, forward, and inverting.

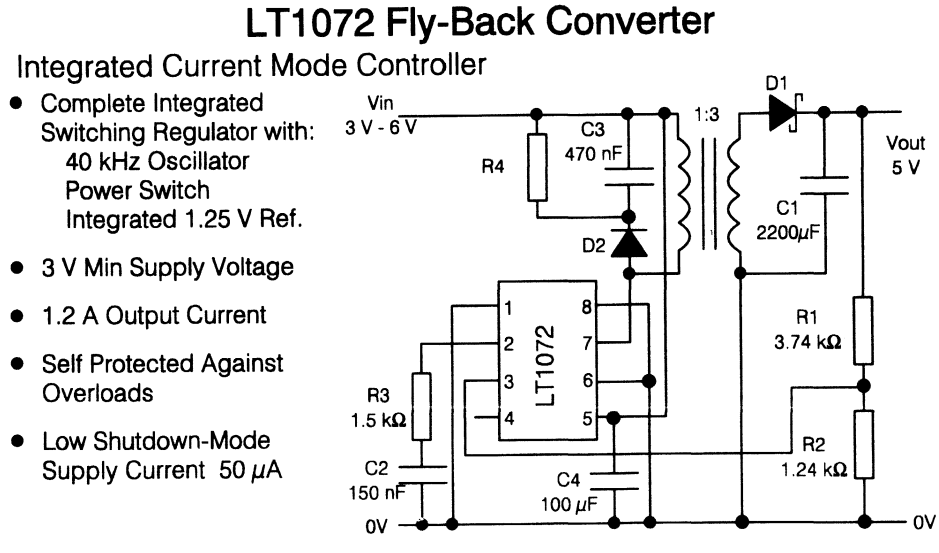


Figure 2.4.18. - LT1072 Fly-Back Converter

Figure 2.4.18 shows an application using the LT1072 in the fly-back configuration. Fly back converters are able to regulate the output voltage either higher or lower than the input voltage. This is accomplished by the use of a transformer The transformers function is to transfer energy from the input to the output. As the LT1072's power transistor switches on, the energy builds up in the core due to the current flow in the primary winding. When the power transistor switches off, the energy stored in the core is transferred to the secondary windings and current is delivered to the load. The current in the secondary just after the power transistor switching off is equal to the reciprocal of the turns ratio (1/N) multiplied by the current in the primary. The output voltage of the flyback converter is not constrained by input voltages as in the Buck or Boost converters.

$$Vout = \left(\frac{SDC}{1-SDC} N \bullet Vin\right)$$

Where SDC = Switch Duty Cycle $= \dfrac{Vout}{Vout + N * Vin}$

N = Transformer turns ratio

By adjusting the duty cycle from between 0 and 1, the output can, in theory, be set anywhere from 0 to ∞. However, the output voltage is limited by the power transistor breakdown voltage. The snubber network is a clamp circuit which has been designed to protect the LT1072's power transistor from over voltage spikes. The maximum output voltage is limited to:-

$$V_{OUT(MAX)} = N(V_M - V_{SNUB} - V_{IN})$$

V_{SNUB} = snubber voltage

V_M = maximum allowed switch voltage

This still allows the LT1072 to regulated output voltages of hundreds of volts by using large values of transformer turns ratios. In many applications, the turns ratio can vary over a wide range without degrading the performance However, if maximum output power is desired, the turns ratio can be optimised.

$$N_{(OPT)} = \frac{(V_{OUT} + V_F)}{V_M - V_{IN(MAX)} - V_{SNUB}}$$

V_F = forward diode voltage of D_1

A second important transformer parameter which must be found is the primary inductance (L_{PRIME}). For maximum output power, the primary Inductance should be high to minimise the magnetising current, but this can lead to very large core sizes. A reasonable design approach is to reduce the value of the primary inductance to the point where the primary magnetising current (ΔI) is about 20% of the peak power transistor switch current

$$L_{PRIME} = \frac{(V_{IN} * V_{OUT})}{\Delta I * f(V_{OUT} + N * V_{IN})}$$

ΔI = 20% peak current

f = Switching frequency (40 kHz)

The maximum output current is a function of the maximum peak current that the output power transistor can switch. The efficiency come from the losses in the snubber network, LT1072 losses in the switch, the output diode, the LT1072 driver and the transformer.

$$I_{OUT(MAX)} = \frac{\eta\left(I_{PEAK} - \frac{\Delta I}{2}\right) * V_{IN}}{N * V_{IN} + V_{OUT}}$$

I_{PEAK} = max LT1072 switch current (1.25 A)

η = overall efficiency > 75%

In order to choose the correct inductor core size, the peak primary switching current needs to be found. This can be calculated using the following formula;

$$= \frac{I_{OUT}}{\eta}\left(\frac{V_{OUT}}{V_{IN}} + N\right) + \frac{V_{IN} * V_{OUT}}{2 * f * L_{PRIME}(V_{OUT} + N * V_{IN})}$$

The Output divider resistor network needs to be calculated for the feed back voltage to the LT1072 switching regulator. This can be calculated as follows;

$$R_1 = \frac{(V_{OUT} - V_{REF})}{V_{REF}} R_2$$

$$V_{REF} = 1.244\ V$$

$$R_2 = 1.24\ k\Omega$$

The fly back converter requires a clamp circuit to protect the output power transistor from over voltage spikes. These over voltage spikes are created by the leakage inductance of the transformer. The leakage inductance is modelled as an inductor which is in series with the primary winding and this inductance is not coupled to the secondary windings. During the power turn on time, the current that is in the leakage inductance is equal to the peak primary current (Iprime). When the output power transistor turns off, the energy stored in the leakage current ($E = 0.5 * I^2L$) will cause the voltage to increase. It is therefore important to clamp this voltage. A zener diode can be used to clamp this voltage and is selected by using the maximum input voltage and the maximum output switch voltage.

$V_{ZENER} = V_M - V_{IN(MAX)}$. The Zener diode has a maximum power rating which should not be over exercised. This can be calculated as

$$P_{ZENER} = \frac{V_Z * I_{PRIME}^2 * L_L * f}{2\left(V_Z - \frac{V_{OUT} + V_F}{N}\right)}$$

The LT1072 switch voltage will show a narrow spike extending above the snubber clamp voltage. This spike is caused by the slow turn-on time of the zener diode in series with the diode in the clamp circuit. This diode should be a fast turn-on diode such as a schottky diode. The diode must be rated to handle the peak current of the primary current (Iprime) and a reverse voltage rating of at least Vin(max).

Alternatively, an RC type circuit could be used for a clamping circuit. One disadvantage is that the RC network will dissipate power even under no load conditions. RSNUB can be found from

$$R_{SNUB} = \frac{2\left(V_R^2 - V_R * \frac{V_{OUT}}{N}\right)}{I_{PRIME}^2 * L_L * f}$$

V_R = voltage across the snubber resistor

The value of C3 is not critical, but it should be large enough to keep the ripple voltage across the snubber to only a few volts

$$C_3 = \frac{V_R}{R_{SNUB} * f * V_S}$$

V_S = voltage ripple across C_3 ($\approx 3V$)

Flyback converters do not use the inductance of the transformer as a filter, so an output capacitor C_1 is used to do the filtering. The capacitor size depends on the amount of ripple voltage that can be allowed on the output. The ESR (effective series resistance) of the capacitor is an important factor when considering the value of capacitance as the formula below shows. Alternatively, an LC output filter can be added to the output to reduce the ripple voltage on the output. Typical values of this filter would be L_1 =10 µH, C_5 = 200 µF.

$$V_{P-P} = \frac{Iout}{f * C_1\left(1 + \frac{N * Vin}{Vout}\right)} + (ESR) * Iout\left(1 + \frac{Vout}{N * Vin}\right)$$

4.22. TLV2217-33 LDO Voltage Regulator

TLV2217-33 Voltage Regulator

3.3 V Low Drop-Out Fixed Output Voltage Regulator

- Meets the new 3.3 V JEDEC Standard.
- Available in the New TSSOP Package.
- 500 mV (max) Drop-out Voltage.
- 500mA (max) Output Current.
- 2% (max) Output Tolerance

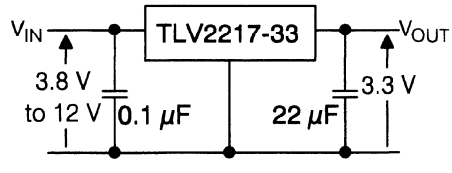


Figure 2.4.19. - TLV2217-33 Voltage Regulator

The move to 3 V supplies has been discussed in 4.16 and 4.17. There are, however, two "3 V" standards one for 3 V applications and the other for 3.3 V applications. The 3 V standard is, at the time of writing this, still under review. The 3.3 V standard has full JEDEC approval.

With response to this new 3.3V standard, Texas Instruments designed a new low drop-out 3.3 V fixed output voltage regulator named the TLV2217-33 This was specifically designed to meet the new 3.3 V JEDEC standard. The TLV2217-33 has a maximum drop-out voltage of 500 mV while sourcing 500 mA of output current. Because the drop-out voltage is low, the minimum input voltage can be 3.8 V which makes it suitable for running off existing 5 V supplies. This enables the device to be designed into the mixed supply systems which are being designed at present.

The device is available in the new 20 pin TSSOP package for high density applications. The package is comparable to the surface area of the SOIC package, but only has a height if just 1.1 mm high. The output tolerance is 1% at Tj=25 °C which guarantees an accurate output voltages to be achieved. The TLV2217-33 requires input and output decoupling capacitors to make the voltage regulator stable. The minimum input capacitor value is 0.1 µF while the minimum output value being 22 µF At present, the alternative solution is to use a variable voltage regulator whose output can be adjusted to 3V. The disadvantage of using a variable voltage regulator is the amount of external component required. Two resistors which are decoupled must be used as the feedback network to the Vreg. Most variable voltage regulators on the market do not have low drop-out voltage when sourcing high output currents. This can render the voltage regulators unsuitable for operating off existing 5 V supplies.

5. High Temperature Devices

5.1. High Temperature Process

In a number of engineering sectors, there is an increase in direct transducer signal conditioning. This can subject the signal conditioner to the extremes in temperature, stress and pressures. Some of the largest problems to which op amps are subjected is elevated ambient temperature operation.

In automotive applications, this can involve direct cylinder block mounting, while industrial applications may require the op amps to be mounted on the vessel containing the process. In the past, this would have involved using expensive hybrid devices in ceramic packages.

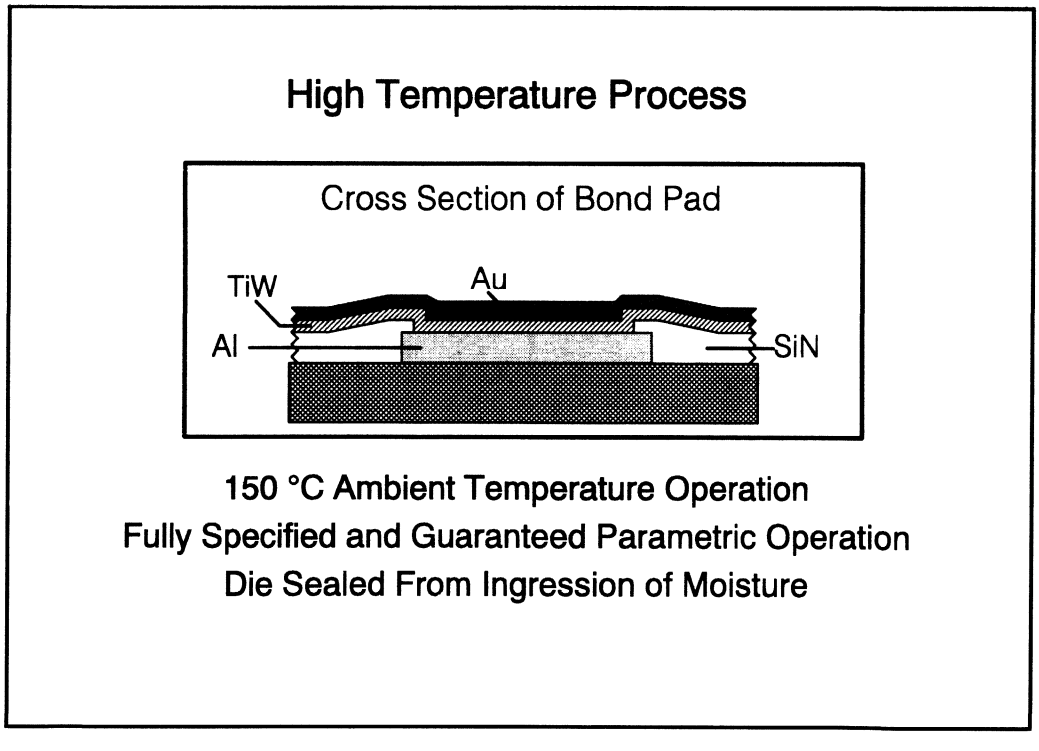


Figure 2.5.01. - High Temperature Process

Plastic packages have, for a long time, suffered great reductions in reliability when subjected to high temperatures for great periods of time. This has been due to several factors of the package and bonding.

5.1.1. Integrated Circuit Process

An integrated circuit will normally have all the silicon covered with Silicon Nitride. This has two main functions, one is to protect the surface from external effects, while the other is to protect the die from moisture ingression. There must, however, be holes in the silicon nitride to enable the bond wire to connect the silicon to the outside world. These holes in the silicon nitride can now let moisture into the silicon.

Plastic packages will normally let much more moisture into the integrated circuit than ceramic packages. This has led to plastic packages being rarely used in harsh environments. Texas Instruments' high temperature process now enables hermetically sealed devices to be produced in a plastic package.

5.1.2. High Temperature Process

The bond wire material used plastic packages is normally Gold, which is bonded to Aluminium pads on the silicon die. At high operating temperatures the bond between the Aluminium pad and the Gold wire can degrade. This can be due to the growth of mechanically weak purple coloured Gold-Aluminium intermetallic layers, and a diffusion driven voiding mechanism known as "Kirkendall Voiding". This degradation is commonly known as "Purple Plague".

The process used for high ambient operating temperature devices involves depositing and patterning Titanium-Tungsten and Gold layers over the bond pad areas. The Titanium-Tungsten layer provides good adhesion to the Aluminium pads and Silicon Nitride overcoat. The Titanium-Tungsten layer also acts as a barrier between the Aluminium and Gold layers, this results in the Gold wire bonds being made to a Gold layer rather than an Aluminium layer. So eliminating the inter-metallic and voiding problems at high ambient operating temperatures.

With the development of this process Texas Instruments has now released the TL2828, TL2829, TLC2801 and TLC2872 devices whose performance is fully specified for operating in ambient temperature ranges up to 150°C.

5.1.3. High Temp Process Qualification

Any new product (and process) must go through a qualification process. This is to make sure that the device is reliably manufacturable. Due to the very harsh nature of the environment in which these products are to be used, and that it is a new process, the qualification procedure for the first op amp, TL2829, was very thorough - far in excess of any other linear design.

The table below shows the qualification performed on the TL2829 op amp.

TEST	CONDITIONS
Steady State Life	155°C for 5000 hours with bias.
Autoclave	121°C for 2000 hours without bias at 15 psi and 100% humidity.
Temperature Cycle	-65°C to 150°C for 5000 cycles.
Storage	170°C for 3000 hours.

Throughout all these extended tests, no failures occurred, which is impressive for any product, and highlights the outstanding reliability of Texas Instruments' high temperature op amps.

5.2. High Temperature Bipolar Op-Amps

TL2828/9 Dual and Quad 150°C Op Amps

- Free-Air Operating Temperature Range
  -40°C to 150°C
- Low Input Offset Voltage
  7 mV (max) @ 25°C
  10 mV (max) full range
- Wide Range of Supply Voltages :
  Single Supply . . . 4 V to 30 V
  Dual Supply

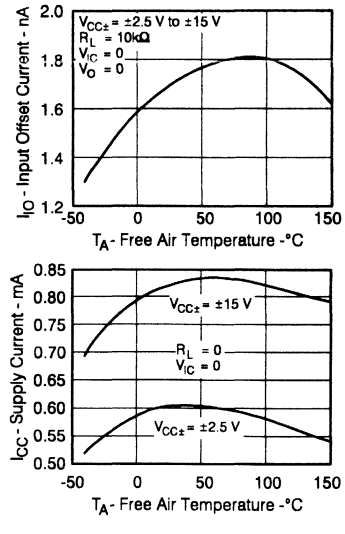


Figure 2.5.02. - TL2828/9 Dual and Quad 150°C Op Amps

The TL2828 and TL2829 were the first in a series of very high temperature op amps from Texas Instruments. They are, at present, the only readily available standard monolithic integrated circuit operational amplifier capable of functioning at ambient temperatures of 150°C.

Texas Instruments now has another temperature range group, the smallest being the commercial temperature range, denoted by C. The next range is industrial denoted by I, which extends from -25°C (some devices operate from -40°C) to 85°C. The military temperature range goes from -55°C to 125°C and is denoted by M. Most of Texas Instruments voltage regulators will have a special Q temperature range which specifies the operating junction temperature range instead of the ambient temperature range, this extends from -40°C to 125°C.

The TL2828 and TL2829 are the first devices to operate over the Z temperature range which goes from -40°C to 150°C.

Both devices are single supply op amps capable of operating from a 4V supply up to a maximum of 30V. The supply current of the TL2829 is only 1.2 mA at a 5V supply over a whole temperature range for all four op amps.

The density of op amps and low quiescent power, adds to its capabilities of functioning at very high ambient temperatures.

5.3. High Temperature Precision Op Amp

The TLC2801 was the third High temperature op amp to be released by T.I.. It combines the 150°C operating temperature range with very low offset voltages. The guaranteed maximum is just 1.5 mV even at 150°C.

This gives it an offset error of just under 12 bits!, and is provided from a single 5 V supply. Added to this its large open loop gain. The gain of the device still remains greater than 50000 even at 150°C. This greater than a lot of op amps can provide even at 25°C. The curve in figure 2.5.03 shows how the open loop gain varies with temperature, clearly showing the consistency of the high gain even at the high temperature extreme.

The low offset voltage and high are just two factors which make this device ideal for high temperature applications.

The low bias currents allow the TLC2801 to directly interface to high impedance sensors. When this is coupled to the high ambient temperature range of the op amp, it makes the TLC2801 just about the only op amp capable of being directly mounted at the sensor output and still provide high accuracy reliable data.

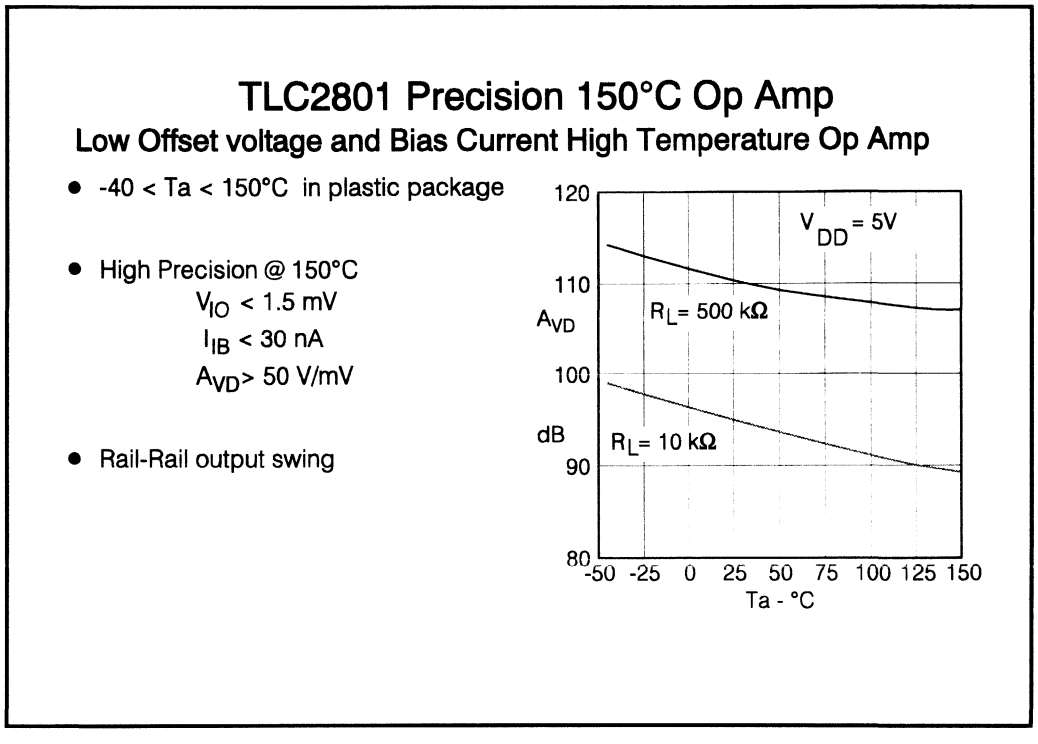


Figure 2.5.03. - TLC2801 Precision 150°C Op Amp

5.4. High Temperature Rail-Rail Op Amp

The TLC2872 is the latest addition to the T.I. high temperature range of op amps. It combines the 150°C capabilities of the process with a dual op amp with rail-rail outputs. This enables the device to maximise the dynamic range by allowing its outputs to swing to within milli-volts of both supply rails.

This allows the device to be mounted at the sensor output, enabling the signal conditioning to be completed there. This means that signal to noise ratio should be increased. In the past the output of the transducer would have to be fed to the signal conditioning section via noisy lines that are susceptible to interference from motors and other sources. By doing the signal conditioning at the sensor output, its output will raised above the noise floor, reducing the impact of the switching noise.

TLC2872 150°C Rail-Rail Output Op Amp

Wide Output Swing High Temperature Op Amp

- -40 < T_a < 150°C in plastic package
- Good Accuracy @ 150°C
  V_{IO} < 3 mV
  I_{IB} < 5 nA
  A_{VD}> 10 V/mV
- Rail-Rail output swing

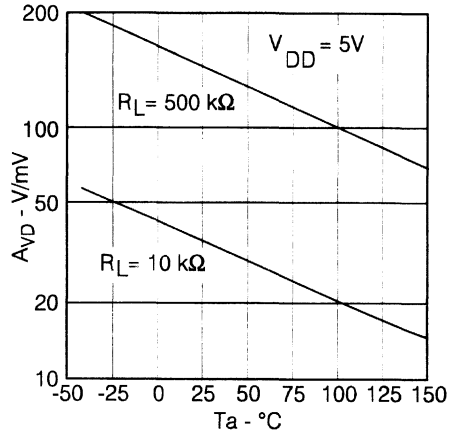


Figure 2.5.04. - TLC2872 150°C Rail-Rail Output Op Amp

Added to the rail-rail performance at 150°C is the large stability in offset voltage. The TLC2872 offers a maximum offset voltage of 3 mV at 150°C, while the bias currents have risen to only 3 nA. In addition to the very low input errors, the TLC2872 still offers a very high open loop gain, greater than 10000, even at 150°C. The curve in figure 2.5.04 shows how the gain varies with temperature.

6. System Protection

6.1. System Protection

Most systems at some time of their life will be subjected to some form of overstress. This stress can come at any time, even during assembly as well as during the system's lifetime in normal operation.

This means that both the devices themselves as well as the system may require some form of protection.

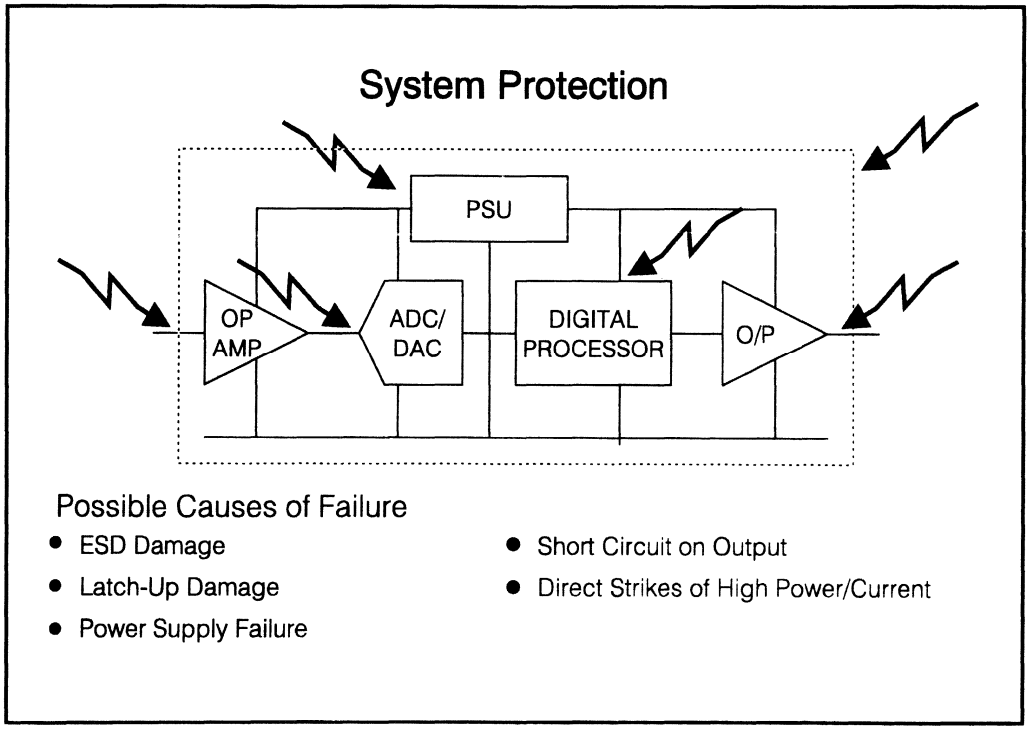


Figure 2.6.01. - System Protection

6.1.1. Electrical Overstress

Device failure can quite often be caused by electrical overstress; this can occur on the inputs, outputs and also on the supply pins. One common cause of electrical overstress is Electro-Static Discharge (ESD). When you walk from one place to another place charges will be constantly be removed and replaced onto your body, this can lead to a build up of charge on your body. The total voltage that can build up can reach kilo-volts, so when your body is discharged onto an integrated circuit a large voltage and large current can be discharged into the device.

6.1.2. Latch-up

The electrical overstress can also lead to latch-up. If the current generated is large enough to trigger a parasitic SCR then a direct short can appear across the supplies which can lead to the device being blown up. Other causes of latch-up can be due to the influences of electro-magnetic components which can either large currents to flow into the device or can cause voltage pulses with very large rate of change of voltages to be applied. Both of which can cause the parasitic SCR to be triggered.

Latch-up normally only affects CMOS devices, there are, however, situations where bipolar devices can also suffer from it.

6.1.3. Shorts on Output

There are situations where short circuits can be applied to the output of the device. Unless the device has some form of over current and over temperature protection, it could be liable to destruction.

6.1.4. Power Supply Failure

This can basically come in two forms; the supply voltage gets too high or the supply falls to a voltage much lower than what it should.

If the supply voltage gets too high it implies that a fault has occurred in the regulator, and so normally a fuse can be used to protect the system from destruction.

The supply voltage falling below predefined level implies either a short across the output of the regulator or some other fault affecting the regulation of the regulator. The problem associated with the supply falling is that of data retention and/or the processing of incorrect data.

6.1.5. High Power/Current Faults

Very few devices can withstand even short periods where it is subjected to externally applied high current or power shorts. The Telecoms industry is quite often subjected to lightning strikes. Any device which is subjected to a lightning strike has to withstand high current and high power surges.

T.I. has developed a special range of devices to meet this particular problem, these will be discussed later in this section.

6.2. LinCMOS™ Input Protection

As discussed earlier all devices can be subjected to some of fault sometime during their lifetime, be it at assembly or during actual use.

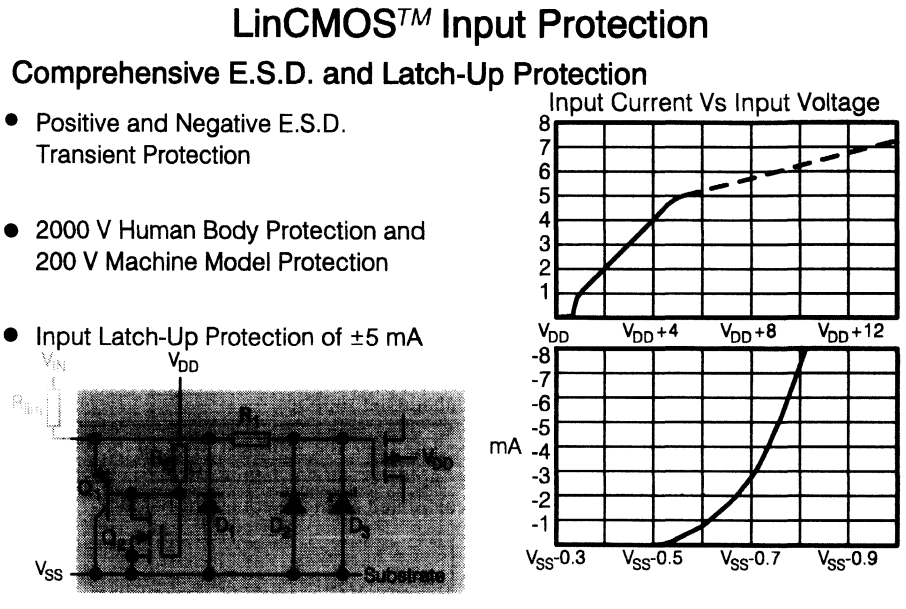


Figure 2.6.02. - LinCMOS™ Protection

One of the most common causes of device damage is electrical overstress. This can be due to applying too large a voltage across the device or by subjecting the device to ESD. CMOS devices are normally susceptible to ESD damage, and if subjected to ESD the effects can be totally destructive.

It is for the last reason that all T.I.'s LinCMOS device have built-in ESD protection circuitry, which protects the device for both positive and negative transients. The ESD protection circuitry will protect the device for voltages meeting the human body model up to 2000 V and up to 200 V for the machine model. These models are specified in MIL-STD-883C, Method 3015.2. This is far better than what is normally specified for bipolar and bifet op amps.

6.2.1. Positive ESD Transients

The initial positively charged energy applied to the input will be shunted to V_{SS} by transistor Q_1. Q_1 will only turn-on once the input has risen $1V_{BE}$ above V_{DD} (see figure 2.6.02). As the input rises, the current gain limit of Q_1 is reached causing it to go into saturation. Further increases in input voltage shunts current to V_{DD} by resistor R_2 and to V_{SS} by Q_1. The gate of Q_2, an enhancement mode N-channel MOSFET, also rises. Q_2 will turn on when the voltage on its gate exceeds its threshold voltage. Q_2 is used to clamp the majority of the energy of the ESD transient via the base emitter of Q_1.

However if the input voltage still continues to rise the zener diode, D_3, and resistor R_1 is used to dissipate the remaining energy.

6.2.2. Negative ESD Transients

The majority of the energy from the negative transient will be shunted to V_{SS} by diode D_1. Any additional energy will be shunted to V_{SS} via diode D_2 and resistor R_1.

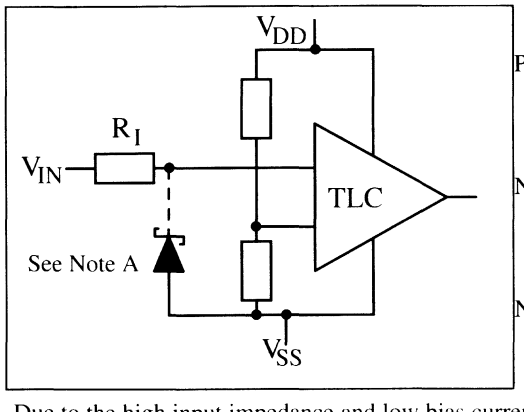
6.2.3. Latch-Up

CMOS integrated circuits are always more susceptible to latch-up due to their parasitic SCR structure. This parasitic SCR can be triggered on when the input is taken outside of the supply rails. If the parasitic SCR is triggered the only way of turning it off is to turn off the power supply.

All LinCMOS devices have their inputs tested to withstand a -100 mA pulse. They then undergo another test where their inputs and outputs are subjected to ±5 mA continuous current. This means that all LinCMOS devices can withstand transients exceeding the supply voltage as long as the input current is limited to less than 5 mA.

The input voltage versus input current curves in figure 2.6.02, show the voltage-current characteristics of LinCMOS devices when their inputs are taken outside the supplies.

If excursions from the supply voltages are expected then the simplest way of providing reliable operation is to place a resistor in series with the input, as shown below. If the largest excursion is known then the minimum resistance value can be calculated from the equations below.



Positive Voltage Input Current Limit

$$R_I = \frac{+V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit

$$R_I = \frac{-V_I - V_{SS} - (-0.3\ V)}{5\ mA}$$

Note A: If the correct output state is required when the negative input exceeds V_{SS}, a schottky clamp is required.

Due to the high input impedance and low bias currents of the TLC devices the errors introduced by the addition of R_I will be very small.

6.3. Integrated Circuit Input Protection

There are some applications where the device being used may require some extra protection. The TL7726 was designed to offer some extra protection for ADCs. One problem with most voltage clamps is that they will only clamp the device they are trying to protect when the voltage has gone above the supply voltage by more than one diode drop.

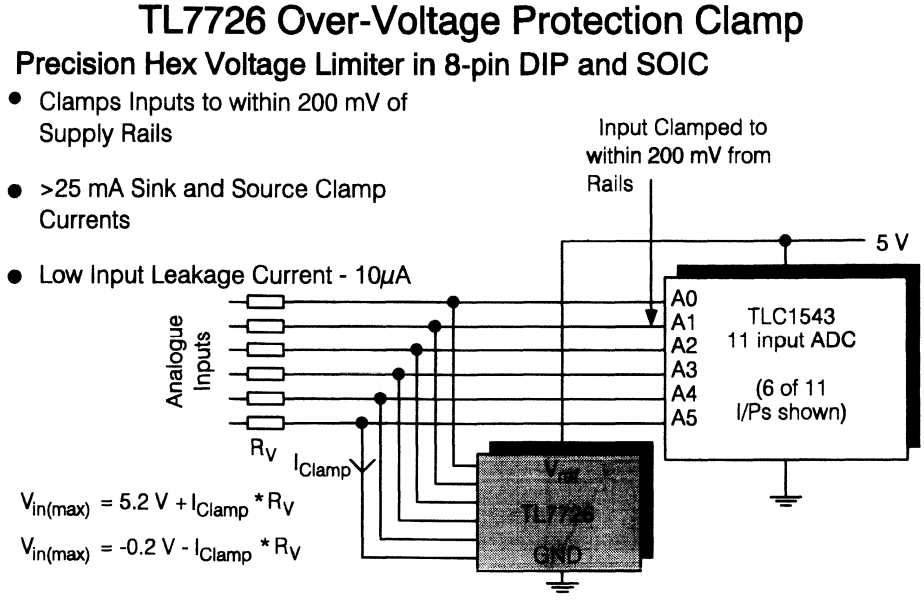


Figure 2.6.03. - TLC7726 Over-Voltage Protection Clamp

This will quite often take the device, that is to be protected, beyond its absolute maximum ratings. The TL7726 has been designed to help overcome this. Normal protectors using bipolar diodes or schottky diodes will only clamp to within 400 mV of the supplies, the TL7726 can clamp to within 200 mV of the supplies. The positive clamping voltage of the TL7726 is set by its reference voltage, which is normally tied the to the supply voltage of the device it is protecting.

The TL7726 is available in 8 pin plastic packages and is capable of protecting up to 6 separate lines. Each output clamp is capable of sinking or sourcing in excess of 25 mA. The maximum input voltage that can be applied to the device is determined by the serial resistor R_V as shown in figure 2.6.03. R_V is used to limit the power dissipated by the TL7726 and, to allow for the difference between the applied transient and the clamping voltage of the TL7726.

The only errors introduced by the TL7726 are due to its bias currents, 10 μA, which are low enough to be used with ADCs without a significant error, but are too large for use with op amps.

For more information see the application note available from the seminar data order form:- SCVDE01.

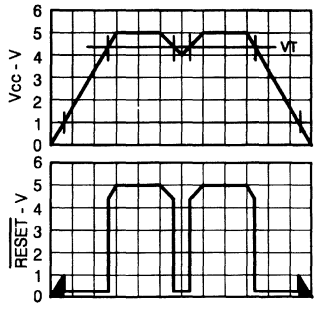
6.4. Micro-Controller Data Protection

Although voltage regulators have become more sophisticated within the last decade, there are still possibilities of fault conditions, such as variations in the supply to the regulator, which cannot be immediately corrected. In these cases, the result is a variation in the regulated supply voltage to the system.

Micro Controller Data Protection

- Defined Output from Vcc > 1V
- Precision Voltage Sensor
- True & complement Reset Outputs

Device	Function	Supply	Tolerance
TL7702A/B TL7705A/B TL7709 TL7712 TL7715	Under-voltage monitor	Prog. 5 V 9 V 12 V 15 V	1%
TL7757 TL7759	Under-voltage monitor	5 V 5 V	2.6%
TL7770-5 TL7770-12 TL7770-15	Under- and over-voltage monitor	5 V 12 V 15 V	1%



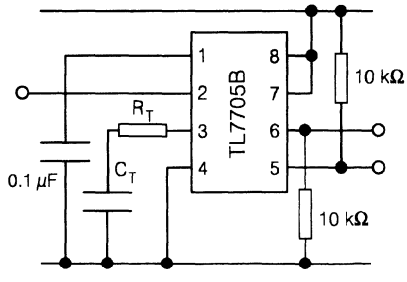


Figure 2.6.04. - Micro Controller Data Protection

In an analogue system, such variations can cause a degradation of the signal to noise ratio and the dynamic range of the system. However, this will occur as an increase in the level of the noise floor of the system and its effect can therefore be predicted. With a digital system however, the results can be more immediate and dramatic. Since a supply fault can affect any of the digital bits equally, it is just as likely that the MSB will be altered as the LSB, resulting in a possible change of the output by a factor of 2. The majority of digital systems operate from a 5 V supply, used by microprocessors and supporting logic. These devices have a defined operating window, within which they are guaranteed to process data correctly. Incorrect operation can be caused either by **under voltage** when the supply falls below its defined level, or **over voltage** when the supply exceeds its defined level. Under voltage is the more common problem since the regulator can normally cope with an increase in its supply, but when the supply fails, the output from the regulator falls with it. Therefore a negative going spike on the input is transmitted to the output as an under voltage condition.

The job of the Supply Voltage Supervisor (SVS) is therefore to monitor the supply voltage to a system, and to ensure that the system only operates within a defined supply voltage "window" by applying a reset signal to shut it down when the supply deviates outside this window. A secondary function of the SVS is to ensure the system powers up correctly by applying the reset to the system until the supply has stabilised. In the past, a simple RC network has been used for this purpose, but it is subject to noise on the supply and therefore may not prove reliable.

6.4.1. TL77XX

Texas Instruments pioneered the monolithic SVS with the introduction of the TL77XXA family of devices. This family consists of four fixed sense voltages (5 V, 9 V, 12 V and 15 V) and one programmable device (TL7702).

In line with T.I.'s drive for continual improvement, T.I. has released a "B" version in the programmable and fixed 5 V version. These offer improved switching speeds and a reduction in the propagation delay, thus improving the response rate to a fault condition. They also provide a defined $\overline{\text{RESET}}$ output with a supply voltage of only 1 V. This family of SVS provide a reset on an under voltage condition and a clean power up reset.

6.4.2. TL7770-XX

An increasing requirement of many new systems is the ability to monitor multiple supply rails. A typical application for this would be a micro processor system with associated analogue functions. The 5 V microprocessor outputting data to an RS232 interface with transceivers operating from ±12 V supply or the data could be passed to a signal conditioning process which includes operational amplifiers and DACs which may require ± 15 V to operate correctly. In each case, it is required to monitor the multiple supply rails to ensure that each part of the system is powered up and in the correct voltage window. The TL7770-XX family was designed for this purpose. Each member of the family is a dual SVS with inputs to monitor both under voltage (1VSU and 2VSU) and over voltage (1VSO and 2VSO) on each of the two channels.

6.4.3. TL7757/9

As battery powered equipment became more and more popular, the typical supply current of 1.8 mA for the TL7705 was unacceptable in their application. In response to this, Texas Instruments designed two new supply voltage supervisors, the TL7757 and the TL7759. These have a low standby current of just 40 µA max. and designed for 5 V power supplies. The major difference between the two is that the TL7757 has only one $\overline{\text{RESET}}$ output, where as the TL7759 has two (RESET and $\overline{\text{RESET}}$) outputs. These devices do not require any timing capacitors or resistor divider networks, only a pull-up/pull-down resistor for the open collector output(s). This reduces the system complexity and saves on valuable board space in portable, battery operated equipment.

"Why the use of R_T for the TL770XXB and TL7770-XX devices ?"

The device could erroneously indicate a fault (outputs will be driven active) if the C_T pin is driven more positive than the V_{CC} pin. At first glance of the circuit, this would not be expected to occur in a typical application because the C_T pin is normally connected to an external timing capacitor. The TL7705B itself charges this capacitor; therefore it should never be driven to a voltage greater than V_{CC}. However, in a common application, the under voltage sense pin and V_{CC} are tied together to V_{CC}. During normal operation (no fault condition), the timing capacitor is charged by the on-board

current source. The capacitor will be charged to approximately. V_{CC} or to an internal voltage clamp (7.1 V zener) whichever is less. If the circuit is then exposed to an under voltage fault condition where V_{CC} is slewed rapidly down, the voltage on the C_T pin will exceed that on the V_{CC} pin. This forward biases a "sneak path" internally which falsely activates the outputs. A fault will be indicated when V_{CC} drops below V_{CT}, not when V_{SENSE} falls below V_{TH}.

It has been found that 1.4 mA must be forced into the C_T pin to trigger this false reset. The device is 100% tested to ensure that the outputs do not switch with 1 mA forced into the C_T pin. One proven way to eliminate this behaviour is to add a series resistor between the capacitor and pin 3. Adding this series resistor will change the duration of the reset pulse, but not by a significant amount. The resistor extends the discharge of C_T, but also skews the V_{CT} threshold. These two effects tend to cancel one another. The precise percentage change can be derived theoretically, but the equation is complicated by this interaction and is dependent on the duration of the supply voltage fault condition.

6.5.3.3 V and 5 V Systems Protection

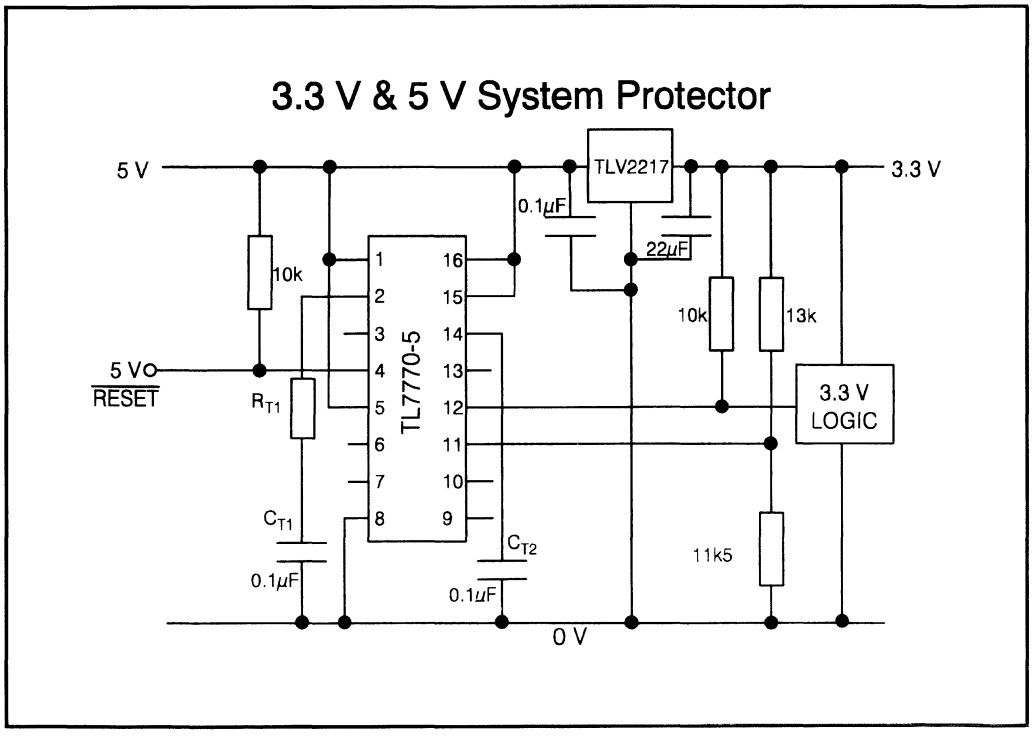


Figure 2.6.05. - 3.3 V and 5 V System Protector

During the transition from 5 V to 3.3 V IC technology, designers are faced with the challenge of integrating the two voltage levels and combining the new lower power, high speed 3.3 V logic chips with existing 5 V products in their new designs. These mixed mode circuits dictate the need for

multiple supply rail supervision. The schematic shows a simple way to monitor both 5 V and 3.3 V power supplies and generating separate RESET signals when either supply experiences an under voltage fault.

6.5.1. TL7770-5

The heart of the circuit is Texas Instruments TL7770-5 dual power supply supervisor (SVS), as discussed earlier.

The TL7770-5 features a 5 V pre-set under voltage (1VSU) supervisor and a programmable under voltage (2VSU) supervisor. It also features two overvoltage sense inputs. During power-up, the active low $\overline{\text{RESET}}$ outputs are guaranteed low after V_{CC} reaches 1 V. When the voltage on 1VSU passes through the threshold voltage of 4.55 V, a time delay is initiated, after which the RESET outputs are de-asserted. During an under voltage condition, when 1VSU again drops below 4.55 V, the 1RESET and $\overline{\text{1RESET}}$ are immediately asserted, and remains so for a period of Time after the under voltage condition expires.

6.5.2. Undervoltage

As discussed earlier, the TL7770-5's 1VSU has an internal resistor network which makes the voltage supervisor switch when the supply voltage is 4.55 V or less. The programmable under voltage (2VSU) has a connection directly to the comparator input, so the resistor divider network can be externally set. The values of R1 and R2 can be found from the following formulae;

$$R_1 = \frac{R_2(V_{CC} - VSU)}{VSU}$$

Where VSU is the under voltage threshold level which is typically 1.5 V. V_{CC} is the supply voltage at which the designer wants the supervisor to switch the outputs. The optimum resistance values can be found with the ratio of R_1 and R_2 known.

6.5.3. Overvoltage

As digital electronics become less tolerant to over voltage conditions, the TL7770-5 supply voltage supervisor has the facility for this also to be monitored. Two Programmable over voltage pins are assigned to the TL7770-5 (1VSO & 2VSO). When the supply voltage passes through the over voltage threshold level, the SCR Drive output is taken active high. An SCR triac could be controlled from this pin which could then be used to short out the supply rails through a low "dummy" load thus blowing the power supply fuse. Since the SCR pin is active high and capable of sourcing current, this pin can also be used to drive an NPN transistor or as an over voltage system flag pin for example.

6.6. Telecom Protector Overview

This section illustrates the need for overvoltage protection in telephone equipment and describes a range of power products specifically designed for the overvoltage protection of Telecom equipment.

Lightning strikes and accidental mains voltage crossed on to the telephone line can create serious problems for modern telecommunications equipment.

Texas Instruments has introduced a range of compact dual wire bi-directional shunt overvoltage protectors with high surge current capability. This TISP (Texas Instruments Surge Protector) series of transient protectors meets the needs of new electronic exchanges, PABX, and telephone subsets.

The TISP products are implemented using TI's high reliability ion-implanted planar process which permits precise control of electrical characteristics, extremely stable parameters, and the monolithic integration of two bi-directional overvoltage protectors in a single power package. In this way complete system shunt protection can be afforded by a single TISP device. Board packing density and layout problems are greatly improved.

Primary overvoltage protectors are manufactured using the same high reliability fabrication process but are designed to withstand the higher surge currents present on the front line. The all soldered cell construction of these devices allows heat to be removed from both faces of the silicon allowing higher power line cross currents. An additional feature is the specially shaped copper electrodes soldered to the silicon which promotes a progressive shorting action under severe overload conditions allowing fail safe protection modules to be developed.

6.7. The Need For Telephone Equipment Protection.

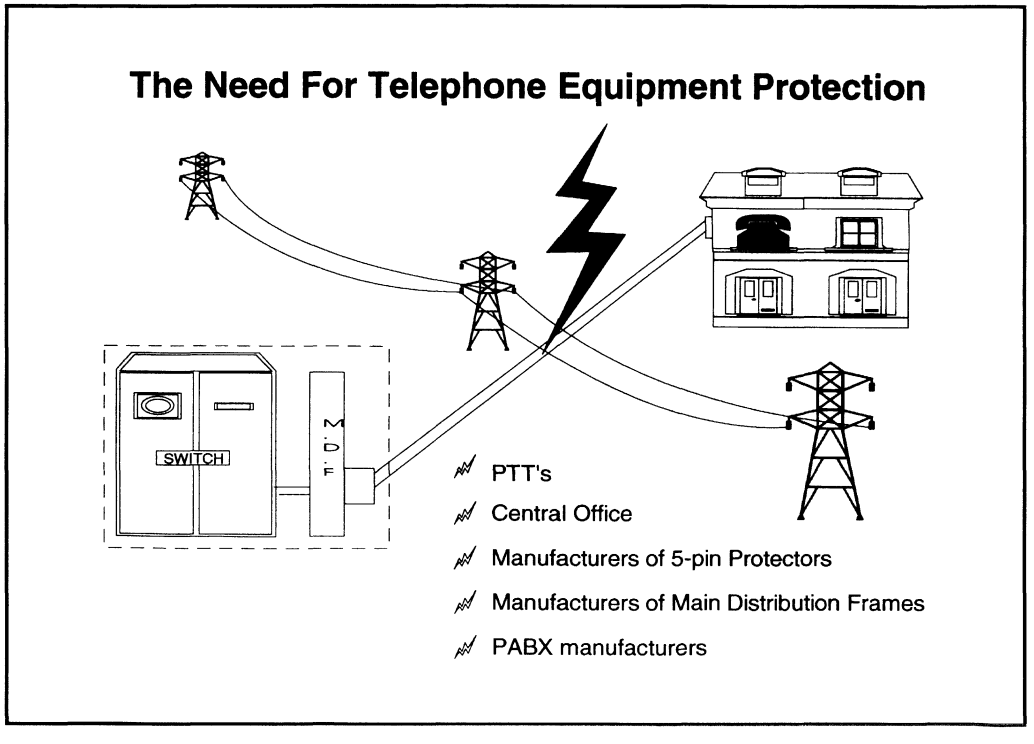


Figure 2.6.06. - The Need For Telephone Equipment Protection.

Disturbing voltages on the telephone line, either from direct contact or induction, can arise from lightning strikes or man made sources: the most common being ac power line. The exposed and distributed nature of the telephone network make it vulnerable to such problems and even buried cables are not immune. These disturbances are extremely difficult to quantify. As a result, each country has evolved standard tests which reflect local conditions and perceived requirements.

Generally two forms of test are specified, one set covers lightning, and the other emulates contact to ac power lines. These tests are applied between the line wires and the ground. Sometimes additional tests are made between the line wires. Most tests require the equipment to be functional afterwards, while some specify increasing the level of stress levels until equipment failure occurs. This is to ensure that the equipment fails in a safe and controlled manner under extreme conditions.

6.7.1. Lightning surge tests

Lightning is characterised by rapidly rising wave-fronts and longer decay times. A typical European test as specified in CCITT K17 specifies an artificial lightning generator circuit in which the open circuit output voltage waveform rises in 7 μs(10%-90%), initial rate 180 V/μs) and decays to 50% of its 1.5kV peak value in 730 μs. The short circuit output waveform rises in 4 μs(10%-90%, initial rate 18 A/μs) and decays to 50% of its 38 A peak value in 310 μs. In comparison, the capacitive energy of this test is over 100,000 times greater than the ESD test used to qualify CMOS 74HC logic. This enormous energy differential means that overvoltage protectors cannot be "hidden" under bond pads but require large amounts of dedicated silicon.

6.7.2. AC power line contact tests

AC power line contact tests are characterised by voltage levels up 650 V RMS, with current levels up to 10 A RMS applied either for a few cycles or continuously. Long term protection against this kind of hazard requires a series overcurrent protector such as a fuse, PTC (Positive Temperature Coefficient) resistor, or some kind of thermally activated trip. The complex interaction between the overcurrent and overvoltage protectors, together with the great variety of test specifications, has necessitated the manufacture of specialised in-house evaluation equipment, and the generation of computer simulation programmes.

6.8. Telephone Equipment Protection

In the protection network shown in figure 2.6.07 the transient suppresser and the solid-state primary provides shunt overvoltage protection and the fuse, PTC (Positive Temperature Coefficient) resistor, or fusible resistor is used for series overcurrent protection.

Overcurrent protectors "open" the line when overloaded. Fuses and fusible resistors automatically dictate board rework after overstress. PTC thermistor based overcurrent protection systems are intended to recover once the overload is removed.

Figure 2.6.07 also compares the various types of overvoltage protectors in terms of operating principles, characteristics and pulse response. The characteristics shown are normalised to 1 mA at 200 V.

6.8.1. Zener diodes

Zener diodes for transient suppression are large area devices with special attention given to chip thermal management to absorb short term energy dumps. The zener is a very efficient clipper for short or low current level disturbances. The relatively low zener thermal capacitance results in high level transients causing large increases in junction temperature which in turn produces very large voltage increases, negating the protection.

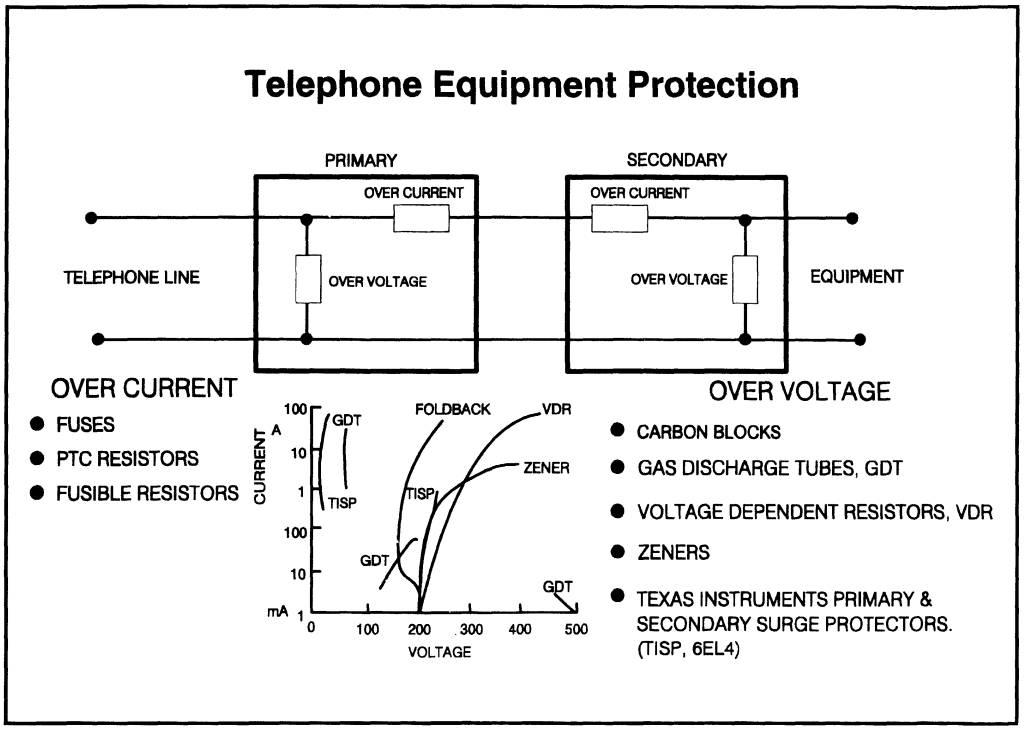


Figure 2.6.07. - Telephone Equipment Protection

6.8.2. Voltage Dependent Resistors

The most popular form of Voltage Dependent Resistor(VDR)/Metal-Oxide Varistor(MOV) is manufactured from zinc oxide compounds and is produced in a variety of shapes. The voltage current relationship of a VDR is given by:-

$$V = C^*(I)^{\beta} + I^*R_S$$

Where V = VDR voltage, I = VDR current, C = voltage coefficient, ß = non-linearity coefficient (typically 0.035), R_S = bulk ohmic resistance (typically 0.5 OHM for 10 mm disc) As the VDR does not have a sharp current initiation, like an avalanche diode, the specification point depends upon the

amount of leakage current that can be tolerated. VDR's are available with a ± 10 % voltage tolerance on the voltage measured at 1 mA.

Inherently VDR clamping is inferior to that of a zener. However at high energy levels the lower thermal sensitivity of the VDR results in a better clamping voltage than a zener. A 50% increase on the 1 mA VDR voltage might be typical at these high levels. Unfortunately VDR's degrade as a result of operation which ultimately leads to a loss in protection.

6.8.3. Foldback Diodes

Foldback Diodes are not diodes but symmetrical (pnp or npn) three layer silicon structures. In transistor terms these devices conduct very little current until the voltage reaches the BV_{CEX} value. As the current increase the device voltage reduces by about 30% to follow a $BV_{CEO(SUS)}$ (type characteristic. This feature allows the foldback diode to absorb higher current surges than an equivalent area zener.

Under ac power line contact conditions, potentially destructive amounts of device power can be dissipated, without the series protection element operating.

The peak voltage level tolerance is typically about ±15%, which is better than a ±5% zener, after allowing for the zener's clamping performance.

6.8.4. Gas Discharge Tube

A Gas Discharge Tube(GDT) protector consists of a gas filled tube with an electrode at each end. At a certain voltage, gas breakdown (sparkover) occurs and the voltage falls to the medium voltage glow discharge region, which is maintained up to medium currents. Beyond this current level a high current, low voltage arc is formed, which passes very high currents (5 kA). This capability makes the GDT suitable for primary protection in an exchange main distribution frame (MDF) wiring. The low voltage conduction mode is not maintained, after the disturbance has subsided, as normal line currents are not high enough. Thus the arc is extinguished and normal operation resumes.

The Gas Discharge Tube Problem

A major GDT problem is the reaction time of the gas to fast rising voltage wave-fronts. A GDT could initiate breakdown at 200 V dc, but delay to 500 V at 500 V/µs and 800 V at 1000 V/us. It is therefore essential that the secondary protector takes care of these high voltage edges let through by the GDT in the MDF.

6.8.5. Texas Instruments Surge Protector (TISP)

The Texas Instruments Primary and Secondary surge protectors are based on a four layer thyristor structure. This gives a voltage triggered "crowbar", whose high holding current ensures delatching after the surge has subsided. This effectively gives an overvoltage protector which has the best advantages and non of the drawbacks of the Gas Discharge Tube(GDT), zener diode, Metal Oxide Varistor(MOV), and foldback diode devices.

The TISP possesses the same rapid response to fast rising voltage wavefronts as the zener, MOV or foldback diode devices. At low current levels the TISP limits the overvoltage in a manner similar to a zener protector.

Higher current levels initiate a crowbar action in the TISP. Important differences exist between the TISP and GDT crowbar characteristics. The TISP does not display an intermediate glow discharge

region like the GDT, and hence any potential dc latchup problems are avoided. In addition the TISP has a much lower "on" state voltage than the GDT for the current range considered. As the current surge subsides, a current level is reached where the crowbar action terminates. Crowbar action is maintained to lower current levels with the TISP and so the remaining surge energy to be dissipated is much less.

Although not shown the TISP leakage currents are extremely low, as would be expected of a solid state device. In this respect it is similar to the zener or foldback diodes.

6.9. Central Office Primary Protection

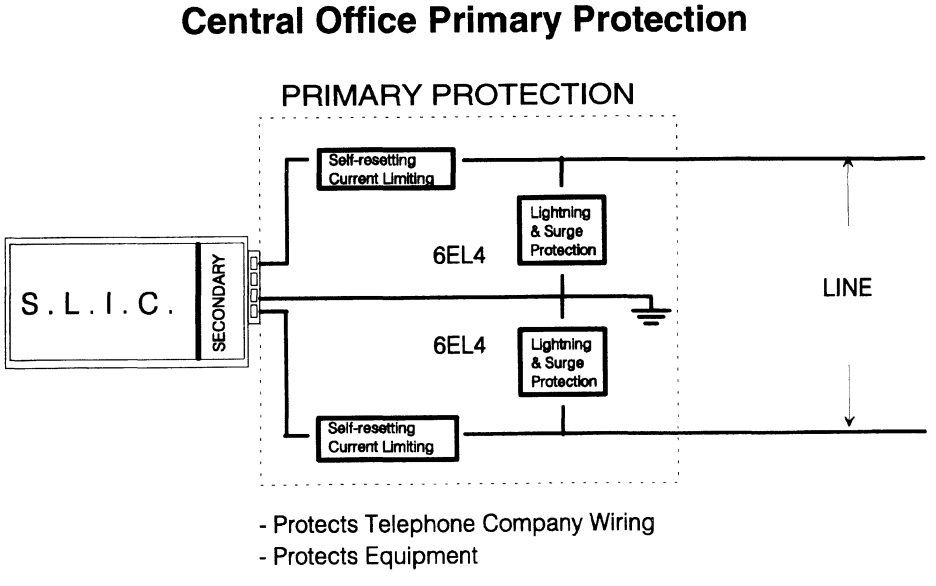


Figure 2.6.08. - Central Office Primary Protection

The 6EL4 is a solid-state symmetrical primary overvoltage protector developed to remove the transient voltages let through by gas discharge tube protectors. The solid-state 6EL4 will not degrade the level of protection during service life and is intended to be a direct replacement for gas discharge tubes as the first line of defence. The device would normally be incorporated within an assembly module along with some form of series current protection and be located on the MDF (Main Distribution Frame) at a point where the copper wires enter the building, thus protecting the building and the exchange equipment

Primary overvoltage protectors are the first line of defence against fault conditions due to lightning surges and power line surge both direct and induced. The major difference between primary and secondary protectors is that the primary must be able to withstand the higher currents present on the front line and to fail in a safe mode. That is, Short Circuit.

Primary protectors generally have higher protection voltages to enable them to be used in all equipment and locations.

6.10. Exchange S.L.I.C. Protection

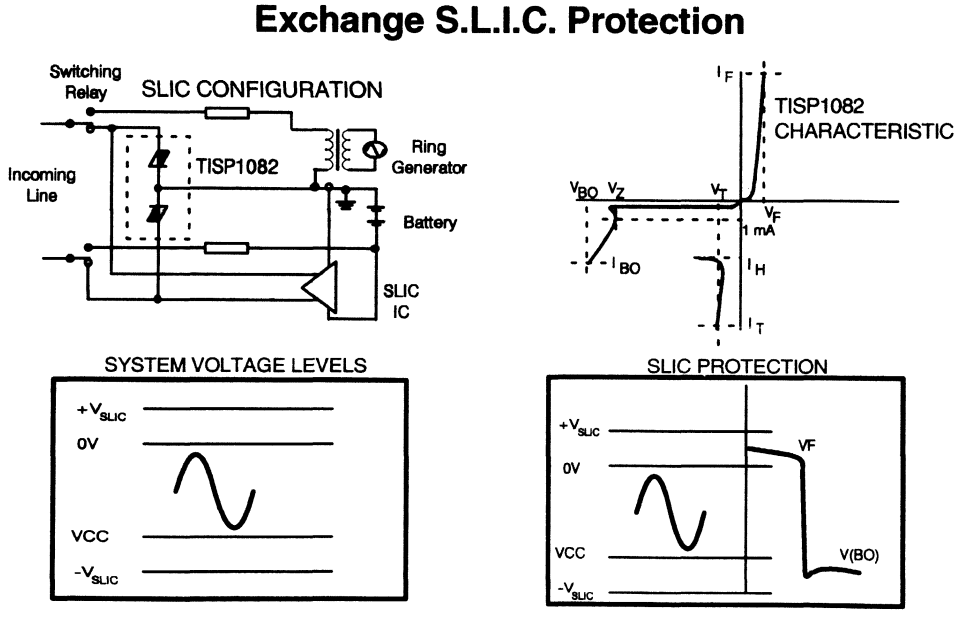


Figure 2.6.09. - Exchange S.L.I.C. Protection

The TISP1082 is a dual asymmetrical device in a TO220 package, to protect particular SLIC types. "Low voltage" SLICs develop their output between 0 V and -Vbat with relay isolation from the ringing voltage. Negative disturbing voltages are suppressed by voltage triggered crowbar action. In this protector the positive voltages are clipped to ground by diode action, because the usual positive voltage triggered crowbar sections have been replaced by diode sections.

6.11. Subscriber Equipment Protection

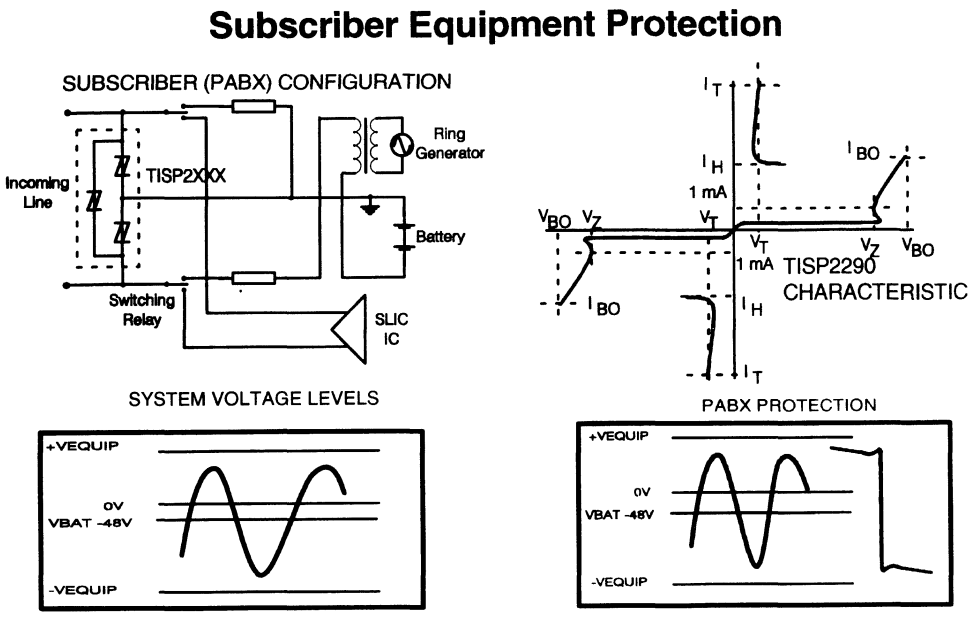


Figure 2.6.10.. - Subscriber Equipment Protection

The TISP2290 is a triple symmetrical device in TO220 package for wire to wire and wire to ground protection, using a smaller symmetrical crowbar protector implemented between the line wires. This results in the clipping voltage being the same for wire to wire and wire to ground. A study of ringing configurations shows that this voltage condition only occurs in battery backed systems. In all other ringing configurations the wire to wire voltage exceeds the wire to ground value.

The TISP3180 is a dual symmetrical device in TO220 package, for wire to wire and wire to ground protection, in all ringing configurations.

6.12. Integrated Services Digital Network

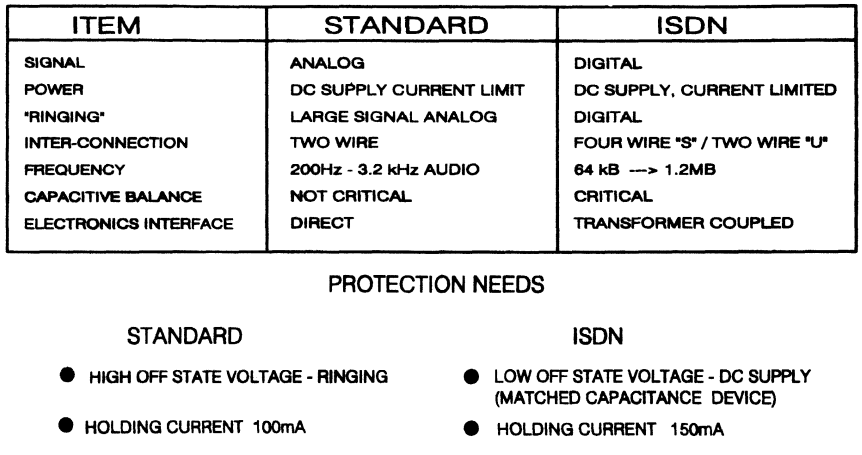


Figure 2.6.11. - Integrated Services Digital Network

Analogue signals are predominately used for both voice and data transmission on current subscriber lines. Modems are employed for conversion to and from the digital domain. A switching and transmission system using digital signals can have advantages to both the supplier and user of the telephone network. Digital signalling will allow the addition of new services for the user and enhanced system control and management for the supplier.

The major differences arising from the change from analogue to digital signalling are addressed in Figure 5. The change in frequency from the audio range to 64 kB and above results in line capacitive balance becoming a critical system parameter in ISDN systems.

These different system needs translate to different protector requirements. The analogue system protector needs to have a high off-state voltage due to the peak ringing voltage and a holding current of around 100 mA as defined by the SLIC short circuit line current. The ISDN system protector, however, needs to have a lower off-state voltage as there is only a lower voltage dc supply. Maximum line currents tend to be higher than those present in analogue systems requiring a higher holding current. The ISDN protector must be capacitively matched between each wire to ground.

6.13. Integrated Services Digital Network Protection

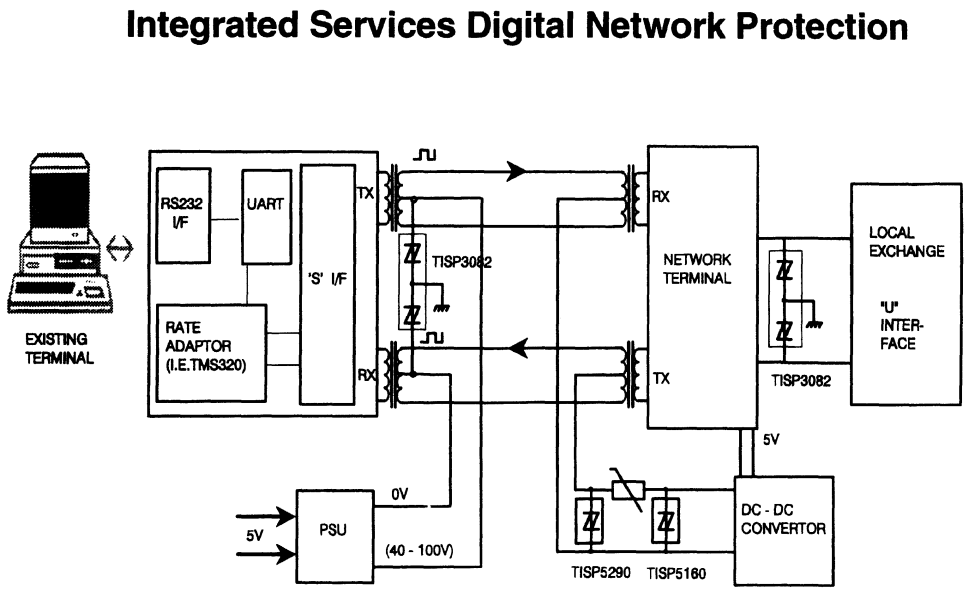


Figure 2.6.12. - Integrated Services Digital Network Protection

Figure 2.6.12 shows the implementation of a 4-wire "S" interface with transformer coupled transmit and receive. Additionally a 2-wire "U" interface is shown between the local exchange and the network termination.

The TISP3082 can protect both the "S" and "U" interfaces as it is a dual low voltage high holding current device in a single package. Power is fed from the network termination to the terminal equipment via the Tx and Rx wire pairs. By placing the TISP3082 protector at the transformer centre tap any capacitance unbalance effects from the protector are avoided.

This is not possible on the "U" interface as Rx and Tx functions are carried by the same two wires. The protector will add "unbalance" to the system as one of its sections is biased at around 0 V while the other section is biased at the power supply voltage. The capacitance of the low bias section will be higher than that of the higher bias section as the capacitance of the silicon junctions is a maximum at 0 V. The difference in capacitance between the two sections will determine the out off balance effect on the system. This in-balance will increase with increasing frequency. Typically the amount of capacitive unbalance introduced by the TISP3082 will be less than 120 pF.

6.14. Texas Instruments Surge Protectors

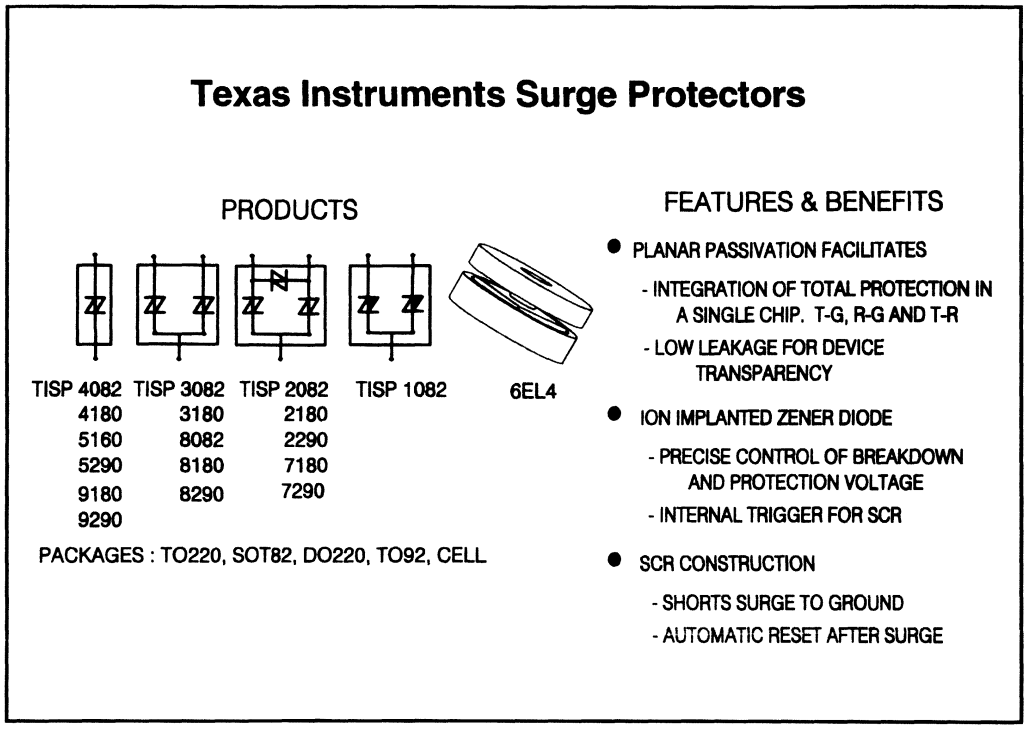


Figure 2.6.13. - Texas Instruments Surge Protectors

The voltage capability of the modern generation of solid state telecommunications circuits is such that they can be connected directly to the telephone line, thus saving the cost of an isolating transformer. However the voltage safety margin of these circuits is typically only 50% greater than the normal operating conditions. Very fast and precise voltage limiting is required to prevent damage from line transients caused by lightning and power line crosses. The Texas Instruments Surge Protector was designed to offer full protection to these new solid state circuits.

In the TISP, the opportunity was taken to integrate protection for both wires to ground and also between wires for both positive and negative overvoltage transients. This integration was greatly facilitated by the use of a high voltage planar passivation process which in addition to its low leakage, in the order of nA, resulting in low battery loading, also meets the 20+ year life reliability requirements demanded by the Telecom industry.

The TISP uses a patented ion-implanted process to define the breakdown voltages. This is a more cost effective solution than setting voltages by selections of wafer resistivity, and gives precise control of stand-off and protection voltages.

Current flowing in the ion-implanted zener diode causes an integrated SCR to turn on and essentially shorts the surge to ground. This thyristor action allows much better silicon utilisation than standard zener diodes.

The additional advantage of the SCR is that as the surge current flowing decays, the SCR will automatically turn off when its holding current is reached.

The single chip, single package TISP is transparent to the line in normal operation, clamps the overvoltage surge by zener action, shorts the surge by SCR turn on and automatically resets when the surge decays.

Analysis of the telephone system shows that there are several fixed voltage protector configurations required for complete market coverage. This has resulted in four protector series, TISP1XXX, TISP2/7XXX, TISP3/8XXX, and TISP4/5/9XXX; where XXX is the protection voltage $V_{(BO)}$. These devices provide a complete system solution to line overvoltage protection in a single package. These protectors can be inserted into a PCB any way round. The standard pinout with line wires to the outer pins and ground to the centre pin allows for this.

The TISP family of programmable products provides the Telecom system designer with a new and more precise form of overvoltage protection function. New system designs will utilise solid state relays and integrated SLICs. To make these designs a practical reality the superior protection performance given by the TISP device will become mandatory.

7. Summary

7.1. Texas Instruments Signal Conditioning

T.I. has a long history in analogue signal conditioning products, and is continuing to introduce more products each year.

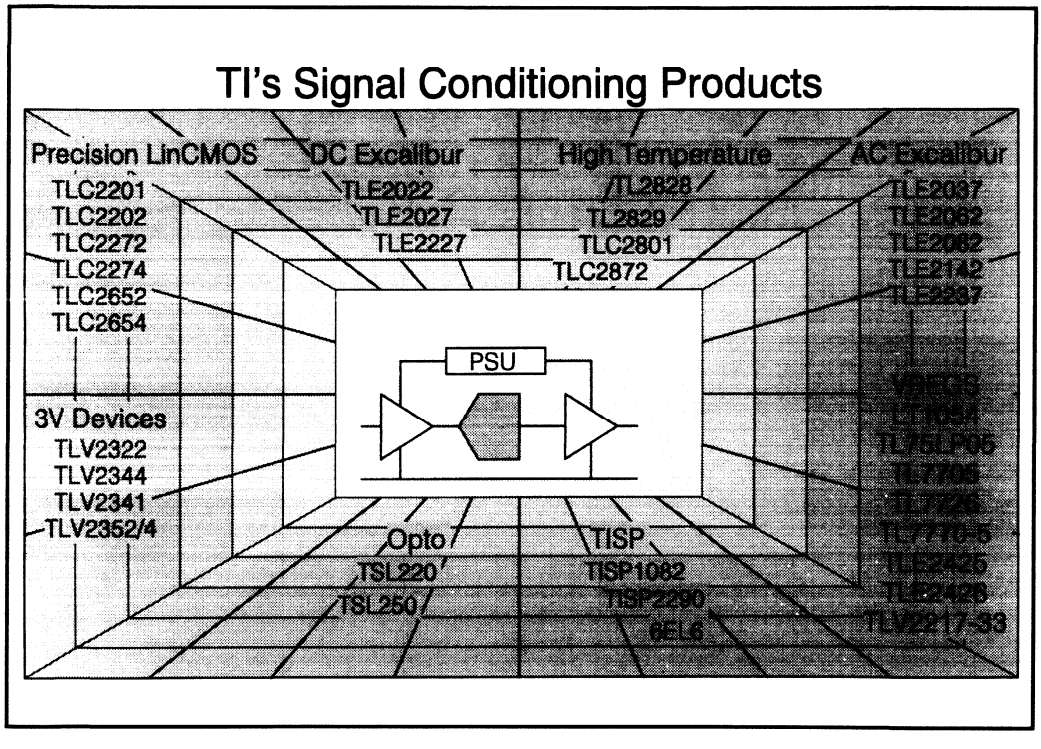


Figure 2.7.. - T.I.'s Signal Conditioning Products

Most of these new products have been designed in Excalibur and in Advanced LinCMOS. These processes enables T.I. to produce high quality and high performance products capable of meeting most of today's system needs.

This seminar has discussed some of the newer and higher performance products, and Figure 2.7 lists most of the devices discussed today.

By gaining better market understanding and combining this with the Excalibur and Advanced LinCMOS technologies we hope to provide you with the right device to meet your needs.

Section 3
Data Conversion

Section Contributions by:

Richard Nail

Al Miller

Bridget Barrett

Dave Cox

Edited by: Dave Cox

Contents
Section 3

1. Introduction

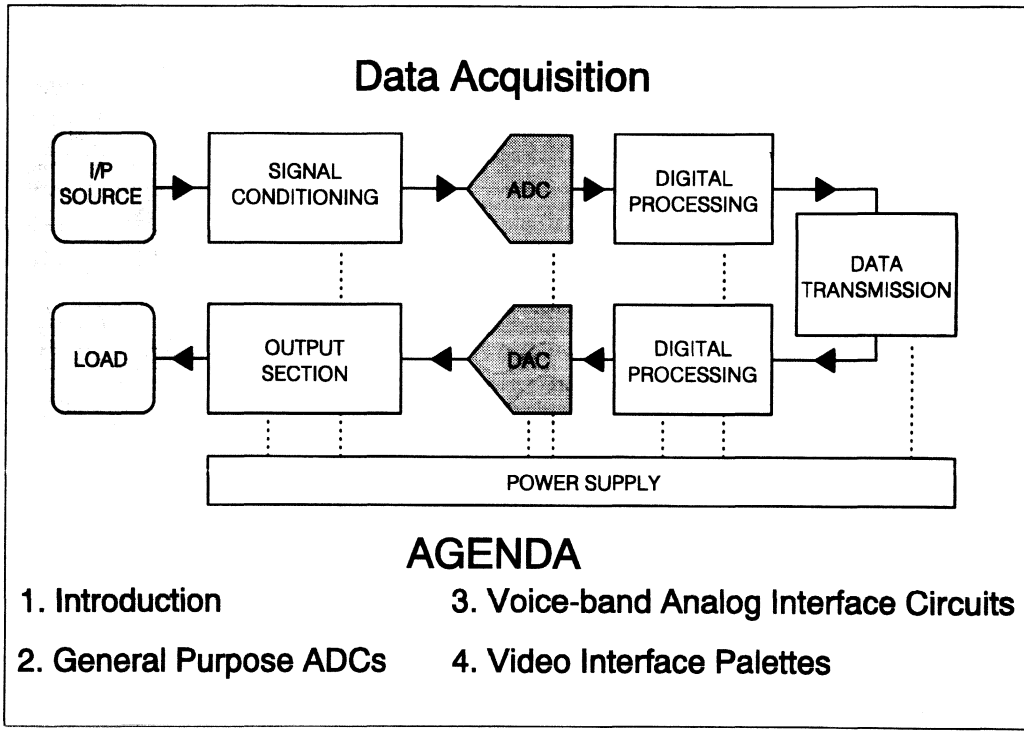


Figure 3.1.1 - Data Acquisition

1.1. Where Data Acquisition fits in a System

Most modern electronic systems have digital processing as the core; from things we are familiar with in every day life such as television, the motor car, personal computers, etc. to more specialised equipment in the industrial and scientific environments. Yet the world we inhabit is essentially analog in nature - so we need devices to convert from the, "real world", analog domain into the digital domain occupied by the processor. The Data Acquisition devices covered in this section of the handbook are one group which fulfils this function.

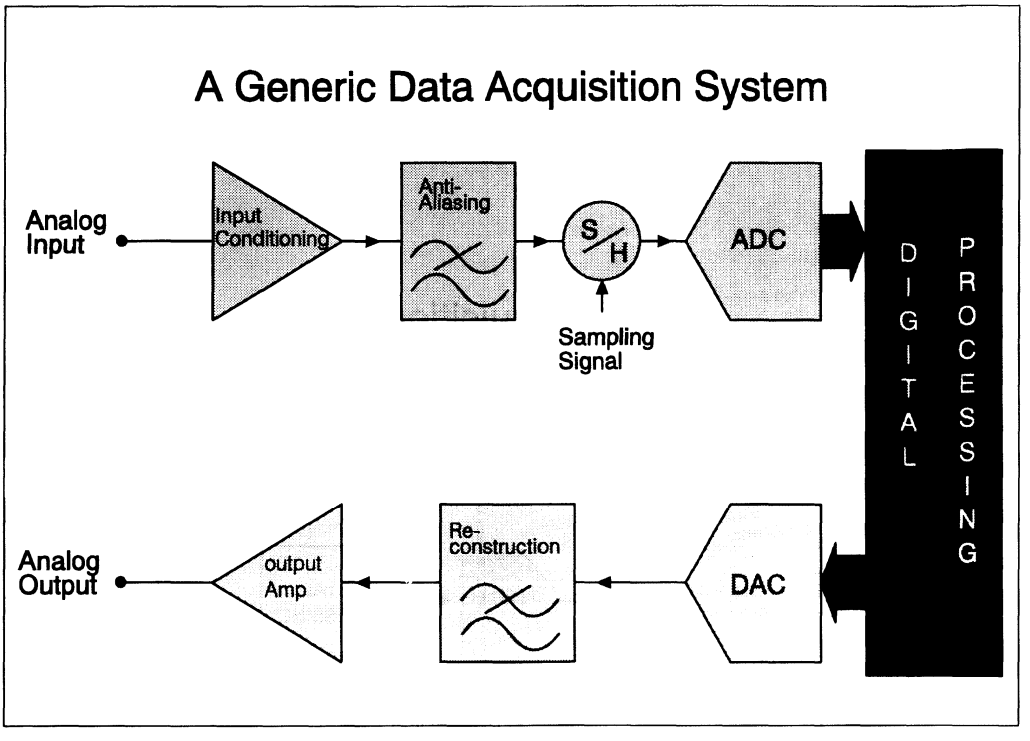


Figure 3.1.2 - Generic Data Acquisition System

The above figure illustrates the basic elements of a generic data acquisition system. Many people think of data conversion as being just the Analog-to-Digital Converter (ADC) or the Digital-to-Analog Converter (DAC). However to convert from the analog domain to the digital domain, the I/P signal needs its levels matched to the I/P range of the ADC; it needs filtering to remove frequency components above the Nyquist rate and sampling to convert the continuous-time signal into a sampled signal. Finally it can be quantised by the ADC. To convert from the digital domain back to the analog domain, the DAC needs a reconstruction filter to convert its O/P back to the correct baseband signal and an O/P amplifier to drive the load.

All the data acquisition devices discussed in this handbook contain at least some of these extra functions and some contain them all.

1.2.Selecting an ADC for Your System

When choosing an ADC for a particular application, you have to consider several aspects of its performance:

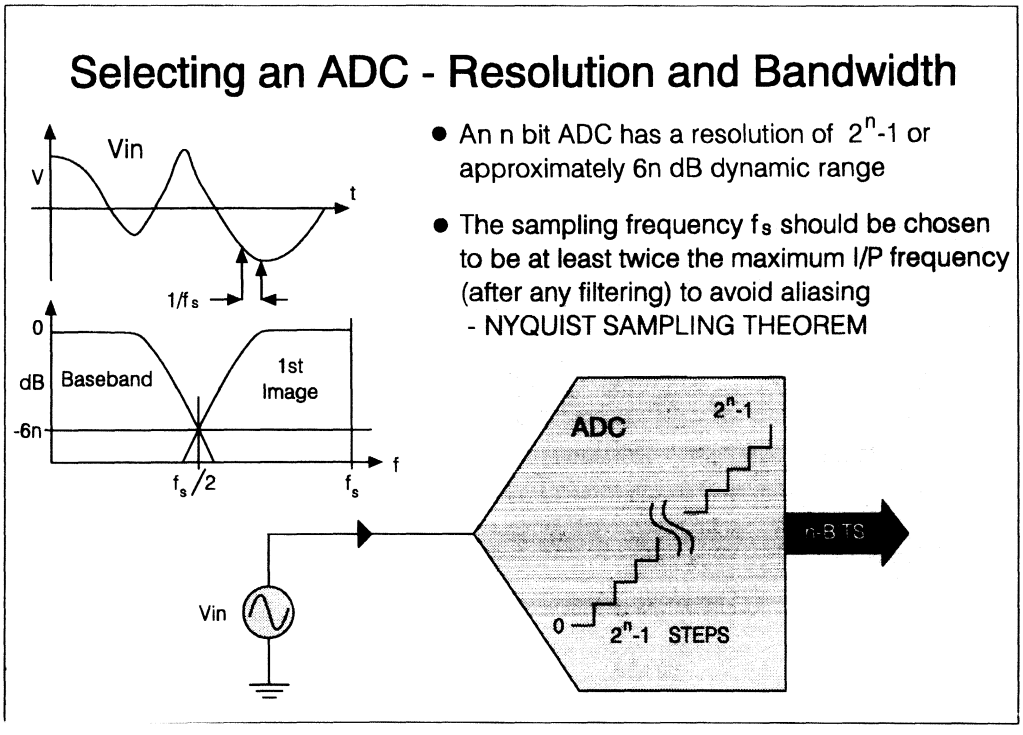


Figure 3.1.3 - Resolution and Bandwidth

1.2.1. Resolution

An ideal n-bit converter will have $2^n - 1$ steps which corresponds to a dynamic range of approximately $6n$ dB. This needs to be matched to the signal-to-noise ratio / dynamic range requirements of your system.

1.2.2. Sampling Rate and Bandwidth

The sampling frequency (f_S) of your system needs to be chosen to be at least twice the maximum I/P frequency (after filtering). This is Nyquist's Sampling Theorem. In practical terms, f_S should normally be twice the frequency at which the signal crosses the noise floor of the system. However the conversion time (T_{CONV}) of the ADC will have to be less than $1/f_S$ in order to allow the sample-and-hold circuit (S/H) time to acquire the signal to the required accuracy.

1.2.3. Linearity, Gain and Offset Errors

The ideal transfer function of an ADC will be affected by errors such as: zero offset, gain error, differential non-linearity and integral non-linearity.

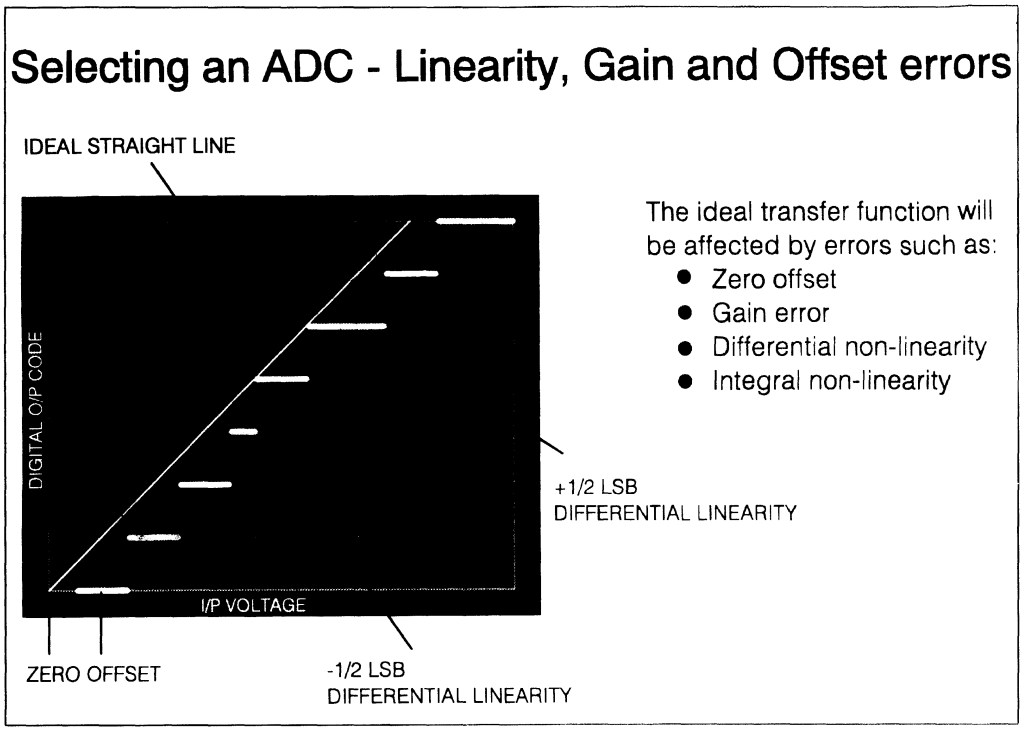


Figure 3.1.4 - Linearity, Gain and Offset Errors

- **Zero offset is the mid-step I/P value when the O/P code is zero.**
- **Gain error is the difference between the actual mid-step value and the ideal mid-step value when the digital O/P code is maximum (measured after correcting zero offset).**
- **Differential non-linearity is the difference between the actual step width and the ideal step width of 1 LSB.**
- **Integral linearity is the deviation of values from a straight line, normally, drawn through the end points.**
- **Total error is the sum of all the above errors.**

Zero offset and gain error can be corrected by adjustment of the DC offset and gain respectively. But in many systems this is an undesirable expense, both in terms of the additional components / board space and in terms of the additional test time.

Differential non-linearity and integral non-linearity add to the noise and distortion of the system, degrading its performance from the ideal value for the given resolution in bits.

TI's devices are well specified in terms of the above errors and, by selecting the right device, the requirement for expensive gain and offset trimming is often precluded.

2. General purpose ADCs

Successive approximation continues to be the most popular conversion technique for general purpose ADCs as it covers a wide range of resolutions from 8-16 bits and conversion rates from 100us to below 1us.

TI's TLC1540 family, TLC1550 family and TLC1225 family of ADCs discussed in this section are all successive approximation ADCs with typical speeds and resolutions for this family.

2.1. Successive Approximation Principle

Successive comparison of an unknown analog input voltage with binary weighted values of a reference give this method its name of "successive approximation".

One input of the comparator, shown in the block diagram, is driven by an unknown input signal, V_{IN} while the output of the DAC drives the other. The successive approximation register provides the input to the DAC and responds to the output from the comparator.

When the DAC has its MSB set to logic 1 (with all other bits zero), by the successive approximation register (SAR), it will produce a voltage output of 1/2 the reference and analog input full scale range. The comparator then determines whether the DAC output is above or below the unknown input signal. If, as shown, the input signal VIN is above the DAC output value, the MSB is retained in the successive approximation register while the next weight of 1/4 the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register. Therefore a converter of N-bit resolution takes N steps to achieve a digital output.

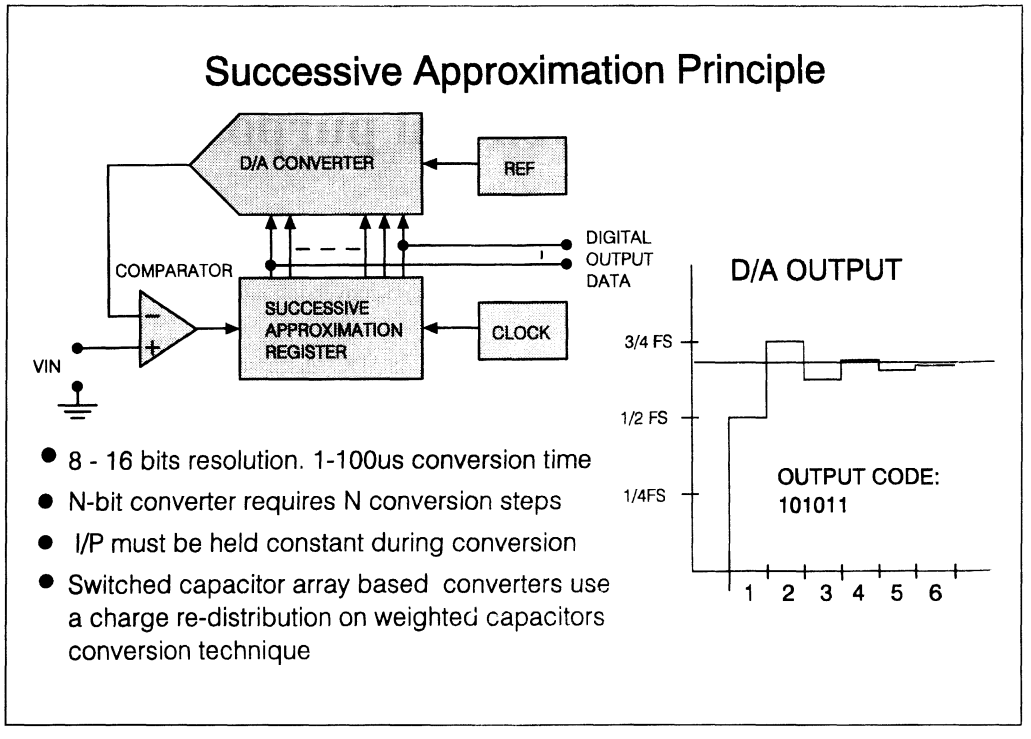


Figure 3.2.1 - Successive Approximation Principle

While the successive approximation converter process continues, the input signal must be held constant using a sample and hold circuit in front of the comparator. More recent successive approximation converter designs, use switched capacitor networks, utilizing charge redistribution, to replace resistive ladder DACs. This is due to the switched capacitor technique's smaller chip area, higher speed and inherent sample and hold function. Texas Instrument's Advanced LinCMOS technology with its double polysilicon layers is an ideal process for building well matched switched capacitor circuits for successive approximation ADCs.

- **Switched capacitor ADCs have an inherent sample-and-hold.**

2.2. The Input of a Switched Capacitor ADC

The I/P equivalent circuit of TI's TLC1540 family, TLC1550 family and TLC1225 family of ADCs looks like a capacitor to ground during the sampling phase and an open circuit during the conversion phase of the ADC cycle.

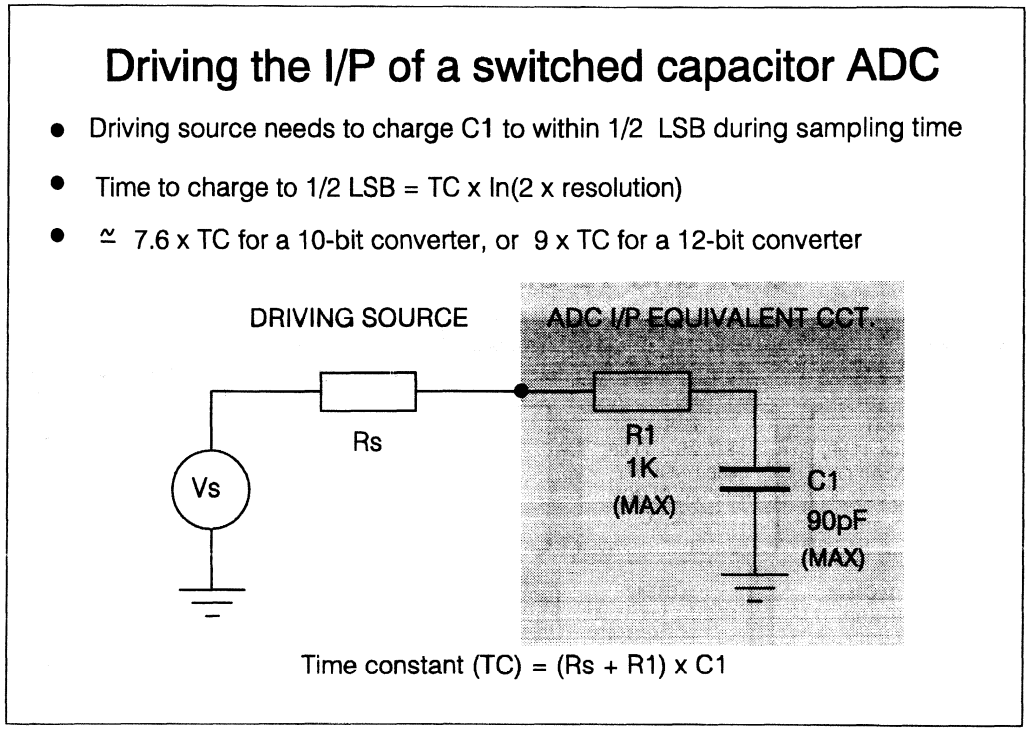


Figure 3.2.2 - Driving the I/P of a Switched Capacitor ADC

For accurate operation of the ADC, the capacitor must be charged to the required accuracy of 1/2LSB (or more, depending on your system error budget) during the sampling phase of the ADC cycle.

The voltage V_C on capacitor C1 is given by $V_C = V_S\ (1 - e^{-t/TC}\ )$

where TC is the time constant $C_1(R_S+R_1)$

So

$$e^{-t/TC} = (1 - \frac{V_C}{V_S})$$

$$-t/TC = \ln(1 - \frac{V_C}{V_S}\ )$$

Hence time taken to settle to 1/2 LSB is

$$t = -TC \cdot \ln\left(1 - \frac{V_S - \frac{1}{2}LSB}{V_S}\right) = TC \cdot \ln(2.RESOLUTION)$$

For a 10 bit converter this would be TC x ln(2 x 1024) $\approx$ 7.6 x TC.

This therefore sets a maximum limit on the source impedance when driving into a capacitive ladder ADC. For the TLC1540 family, TLC1550 family and TLC1225 family of ADCs, the maximum value of C1 is 90pF and there is an internal series resistance of 1KΩ for (ESD protection).

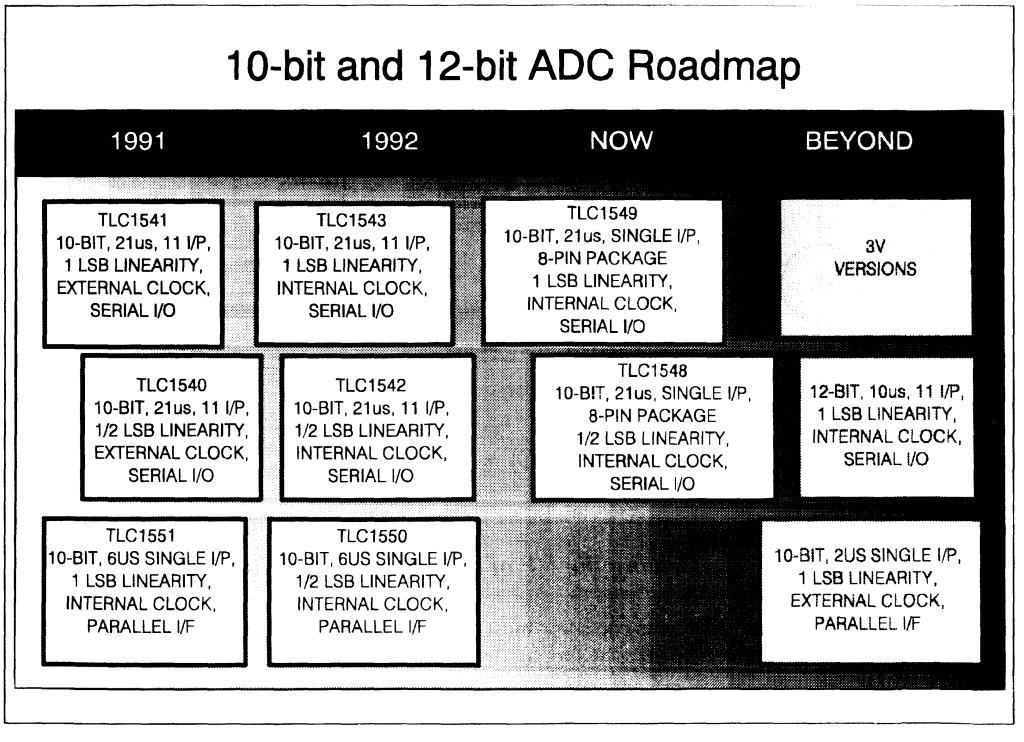


Figure 3.2.3 - 10-bit and 12-bit ADC Roadmap

Figure 3.7 shows the current product range for the TLC1540 family and TLC1550 family of ADCs and the technical direction TI is pursuing.

2.3. TLC1540 Family of ADCs

The TLC1540 family of ADCs are 10-bit serial O/P devices with a conversion time of 21us. They are available in commercial temperature range (0^{o}C to $+70^{o}$C) and industrial temperature range (-40^{o}C to $+85^{o}$C).

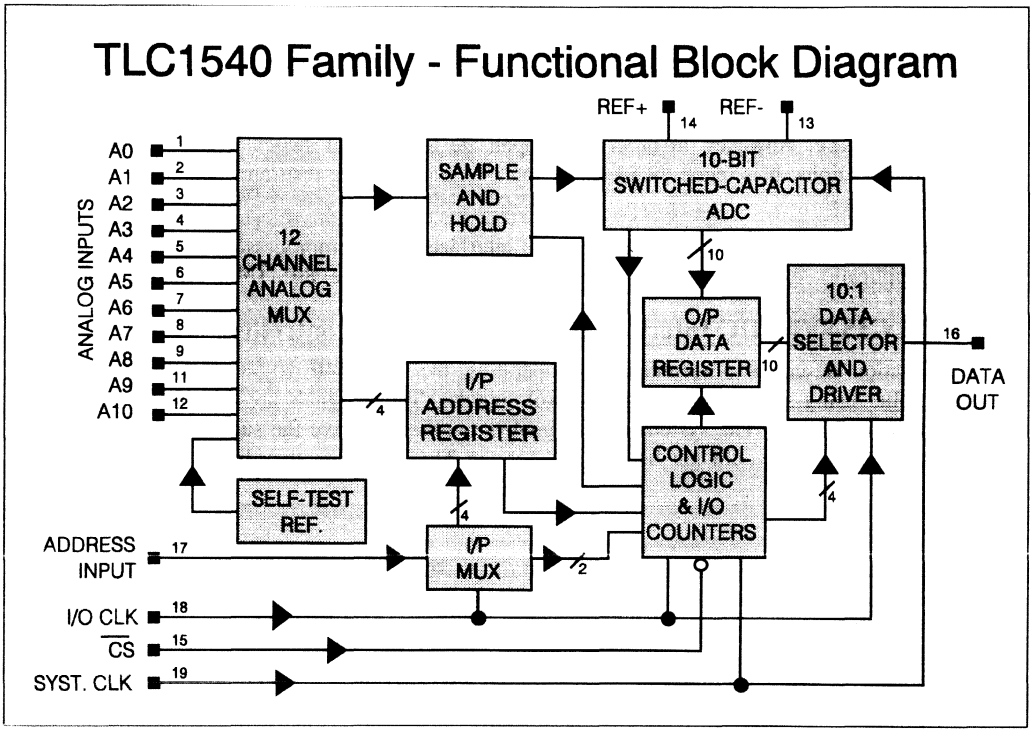


Figure 3.2.4 - TLC1540 Family Functional Block Diagram

The TLC1540 through TLC1543 ADCs all feature a 12-channel I/P multiplexer giving 11 analog inputs and 1 self-test I/P. The TLC1540/1 require an external system clock on pin 19 while the TLC1542/3 have an internal system clock and use pin 19 to provide an End-of-Convert (EOC) output.

The complete conversion cycle takes 30us which consists of 21us (T_{CONV}) plus 10 I/O clocks which, at the maximum rate of 1.1MHz is 9us

Therefore the maximum sampling frequency for a system using a TLC1540 family device is:

$$f_s\big|_{MAX} = {}^{1}\!/_{30\text{us}} = 33.3KHz$$

Six of the I/O clocks are used for the sampling time. So at the maximum I/O clock rate there is approx. 5.4us available to charge the I/P capacitance of the ADC to the required accuracy. This will then give

the maximum allowable source impedance for driving the TLC1540 family at max. Fs for 1/2 LSB error of the capacitor voltage.

t = TC x ln(2 x RESOLUTION). So substituting the above values we get:-

$$5.4x\ 10^{-6} = R\big|_{MAX}\ x\ 90x10^{-12}x\ \ln(2^{11})$$

$$\therefore\ R\big|_{MAX} = \frac{5.4x\ 10^{-6}}{90x10^{-12}x\ 7.6} = 7.9x\ 10^{3}\Omega$$

As there is already an internal resistance of 1KΩ, the maximum source impedance for full speed operation is 6.9KΩ. However, in order to compensate for internal switch resistance and external temperature variations, it is recommended that the maximum source resistance should be no greater than half this value.

All the devices in this family have a simple serial interface to a microprocessor or peripheral and the following application example shows the interface to the, popular, Intel 8051™ microcontroller.

2.3.1. TLC1540/1 ADC Interface to Intel 8051 Microcontroller

This application describes a technique for operating the TLC1540 10-bit ADC with the 8051 microcontroller using software generated control signals. These signals are CS, I/O clock, address input, and system clock. The system clock signal is required to drive the successive approximation conversion process and would not be required for the TLC1542/3 as they have an internal system clock.

Hardware

The system clock is derived from the ALE signal of the 8051 device. Another method uses a signal that is tapped off the oscillator through a high impedance buffer or inverter and divided down to the appropriate frequency. Care should be taken when using the ALE signal for the TLC1541 system clock to ensure that the high and low pulse widths are within specifications. The ALE signal is dependent upon the oscillator frequency and may not meet pulse width specifications at high oscillator frequencies.

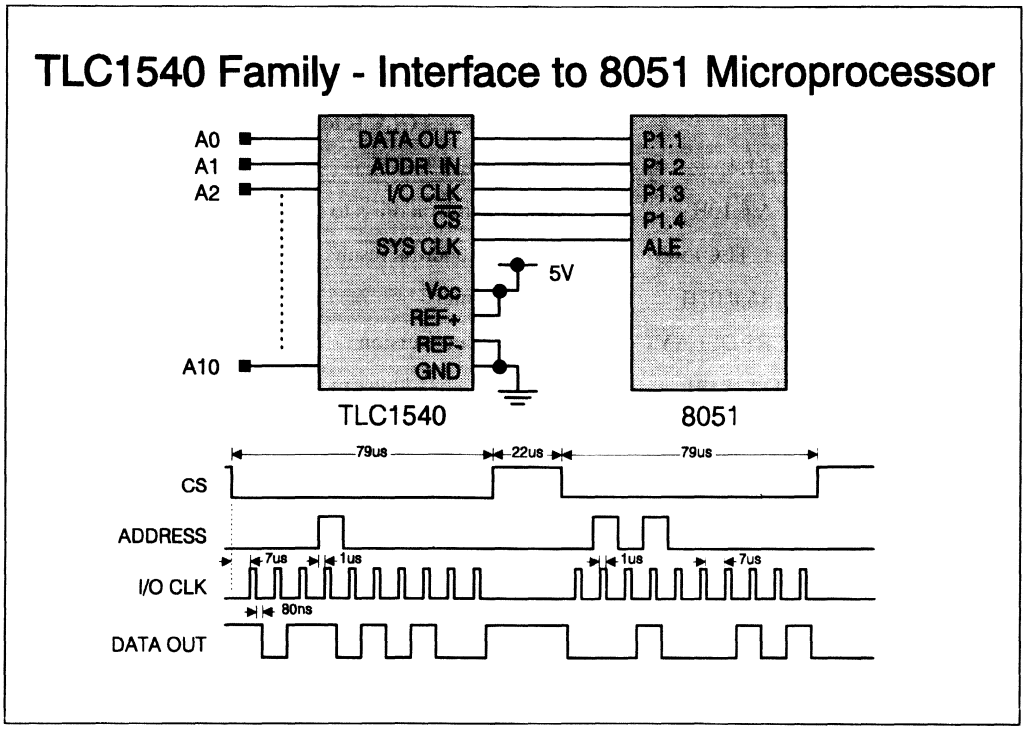


Figure 3.2.5 - TLC1540 Family Interface to 8051 Microcontroller

The subroutine can be executed in 79 µs. With a system clock of 2.1 MHz from the ALE pin, conversion results may be read every 101 µs.

Software

All interface control signals are generated through software manipulation of port pins. A subroutine is used to load a new multiplexer address and retrieve a previous conversion result. A listing of the subroutine follows this discussion.

A multiplexer address should be loaded into the most significant 4 bits of the accumulator before calling the subroutine. Previous conversion results are returned left justified, with R2 holding the eight most significant bits and R3 holding the two least significant bits. After returning from the subroutine, a delay loop is executed to allow time for the conversion. Conversion requires 44 system clock cycles, therefore, delay loops of appropriate length should be included according to the system clock frequency.

Software List for TLC1540 Family to Intel 8051 Microcontrollers

Main Program

```
START:      MOV P1,# 02H        ; Initialize port 1 I/O pins
            CLR P1.3            ; Make sure I/O CLK is low
            SETB P1.4           ; Make sure /CS is high
CONTINUE    MOV A.# 10H         ; Initiazlie muxaddress to channel 1
            ACALL TLC1540       ; Shift muxaddress/results
            MOV R5,# 07H        ; Load counter
DELAY 1:    DJNZ R5,DELAY1      ; Delay for conversion
            MOVOA, # 0H         ; Initialize muxaddress to channel 5
            ACALL TLC1540       ; Shift muxaddress/results
            MOV R5,# 07H        ; Load counter
DELAY2:     DJNZ R5,DELAY2      ; Delay for conversion
```

Subroutine

```
TLC1540     MOV R4,# 08         ; Load counter
            CLR P1.4            ; Bring /CS low
            NOP                 ; Delay for /CS to go low
            NOP                 ;
LOOP:       MOV C,P1.1          ; Read data bit into carry
            RLC A               ; Rotate into accumulator
            MOV P1.2,C          ; Write muxadd bit out
            SETB P1.3           ; I/O clock high
            CLR P1.3            ; I/O clock low
            DJNZ R4,LOOP        ; Go back and get another bit
            MOV R2,A            ; Store MSB'S in r2
            MOV C,P1.1          ; Read data bit into carry
            CLR A               ; Clear accumulator
            RLC A               ; Rotate data bit into accumulator
            SETB P1.3           ; I/O clock high
            CLR P1.3            ; I/O clock low
            MOV C,P1.1          ; Read data bit into carry
            RRC A               ; Rotate right into accum MSB
```

```
RRC A                   ; Rotate right into accum MSB
MOV R3,A                ; Store LSB'S in R3
SETB P1.3               ; I/O clock high
CLR P1.3                ; I/O clock low
SETB P1.4               ; Bring /CS high
RET                     ; Return to main program
```

2.3.2. TLC1549 Single Input, 10-bit ADC

Available in 8-pin DIL or 8-pin SOIC, the TLC1549 is a 10-bit ADC for applications requiring only 1 input and/or where space is at a premium. It features the same ADC as the TLC1543 but without the input multiplexer.

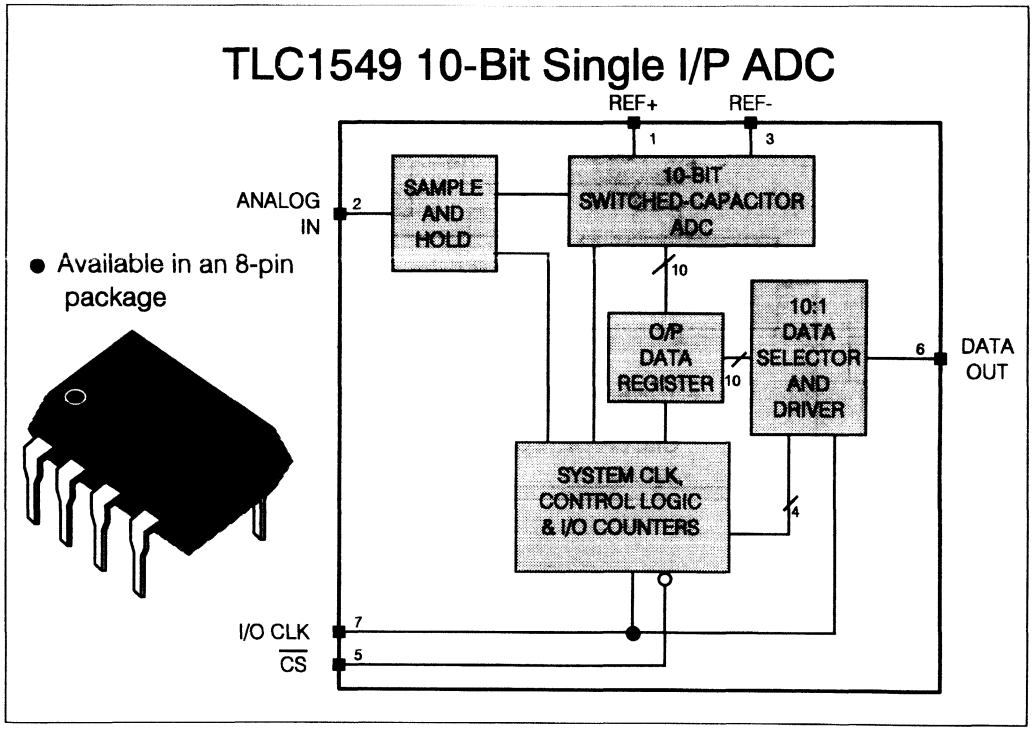


Figure 3.2.6 - TLC1549 10-bit Single Input ADC

2.4. TLC1550 Family of ADCs

The TLC1550 and TLC1551 are 10-bit, parallel O/P ADCs designed for easy interface to DSP. Their features include:

- **Low power dissipation (40mW maximum)**
- **Parallel interface**
- **External or internal clock**
- **6us conversion time**
- **±0.5 LSB total unadjusted error - TLC1550**
- **±1.0 LSB total unadjusted error - TLC1551**

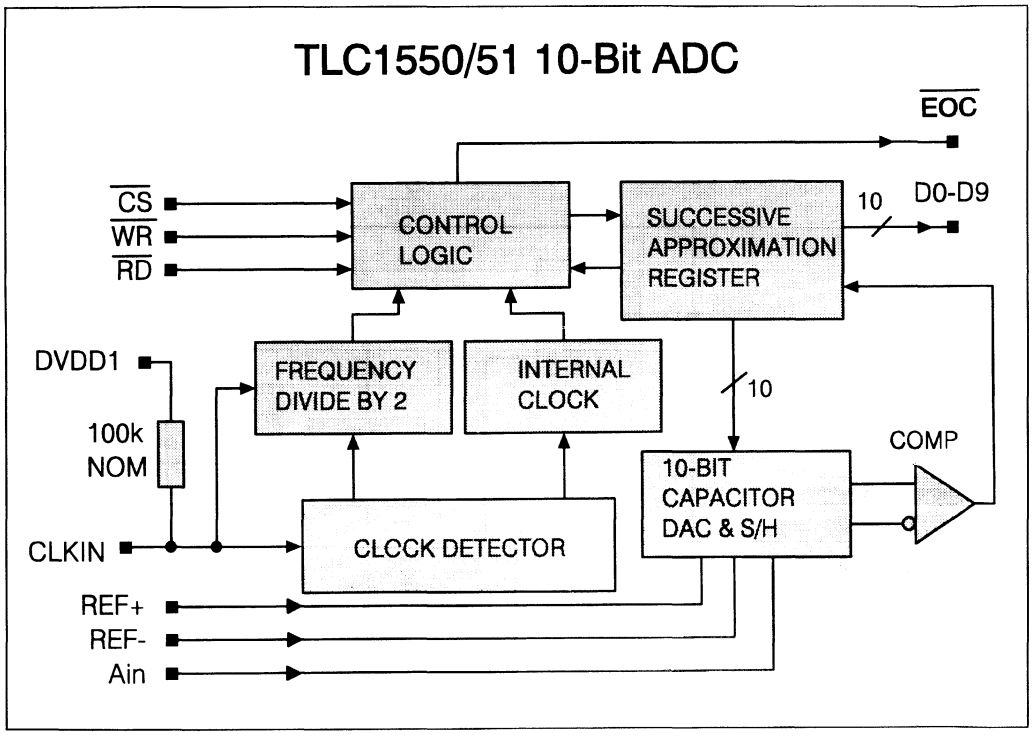


Figure 3.2.7 - TLC1550/1 10-bit ADC Functional Block Diagram

The TLC1550 ADC will sample its analog I/P from the rising edge of $\overline{EOC}$ to the rising edge of the next $\overline{WR}$ pulse. So consideration must be given to the required sampling accuracy (as previously described) when determining the timing of these signals.

2.4.1. A Control System using the TLC1550 and TMS320C14

Electromechanical control systems are used in automobiles, appliances, industrial controls and many other systems. Today most control system designs are digital signal processor (DSP) based. A DSP based system, such as the one below, typically consists of one or more sensors, an analog-to-digital converter (ADC), a DSP and an actuator system.

DSP-based systems offer several advantages over conventional control systems. For example:

- **Replacing large look-up tables with mathematical equations reduces ROM requirements.**
- **Use of software models reduces the need for expensive linearized sensors.**
- **A DSP calculation result can be more accurate than a linear interpolation.**
- **The high processing power of a DSP enables use of advanced control algorithms.**
- **Using a DSP and a single ADC reduces the need for additional precision components.**
- **DSP implementation of real time system diagnostics can improve system reliability and reduce cost.**

To give design engineers the full advantage of a DSP-based approach, TI has designed the TMS320C14 DSP microcontroller and the TLC1550 10-bit ADC. These components can be used to simplify designs and increase performance.

TLC1550 A/D Converters

The TLC1550 features high speed (6 us conversion) combined with a 10-bit parallel data bus, making it possible to use a single ADC with multiple sensors. The parallel bus also allows for easy interface the TMS230C14. The control system schematic includes the signal conditioning and multiplexing necessary to utilize multiple sensors.

TLC1550 / TMS320C14 System Benefits

- **Fast Operation**
- **Accurate control**
- **CMOS technology reduces system power requirements**
- **Design Flexibility**
- **Simple A/D & DSP Interface**

TMS320C14 DSP Microcontroller

The TMS320C14 combines a digital signal processor with microcontroller peripheral functions. The DSP core provides the processing power of a hardware multiply and 32-bit ALU. This processing power combined with a clock frequency of 25 MHZ makes possible the use of advanced control software. The peripheral functions provide interfaces to other system functions with a minimum of external components. This enables the TMS320C14 to be used in a variety of control applications. The TLC1550 and the TMS320C14 are both implemented in CMOS technology, minimizing system power

dissipation and requiring only a single 5V power supply. This further simplifies the design requirements for the system that follows.

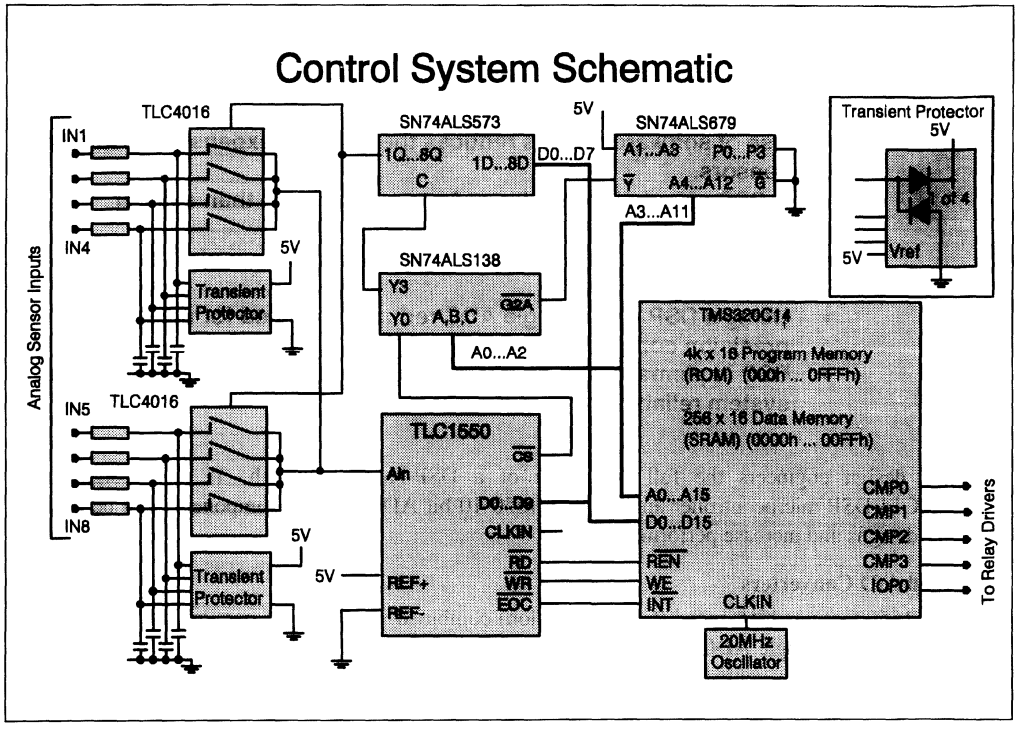


Figure 3.2.8 - TLC1550, TMS320C14 Control System

Design Considerations

Since most control applications require more than one analog input, two 4-channel analog switches (TLC4016) are interfaced as multiplexers to the analog input (A_{in}) of the TLC1550. The selection of one of these eight analog inputs is done via the transparent latch (SN74ALS573) with an OUT instruction to I/O port address PA3 and the appropriate data. Each of the eight analog inputs has a separate circuit for transient protection and filtering. The resistor and capacitor network provide a simple low pass filter. The diode circuit labeled "transient protector" is used to conduct transients to ground or 5V, thus protecting the input circuitry.

The TMS320C14 can address the TLC1550 as an external memory. In order to use the simple IN and OUT instructions of the DSP-controller, the TLC1550 is mapped into the I/O port address range 1111 1111 1xxx. This is accomplished by simply decoding the 9 address lines (A3 - A11) using the SN74ALS679. The decoder output Y enables the 3-line to 8-line decoder SN74ALS138, to chip select

$\overline{CS}$ of the analog-to-digital converter. In this configuration, the TLC1550 can be selected via I/O port PA0.

The write ($\overline{WR}$) and read ($\overline{RD}$) signals are only valid when $\overline{CS}$ is active low. An OUT instruction on PA0 sets $\overline{CS}$ low, permits sampling to begin with an $\overline{EOC}$ high signal and initiates the hold mode with a $\overline{WR}$ high signal.

After entering the hold mode, the internal clock controls the conversion automatically. When the conversion is complete, the end of conversion $\overline{EOC}$ goes low, indicating that the digital data has been transferred to the output latch. Lowering $\overline{CS}$ and $\overline{RD}$ resets and $\overline{EOC}$ transfers the result to the data bus for the TMS320C14 read cycle.

Analog Channel Addressing

0000	0000	0000	0001	(1H)	=	Channel IN1
0000	0000	0000	0010	(2H)	=	Channel IN2
0000	0000	0000	0100	(4H)	=	Channel IN3
0000	0000	0000	1000	(8H)	=	Channel IN4
0000	0000	0001	0000	(10H)	=	Channel IN5
0000	0000	0010	0000	(20H)	=	Channel IN6
0000	0000	0100	0000	(40H)	=	Channel IN7
0000	0000	1000	0000	(80H)	=	Channel IN8

Channel Selection Routine

```
lack    4               ; load accumulator with 4
sacl    four            ;store 4 into four
out     portadr,bsr     ;select band FFFF (hex) - ports PA0 - PA6
out     four,PA3        ;select analog channel IN3
```

Note: To avoid analog I/P conflicts, only one logic high should be written to the octal D-latch.

A to D Conversion Routine via Polling

```
init    ldpk    0           ;
        larp    0           ;
        dint                ; disable all interrupts
sel     lack    1           ;load accu with 1
        sacl    one         ;store 1 into one
        zac                 ;clear accu
        sub     one         ;0000h-0001h=FFFFh
        sacl    portadr     ;FFFFh->portadr
        out     portadr,bsr ;select bankFFFFh (ports pa0 - pa6)
        out     one,pa3     ;select analog channel IN1
        nop                 ;these nop instructions
        nop                 ;allow the I/P voltage
        nop                 ;to settle
conv    out     dummv,pa0   ;start conversion
        call    wait        ;
        in      advalue,pa0 ;read conversion result
        lac     mask        ;load mask 03FF for 10 bits
        and     advalue     ;mask conversion result
        sacl    advalue     ;store 10-bit conversion result
        b       conv        ;
wait    lark    0,value     ;
wait1   nop                 ;delay loop of 6us to allow conversion
        banz    wait1       ;
        ret                 ;
```

2.5. Self calibrating 12 bit plus sign ADC - The TLC1225

TLC1225 is a 12-bit-plus-sign successive approximation ADC utilizing a self-calibration technique to eliminate expensive trimming of thin-film resistors at the factory. Additionally, this technique ensures excellent long term stability, avoiding regular field trimming to maintain conversion accuracy.

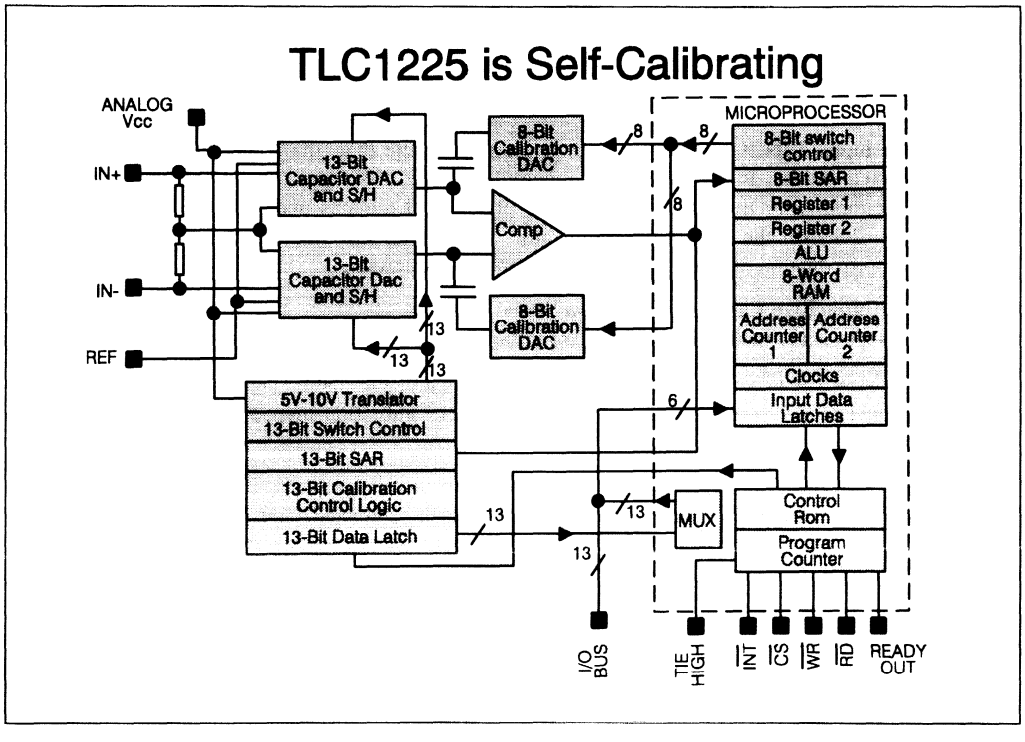


Figure 3.2.9 - Self calibrating 12 bit plus sign ADC - The TLC1225

The design uses a switched capacitor based charge redistribution technique for the conversion. As 12-13 bits accuracy of capacitor matching is difficult to achieve, seven of them are calibrated during a non-conversion, capacitor-calibrate cycle in which all seven of the capacitors are calibrated at the same time. The calibration or conversion cycle may be initiated at any time by issuing the proper command word to the data bus.

TLC1225 Self calibrating ADC

- **Self calibration eliminates expensive trimming**
- **0V to 5V Unipolar or -5V to +5V Bipolar ranges**
- **12us conversion time**
- **True differential inputs**
- **Low Power . . . 85mW max.**

Calibration cycle (simplified description)

Comparator Offset Calibration Steps:

Step 1 : The input, VIN is shorted to GND in order to ensure that the comparator input is zero. A coarse offset calibration is performed by manipulating the offset error using switches and offset storage capacitors. After this action some of the offset still remains uncalibrated. Step 2 : An A/D conversion is done on the remaining comparator offset with the 8 bit calibration DAC and 8 bit successive approximation register. The result is stored in the RAM.

13 Bit DAC Capacitive Ladder Calibration Steps:

Step 1: The input is internally disconnected from the 13 bit capacitive DAC.

Step 2: The MSB capacitor is tied to VREF, while the rest of the ladder capacitors are tied to GND. The ADC conversion result from the Comparator Offset Calibration Step 2 above, is retrieved from the RAM and is input to the 8 bit DAC.

Step 3: Step 1 of the Comparator Offset Calibration sequence is performed. The 8 bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.

Step 4: Now the MSB capacitor is tied to GND, while the rest of the capacitors are tied to VREF. An MSB capacitor voltage error on the comparator output capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8 bit word and stored in the RAM.

Step 5: The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Step 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

Conversion Cycle (simplified description)

Step 1: Step 1 of the Comparator Offset Calibration sequence is performed. The remaining offset obtained in Step 2 of the Comparator Calibration sequence, is retrieved from the RAM and is input to the 8 bit DAC. Thus, the comparator offset is completely corrected.

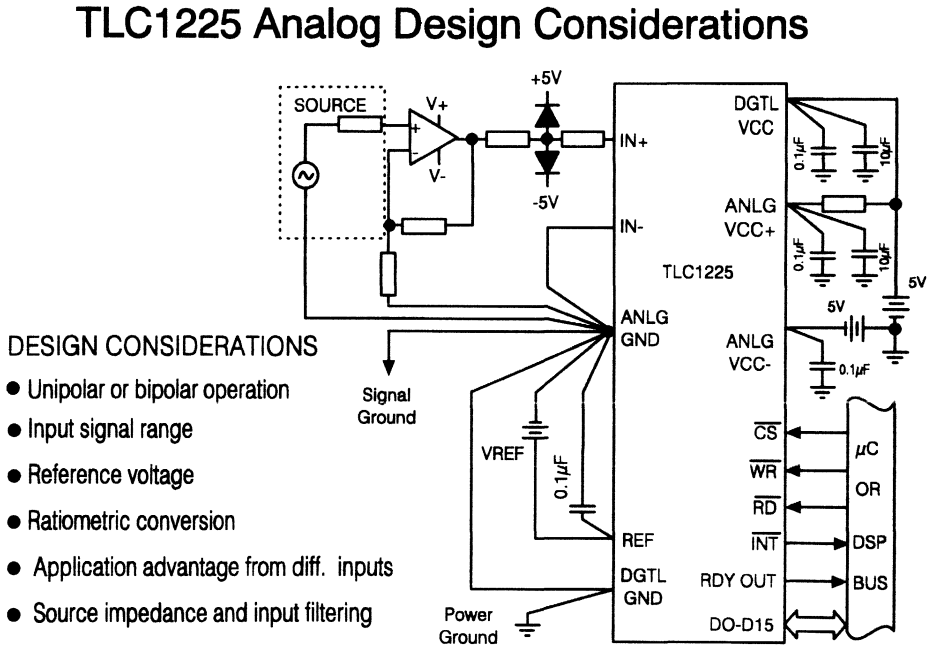
Step 2: The input signal, VIN is sampled onto the 13 bit capacitive ladder.

Step 3: The 13 bit ADC conversion is performed. As the successive approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in the 8 bit successive approximation register. This register controls the 8 bit DAC so the total accumulated error for these capacitors is subtracted out during the conversion process.

A conversion takes only 12us. A calibration cycle takes 4 times longer. Calibration is required upon power-up to achieve full accuracy. Regular recalibration is recommended to avoid drift. This is particularly true in systems where self-heating or environmental temperature changes occur.

TLC1225 Analog design considerations

When designing with a medium to high resolution converter like the TLC1225 several fundamental considerations have to be made.



TLC1225 Analog design considerations

Power supply

The device features a 0 to 5V analog input range with a single +5V supply voltage (Unipolar configuration) or -5 to +5V analog input range with +/-5V supplies (Bipolar configuration). The choice of the configuration depends on the application and available supply voltages.

Proper supply grounding of both digital and analog supplies are required as shown. Avoid ground loops that inductively could pick up hum. Also, signal ground leads should only carry the return current from the signal source. Any additional current may cause a voltage drop and result in system errors. Noise spikes on the supply lines can also cause conversion errors.

All supply input pins should be bypassed by 1 to 10uF low inductance capacitors with short leads. Further high frequency decoupling can be achieved with a 100nF ceramic capacitor, placed in parallel with the aforementioned tantalum capacitors. A separate regulator for the TLC1225 or other analog circuitry will greatly reduce digital noise on the analog supply line.

Differential inputs

The device is provided with a true differential input structure. This can be utilized to reduce effects of noise and hum signals common to both input wires. Common-mode noise often appears where long input leads are used or in noisy environments. There is no time interval between the sampling of IN+ and IN- input so these are truly differential and simultaneous sampling rejects even high frequency common-mode signals within the bandwidth of the ADC. Keep IN+ and IN- input leads twisted and their PCB tracks close together.

The true differential input structure allows for simple interface to differential sources such as some strain-gauge configurations. Also, the input can often save a pre-processing differential instrumentation amplifier or act as the third amplifier in such a configuration.

Noise constraints

A general rule of thumb is that the input leads should be kept as short as possible and that the source impedance should be as low as possible.

Long input leads can pick up noise from a digital clock signal with edges too fast for the differential input amplifier's common-mode rejection. This noise can cause conversion errors. Input bypass capacitors may be used for noise filtering. However, the charge on these capacitors will be depleted during the input sampling process when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source impedance must keep pace with the charge depletion of the bypass capacitors during the sampling sequence. The above phenomenon becomes more significant as source impedance and conversion rate increases. For source impedances below 100 Ohm, a 1nF bypass capacitor at the input will prevent pick-up due to series lead inductance of a long wire.

Even in applications without an input bypass filter capacitor, high source impedance can cause a voltage drop when charging the internal capacitors during the sampling phase. Note, that some op amps, when used as signal source, have high output impedance for the current spikes required to charge the internal capacitors of the TLC1225.

Signal conditioning

The input signal range is limited by the supply voltages which means 0 to 5V in unipolar mode and -5 to +5V in bipolar mode of operation.

In either mode, when using a signal conditioning op amp supplied from the same analog supply (supplies), you will need an output swing to the supply rails within a fraction of a millivolt. No op amp can guarantee this performance but some come very close. The LinCMOS precision op amp TLC2201 has a complementary CMOS output state that can swing very close to either rail when not loaded. In addition, it can operate with a single +5V supply as well as with +/-5V supplies. Using this op amp eliminates adjustment of the input range, but a few codes in both the top and bottom of the ADCs dynamic range will be missed due to the limited output swing. A worse limitation is often the accuracy and stability of the power supply (supplies) limiting the input range significantly, even if 1% voltage regulators are used.

For applications demanding high frequency signal conditioning a faster precision op amp like the TLC2027/37 should be employed. However, such op amps have not got rail-to-rail output swing so higher supply voltages must be used. If +V and -V exceeds the ADC supplies, precautions must be taken to avoid over-voltage on the ADC's input pins. A suitable protection can be accomplished by a small series resistor (preferable a PTC resistor) followed by schottky clamping diodes to either supply. To ensure that the bulk of current from any over-voltage will flow in the schottky diodes rather than in the ADC's internal ESD protection circuitry, an additional small series resistor can be added in series with the input. The maximum input current for the ADC caused by over-voltage should be kept well below $\pm 5mA$.

Mode of operation

The ADC can be used in either absolute or ratiometric reference applications. In an absolute reference system, where the analog input varies between very specific voltage limits, a 13 bit precision voltage source reference is required. An example of such an application is a temperature measuring system using a sensor, which provides 10mV/°C independent of the supply voltage.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the REF pin can be tied to the ADC's positive supply. This technique relaxes the stability requirement of the system

reference as the analog input and the ADC reference move together maintaining the same output code for a given input condition. An example of a ratiometric transducer is a strain-gauge bridge supplied directly from the system power supply. Often both the VIN- and the REF pins are tied to the system power supply via resistive voltage dividers to define an input dynamic range window slightly smaller than that of the supply voltages. This allows a driving op amp to operate at the same supplies as the ADC without needing rail-to-rail swing.

Reference input

The restrictions on the source impedance for the analog inputs also applies to the reference input. In addition, noise from the reference must be kept at a minimum by careful decoupling of both low and high frequency noise.

In summary, precision 12 bit ADCs require some adjustments to compensate for offset errors. The TLC1225, with its self-calibration facility ensures low and stable offset with time and temperature eliminating initial trimming and re-adjustment due to aging.

2.5.1. Interface of the TLC1225 A/D Converter to the TMS320C25

Advanced control systems often combine data acquisition circuits with digital signal processors (DSPs) to provide real time control of complex mechanical equipment. The system performance depends on both the selection of key components as well as efficient interface design.

An automotive active suspension system is an example of a complex mechanical system suited for DSP control. The block diagram below describes a typical system. The major parts of the system are sensors, analog-to-digital converter (ADC) interface, ADC, ADC-to-DSP interface and DSP-to-pump interface.

A control system such as this requires a fast, accurate ADC and a high-speed DSP. The TLC1225 ADC features 12-bit accuracy, 12-µs conversion time and a parallel interface for high speed. The

TLC1225 combined with a TMS320C25 DSP offers a cost effective solution to the automotive active suspension system design.

The complete suspension system contains three separate interface circuits. Each interface is important; however, this application brief covers only the ADC-to-DSP interface. The designer must consider the timing requirements for both the DSP and ADC in order to produce a simple, cost effective interface.

The ADC-to-DSP interface consists of three functions: clock generation, chip select and ready generation. Several clock circuit options are discussed, based on different system speed requirements.

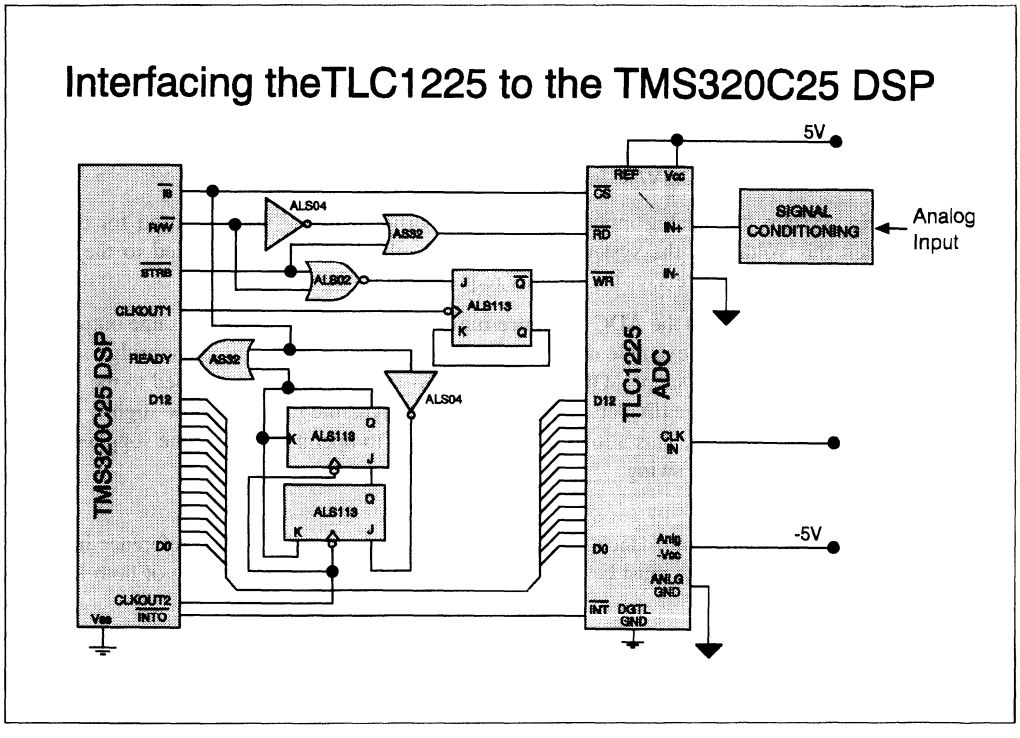


Figure 3.2.10 - Interfacing the TLC1225 ADC to the TMS320C25 DSP

Clock Generation

Separate clock signals are required for the TLC1225 and the TMS320C25. Although each clock is a different frequency, the TLC1225 clock can be generated from the TMS320 CLKOUT1 signal.

The TLC1225 requires 24 clock cycles to perform an A/D conversion, regardless of its input clock frequency. Therefore, if minimum A/D conversion times are desired, the TLC1225 should be run at its maximum input clock frequency of 2 MHz.

The interface presented here is designed to be compatible with either the standard TMS320C25-40 operating at up to 40 MHz, or the enhanced performance TMS320C25-50 operating at up to 50 MHz. With the TMS320C25-40 operating at its maximum rate, its output clock frequency is 10 MHz. If

system requirements dictate that both devices be run at their maximum rates, external circuitry can be used to divide the TMS320C25 output clock by five, or an external oscillator may be used to provide a 2-MHz clock for the TLC1225.

Other approaches may be employed to provide a clock for the TLC1225 if input clock frequencies for either the TLC1225 or the TMS320C25 may be reduced. For example, if the speed of the TMS320C25 can be reduced to 32 MHz, a simple external circuit can be used to divide one of its clockout signals by four. This approach, which requires a minimum of inexpensive external logic, is illustrated in the application circuit shown here.

In contrast, if the TLC1225 input clock can be decreased to 1.25 MHz, the TMS320C25 may still be run at 40 MHz and its clockout divided by eight. If the high performance of the TMS320C25-50 is required, an extension of one of these approaches may be used to provide a clock signal for the TLC1225.

Chip Select

In this application, $\overline{IS}$ (the TMS320C25 I/O space select signal) is used as the chip select for the TLC1225. This approach is appropriate if the TLC1225 is the only device mapped into the TMS320C25 I/O space. If other devices are mapped into the I/O space, a unique chip select must generally be decoded for each device using the IS signal and address bus information. If this approach is used with the application circuit presented in this document, the same signal used to provide $\overline{CS}$ for the TLC1225 should also be connected to the ready generation circuitry.

Generation of a decoded $\overline{CS}$ signal must meet the timing requirements for the TLC1225 in addition to meeting the timing requirements for the TMS320C25 ready generation. On the TLC1225, $\overline{CS}$ must occur early enough with respect to $\overline{WR}$ and $\overline{RD}$ to meet the timing requirement. However, because two wait states are used when interfacing the TLC1225 and the TMS320C25, this requirement is easily met, even if relatively slow decode logic is used. In fact, timing requirements for ready generation typically dominate chip select decode considerations. Specifically, if the ready generation logic is driven directly by the same signal used for $\overline{CS}$ on the TLC1225, in order to meet the TMS320C25 timing requirements, this signal may be delayed from address by no more than 18 ns (8 ns for the TMS320C25-50). This includes the 5.8 ns 74AS32 propagation delay, which leaves 12.2 ns for decoding (2.2 ns on the TMS320C25-50).

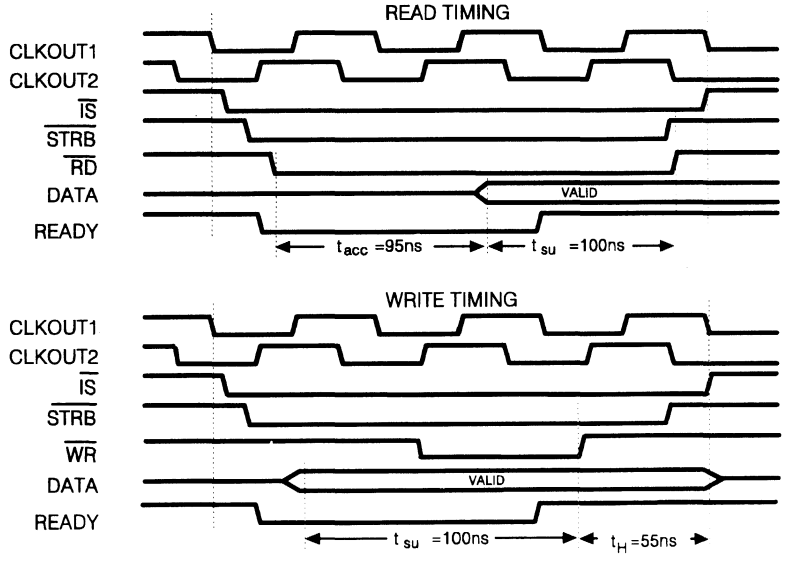
Ready Generation

In many case, in order to facilitate ready signal generation, wait state devices may often be grouped together within a coarse address segmentation, or even in the same logical space (for example, I/O), with a signal requiring little or no decoding used to initiate a wait state. Once a wait state is initiated, then decode logic is allowed significantly longer to respond with a signal indicating ready status. This concept is discussed in greater detail in the TMS320C2X User's Guide (Document Number SPRU014B) Hardware Applications Section.

As mentioned previously, two wait states are used when interfacing the TLC1225 and the TMS320C25. This is implemented with two 74ALS113 flip-flops, which delay the signal indicating a TLC1225 access (IS, in this case) by two TMS320C25 CLKOUT2 cycles. Therefore, when the TLC1225 is first accessed, IS goes low, also driving ready low, and a wait state is initiated. Then after two clock cycles, a ready indication meeting the TMS320C25 timing requirements is generated, terminating the I/O access.

The interface described here has been implemented as a normally ready system. In a normally ready system, ready is normally asserted and de-asserted early in cycles where wait states are required. Fast devices which require no wait states are not required to respond, thereby simplifying the system design.

TLC1225 / TMS320C25 System Timing Diagram



System Timing Diagram

Read and Write Cycle Operation

Read Cycle - A read cycle is initiated with $\overline{IS}$ going low, which selects the TLC1225. At this time, R/W also goes low, signifying a read operation; $\overline{RD}$ remains high, since $\overline{RD}$ is the AND of inverted R/W and STRB. When STRB goes low, $\overline{RD}$ goes low and the two wait state access allows the TLC1225 approximately 180 ns to provide data to the TMS320C25, which the TLC1225 easily meets with its 95 ns read access time. The cycle terminates when ready is sampled high during the third cycle of the access, and STRB goes high, causing $\overline{RD}$ to go high. Finally, $\overline{IS}$ goes high, de -selecting the TLC1225.

Write Cycle - A write cycle is initiated in the same manner as a read, with $\overline{IS}$ going low, which selects the TLC1225. At this time $R/\overline{W}$ also goes low. When STRB subsequently goes low, this causes the output of the 74ALS02 to go high, signifying a write cycle.

The TLC1225 requires a data setup time of 60 ns and a hold-up time of 50 ns with respect to the rising edge of $\overline{WR}$. The 74ALS113 flip-flop is used to detect a write from the TMS320C25, wait until the next falling edge of CLKOUT1, and generate a $\overline{WR}$ pulse. $\overline{WR}$ is only active during the second CLKOUT1 cycle of the two wait state (three cycle) access. The Q output of the flip-flop is connected back to the J input, causing the $\overline{WR}$ pulse to be terminated by the next CLKOUT1 cycle.

Thus, the rising edge of $\overline{WR}$ occurs at least 100 ns after data becomes valid and at least 55 ns before data becomes invalid, easily satisfying the TLC1225 interface timing requirements.

Once $\overline{WR}$ goes high, it stays high since STRB goes high before the next falling edge of CLKOUT1. the cycle terminates when ready is sampled high during the third cycle of the access, and STRB goes high, causing the output of the 74ALS02 to go high. Finally, IS goes high, de -selecting the TLC1225.

System Considerations

The TMS320C25 is a high-speed processor and, accordingly, executes fast bus cycles. TLC1225 data bus timing specifications are such that, if other external TMS320C25 bus cycles follow immediately after reading the TLC1225, data bus conflicts are likely to occur. Isolation between data buses on the two devices may be accomplished using high impedance buffers, such as the 74ALS244 or an equivalent, but an increase in system cost is incurred. In order to avoid this, system software may be designed to guarantee that external TMS320C25 cycles do not occur in the cycle after reading the TLC1225.

System software may be partitioned such that the code executes from internal memory when reading the TLC1225, and that at least one NOP instruction is executed before resuming external bus activity. This will prevent unwanted external cycles.

Since this system is designed to implement a minimal glue logic interface, the 74ALS02 used to detect write cycles does not distinguish between writes to different devices. Accordingly, a write to any external device generates a $\overline{WR}$ pulse. This does not cause spurious writes to the TLC1225 since $\overline{CS}$ is high. When devices other than two wait state devices are written to immediately prior to writing to the TLC1225, an inappropriately timed $\overline{WR}$ signal may be generated, and an improper write cycle may occur. Accordingly, writes to other external devices should not be performed immediately prior to writing to the TLC1225 especially those requiring other than two wait states.

If system requirements dictate, however, this can be avoided by including the TLC1225 chip select signal as a term in the signal used to drive the J input to the 74ALS113. This can be accomplished by using a three-input NOR gate such as a 74ALS27 or equivalent, in place of the 74ALS02. Thus, the J input will be driven high only when writes are performed to the TLC1225.

2.6. TLC32071 - A Complete Analog I/O System on a Chip

The TLC32071 is a complete analog I/O system on a chip with easy DSP interface.

The primary application is the interface between analog control signals and digital signal processing within motor control loops. Other uses include industrial controls, system performance control, and transducer interface to the digital processing channel.

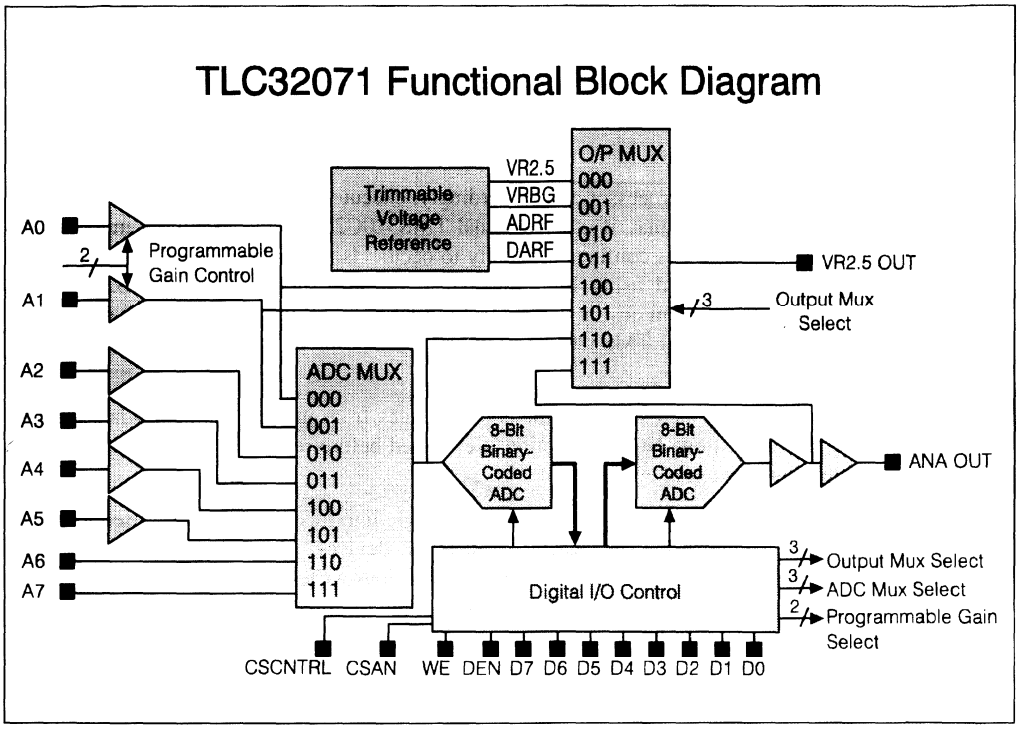


Figure 3.2.11 - TLC32071 Functional Block Diagram

The device includes an 8-bit voltage-output DAC, an 8-bit ADC, an analog input multiplexer with eight analog inputs, an output reference MUX and a high speed 8-bit bi-directional data bus that interfaces directly to the TMS320XX DSP family and to most other popular digital signal processors.

The reset pin (RESET) is used to clear the DAC and control registers. The 8-bit DAC converts digital signals to the equivalent analog values. The DAC is followed by a level shifter which adjusts the center of the DAC output range to the voltage externally applied to the ACOM pin. One of three output ranges can be selected by an internal register. The 8-bit ADC converts any one of eight analog inputs (A0 - A7) selected by programmable internal register through an input multiplexer. The input multiplexer selects the desired analog input channel according to the register contents.

Six of these inputs (A0 - A5) are buffered and have inverting inputs with built-in level shifting so that these six input ranges are centered at the ACOM pin voltage. Two of the six inputs (A0, A1) have

register selectable gains. The two remaining inputs (A6, A7) are direct inputs to the ADC multiplexer with output ranges centered at the internal 2.5 volt reference. After reset, this reference is available at the VR2.5OUT pin. This combination of features means that, in many applications, no additional signal conditioning is required.

The VR2.5OUT pin can also be programmed by an internal register to provide access to other internal references, any of the analog inputs after scaling and shifting, or the un-scaled output of the DAC, thus providing a useful self-test feature.

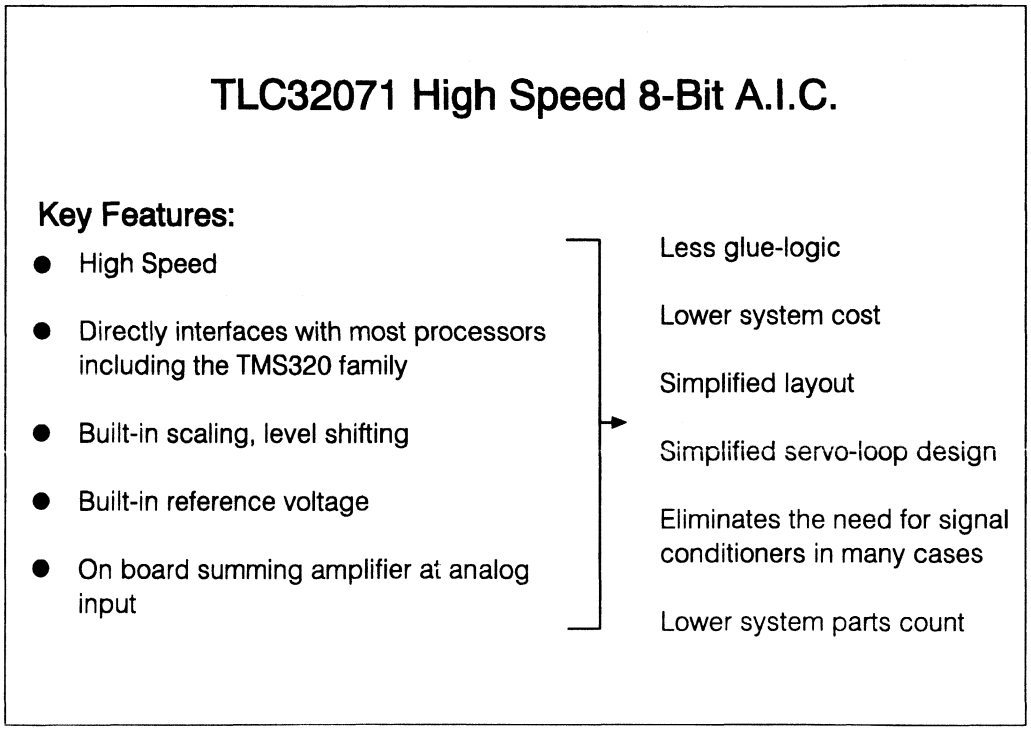


Figure 3.2.12 - TLC32071 Features and Benefits

General Purpose ADC Summary

PART NUMBER	RESOLUTION (BITS)	LINEARITY (LSBs)	CONVERSION SPEED	OUTPUT	FEATURES
TLC1540	10	0.5	21us	SERIAL	11 I/P MUX, EXT CLOCK, SINGLE 5V RAIL OPERATION
TLC1541	10	1.0	21us	SERIAL	11 I/P MUX, EXT CLOCK, SINGLE 5V RAIL OPERATION
TLC1542	10	0.5	21us	SERIAL	11 I/P MUX, INT CLOCK, SINGLE 5V RAIL OPERATION
TLC1543	10	1.0	21us	SERIAL	11 I/P MUX, INT CLOCK, SINGLE 5V RAIL OPERATION
TLC1549	10	1.0	21us	SERIAL	8-PIN PACK, INT CLOCK, SINGLE 5V RAIL OPERATION
TLC1550	10	0.5	6us	PARALLEL	INT/EXT CLOCK, SINGLE 5V RAIL OPERATION
TLC1551	10	1.0	6us	PARALLEL	INT/EXT CLOCK, SINGLE 5V RAIL OPERATION
TLC1125	12+SIGN	2	12us	PARALLEL	SINGLE 5V RAIL OR ±5V OPERATION, SELF CALIBRATING
TLC1225	12+SIGN	1	12us	PARALLEL	SINGLE 5V RAIL OR ±5V OPERATION, SELF CALIBRATING
TLC32071	8	1	2.5us (ADC)	PARALLEL	COMPLETE 8-BIT ANALOG I/O ON A CHIP

- ALL PARTS HAVE INTEGRAL SAMPLE/HOLD

Figure 3.2.13 - General Purpose ADC Summary

3. Analog Interface Circuits (AICs)

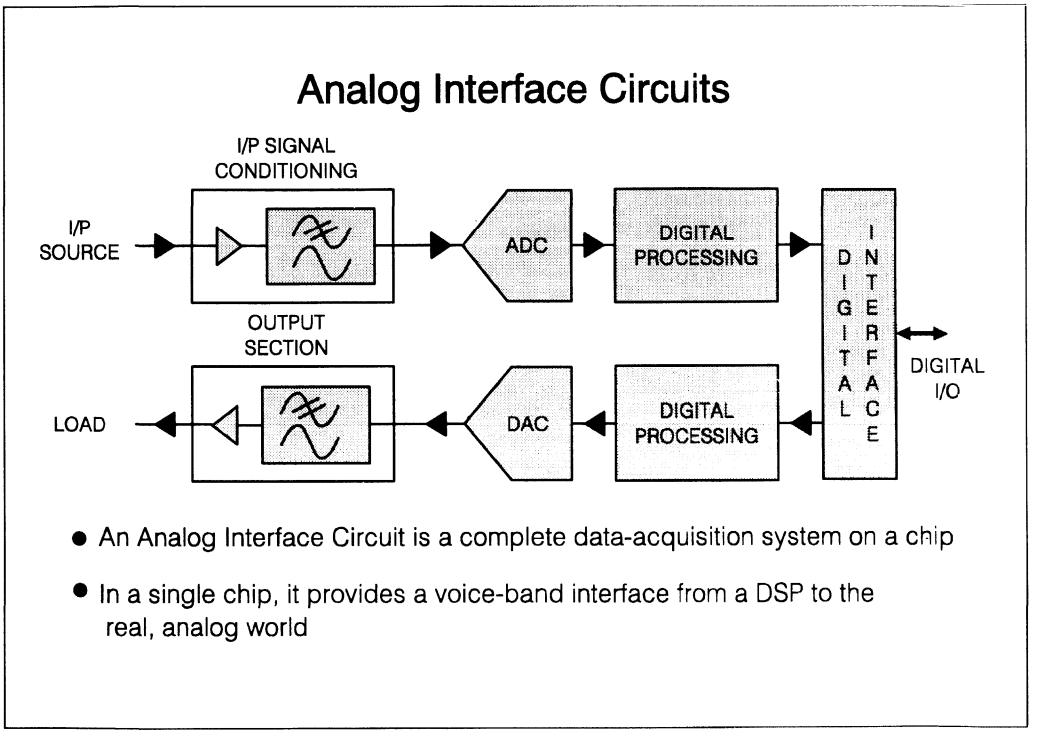


Figure 3.3.1 - Analog Interface Circuits

Texas Instruments' families of Analog Interface Circuits are complete data-acquisition systems on a chip.

They are highly integrated with ADC, DAC, pre- and post filter stages and input/output amplifiers on-chip. They have been developed mainly for high performance voiceband (currently up to 11.4KHz) system applications which require high resolution, a high degree of programmability with a simple DSP interface and an integrated design that conserves board space.

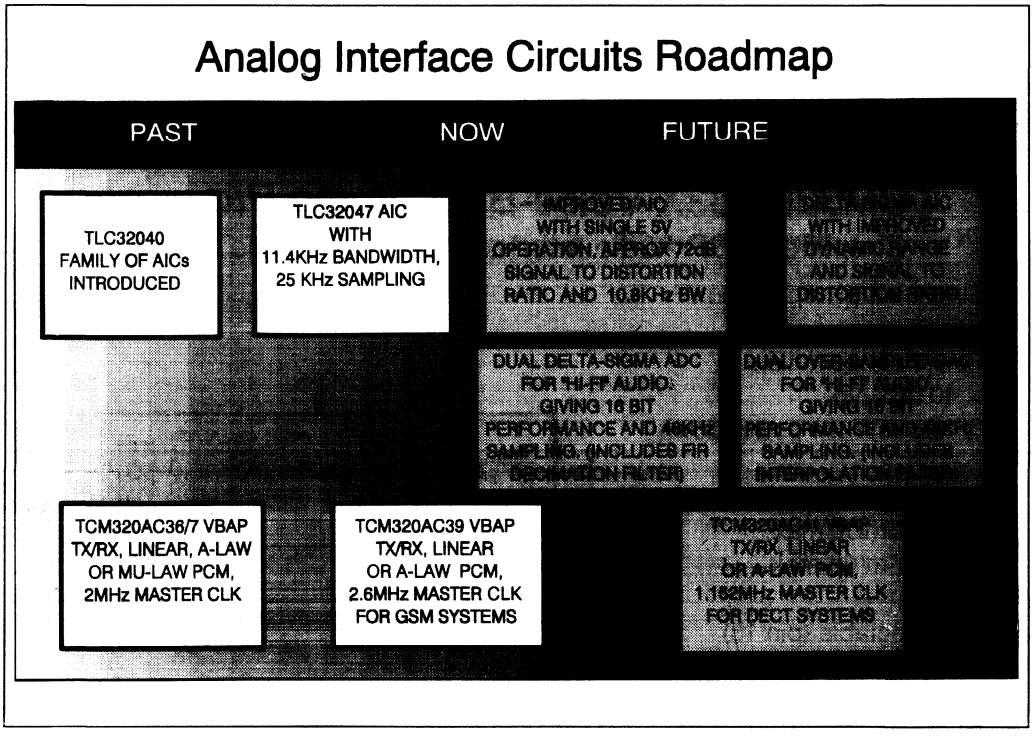


Figure 3.3.2 - Analog Interface Circuits Roadmap

The TCM320ACxx Voice-Band Audio Processor (VBAP) family is specifically designed to provide voice-band interface for mobile communications applications, while the TLC3204x family is more general purpose.

3.1. The Voice-band Audio Processor

TCM320AC3X Voice-Band Audio Processor

Simplified DSP Audio Interface From A Single Supply

- Single supply operation
- Power consumption
  40 mW typ
  1.25 mW typ power down
- Low noise (transmit direction)
  10 dBrnC0 max
  70 dBm 0p max
- Pin selectable (pin 15)
  linear or companded mode
- Direct interface to electret microphone and earpiece

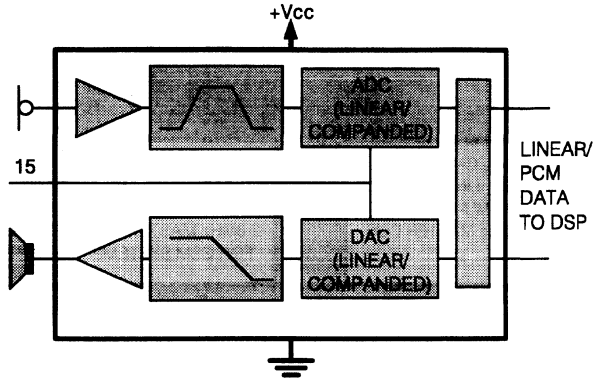


Figure 3.3.3 - The Voice-band Audio Processor

Many applications using voice-band signals require an Analog DSP interface that functions from a single supply and offers ADC, DAC, pre and post filter stages and on-chip amplifiers. Texas Instruments has developed the TCM320AC3X family of devices to provide the complete voice-band audio interface on a single chip. The devices are suitable for a wide range of voice-band data acquisition systems using a DSP that do not require the flexibility of the TLC3204X family including cellular and cordless telephones, answer machines and test equipment.

3.1.1. The Voice-band Audio Processor Building Blocks

The Voice-band Audio Interface is divided into a transmit and receive section which is controlled from a central timing unit. The input signals from the microphone are amplified via an input amplifier with provision for setting the amplifier gain to accommodate a range of signal input levels. The amplified signal is passed through an anti-aliasing and band pass filter then the clean analog signal is converted into digital code. The linear selection pin, when LOW, selects linear coding/decoding and, when HIGH, selects companded coding/decoding. Selection of the linear mode of operation reduces the

software required in the DSP. The filtered signal is then input to a compressing ADC if companded mode is selected otherwise the ADC performs a linear conversion. The digital data is buffered and clocked out via the output logic.

The receive signals are clocked into the device via input logic. The status of the linear selection pin determines if the incoming data is companded and requires decoding or if the data may be transferred directly to the DAC. The analog signal from the DAC is passed through switched capacitor filters, which provide out of band rejection, (sin x)/x correction functions and smoothing. Switched capacitor design techniques provide the user with precise audio band pass filtering and low power consumption. The filtered signal is presented to the differential output amplifier which may be connected directly to a piezo speaker.

Both the input and output amplifiers have a mute function accessible by a microcontroller. When the mute function is activated both amplifiers are disabled. In a telephone this function may be used to provide the user with a secrecy function.

The devices are designed using Texas Instruments LinEPIC^{TM} Technology. This technology offers the user single supply operation and low power consumption. The devices have a typical power consumption 40mW and only 1.25mW typical in power down mode.

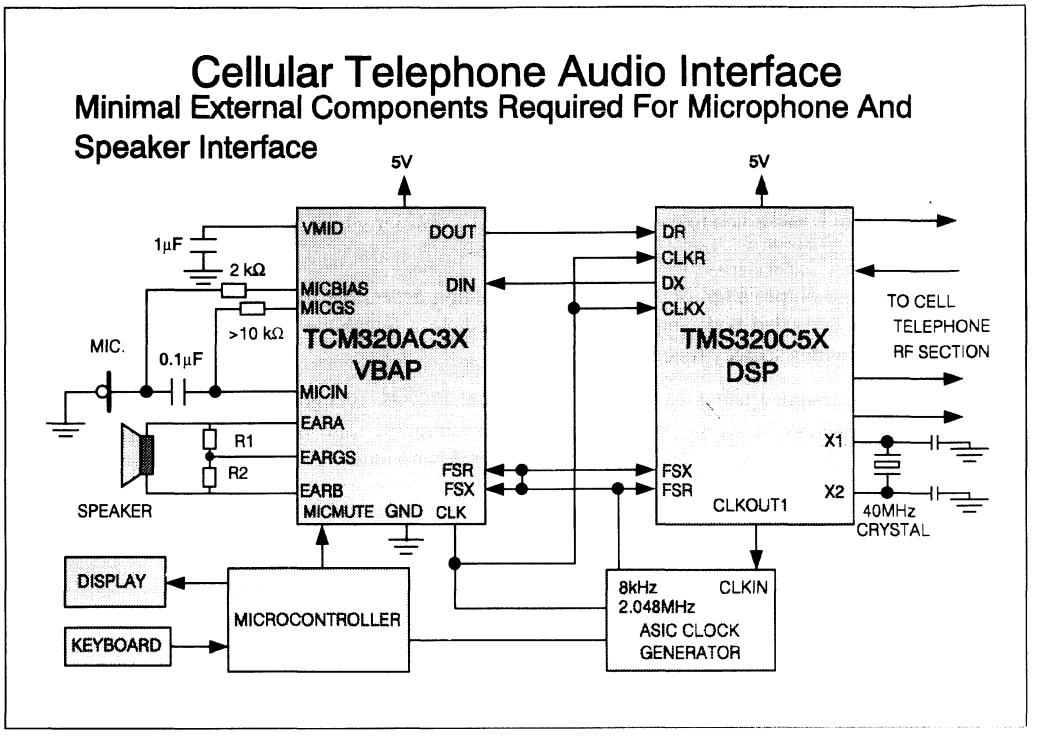


Figure 3.3.4 - Interfacing the VBAP to the load and DSP

The Voice-band Audio Processor is designed to provide a direct interface to the microphone, earpiece and DSP.

The Earpiece Interface.

This interface provides a balanced output from the differential output amplifier which drives a piezo speaker without the need for additional components.

The output amplifier has adjustable gain-setting via the external resistor network R1 and R2. It is recommended that R1 is greater than 10kΩ and R1+R2 is less than 100kΩ. This ensures that the time constant derived from the combination of the parallel resistor network and the capacitance at the earphone gain set input pin is minimised to avoid inaccuracies.

The output stage may be disabled by using the earphone mute control function. This prevents the audio signal being sent to the earphone and allows a secrecy function to be incorporated in the system.

The Microphone Interface.

A direct interface is provided to an electret type microphone. The reference voltage for the microphone amplifier and the bias voltage for the electret microphone are generated on-chip. Thus minimising the external circuitry around the device.

When the input amplifier is disabled the device transmits only zero codes.

In the linear mode of operation the microphone interface provides an adjustable volume control, this provides the user with a "soft touch" volume facility. The data word is 16 bits long, the first 13 bits contain the linear data, bits 13-15 allow the volume level to be adjusted in 8 steps between -18dBm0 and +3dBm0. In the companded mode of operation the data is transmitted and received in 8 bit words. The mode of operation is pin selectable, use of the linear mode simplifies software in the DSP.

The DSP Interface.

The Voice-band audio processor provides a standard serial interface to a TMS320 DSP or any other standard DSP. Transmit and receive directions can be operated independently.

The Voice-Band Audio Processor Family

Dedicated Silicon to Match End Equipment Needs!

Part Number	Master Clock Frequency (MHz)	Data Conversion	Channel Performance
TCM320AC36	2	Linear/μ-Law	AMPS/TACS
TCM320AC37	2	Linear/A-Law	PCN
TCM320AC39	2.6	Linear/A-Law	GSM

All devices available in 20 pin dual-in-line and small outline packages, ambient temperature range 0 to 70°C and -40 to +85°C

Figure 3.3.5 - The VBAP Family

Texas Instruments has released a family of devices tailored to specific mobile telephony systems. The distinguishing features between the devices are the frequency of the master clock, the out-of-band

rejection characteristics of the filters and the companded format of the digital data. The devices are tailored for use in cordless and cellular telephones in particular AMPS/TACS, CT-2 and GSM systems. Although targeted at these areas the devices are suitable for use in many voice-band data acquisition systems using a DSP e.g. digital encryption systems, digital voice-band data storage systems, test and measurement systems.

The devices are available in 20 pin dual-in-line or wide body small-outline packages. The devices are characterised from 0° C to 70° C or -40° C to 85° C.

3.2. TLC32040 Family of AICs

The TLC32040 family of AICs are more general purpose than the VBAP. They are used in applications such as FAX, modems, secure telephony, speech recognition and multi-media, in fact, in any DSP application which requires a voice-band interface to the real world.

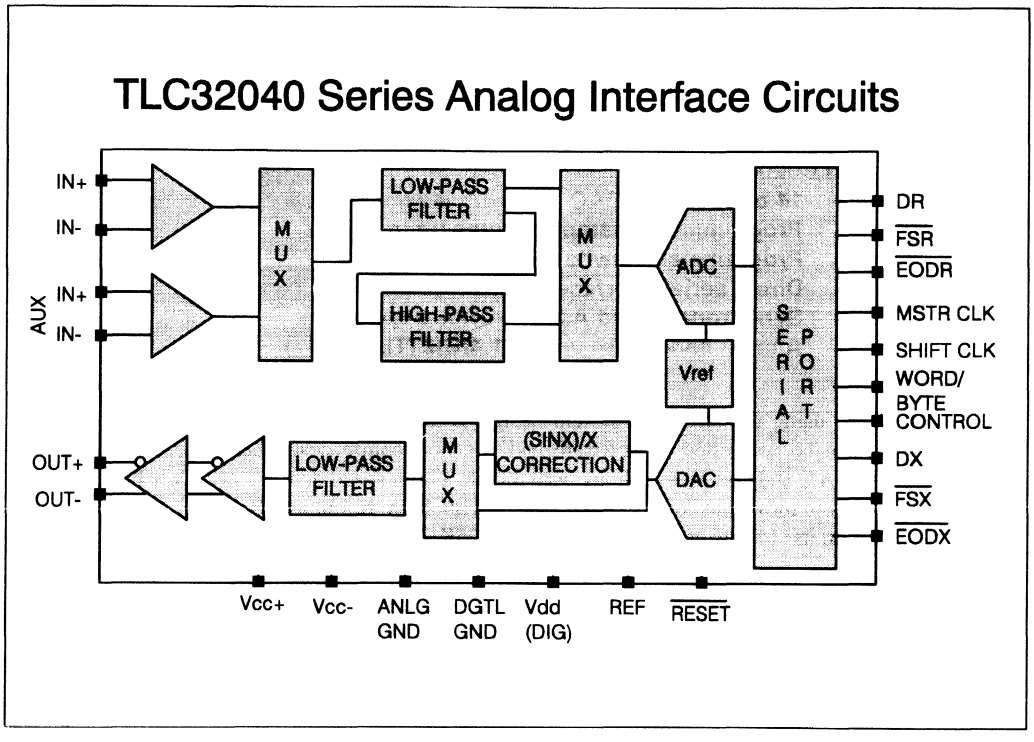


Figure 3.3.6 - TLC32040 Family Functional Block Diagram

3.2.1. AIC building blocks

The AIC is divided into a transmit and a receive section which are controlled from a central timing block. On the receive side, an analog signal is fed into either a main or auxiliary fully differential input which is selected by a multiplexer. The input stages have programmable gain so that the signal level can be optimised for maximum resolution. It is then passed to an anti-aliasing filter consisting of a LP followed by an optional HP which can be selected or bypassed as required. These are both switched capacitor filters (SCF) driven from a sub-multiple of the central master clock. This frequency is nominally set to 288kHz and all the data sheet specifications are derived from this value, but it can be easily altered to adjust the corner frequencies of the filters.

The ADC itself is also driven from a further sub-multiple of the same clock which ensures the sampling is synchronised with the SCF filter. The sampling rate is programmable up to 25KHz , and encompasses the standard modem sampling rates (7.2KHz, 8.0KHz, 9.6kHz , 14.4kHz, 19.2KHz). The output from the ADC is a 14 bit word which is then passed out of a serial port to a DSP.

In the transmit section, data and control information is transferred from the DSP into the DX pin of the serial port. This is transmitted to a 14 bit DAC which is controlled in the same way as the ADC. The sampling rate for both can be tied together in Synchronous operation but they can be run independently in Asynchronous mode. The output from the DAC is fed to a LP SCF and then to a sinx/x correction filter (which can be bypassed if required). It is finally transmitted out of a differential output buffer.

TLC3204X AIC

- **14 bit ADC and DAC**
- **Programmable sampling rates up to 25KHz**
- **Programmable switched capacitor filters**
- **Direct serial interface to DSP**
- **Synchronous and Asynchronous operation**
- **Analog bandwidth up to 11.4KHz (TLC32047)**

The advantage of using the AIC in a system design is the degree of flexibility that results from parameters that can be controlled by software and do not require costly hardware modifications. Applications like FAX and secure telephony both dictate a high speed data rate with low bit error rate figures (BER). This in turn demands a flexible system with high resolution. Both these parameters are met by the AIC with its 14-bits of resolution and up to 25K samples per second data rate.

3.2.2. Interfacing the AIC to the TMS320 DSP

The interface of the AIC is built on a serial data format concept aimed at interfacing the device directly to the serial I/O of the TMS320C25 digital signal processor. As such, the core of the system consists of these two chips alone, rather than being supplemented by a number of interface devices commonly found in many applications.

The communication between the AIC and the DSP is based on just six lines. These are outlined in the following list:

MASTER CLK : The AIC is built on a single master clock input which is divided by the contents of control registers to determine the conversion rates and filter characteristics.

FSX : Initiates the AIC to prepare for a data transfer from the host processor.

DX : When the FSX has initiated the AIC,a transfer of data will take place to the AIC from the host along this line.

FSR : Initiates the serial input of the host to receive output data from the AIC.

DR : When the FSR serial input has been activated, the AIC will transfer data from the A/D to the host along this line.

SHIFT CLOCK : Dictates the speed of data transfer between the AIC and the host. This clock shifts the data into and out of the AIC.

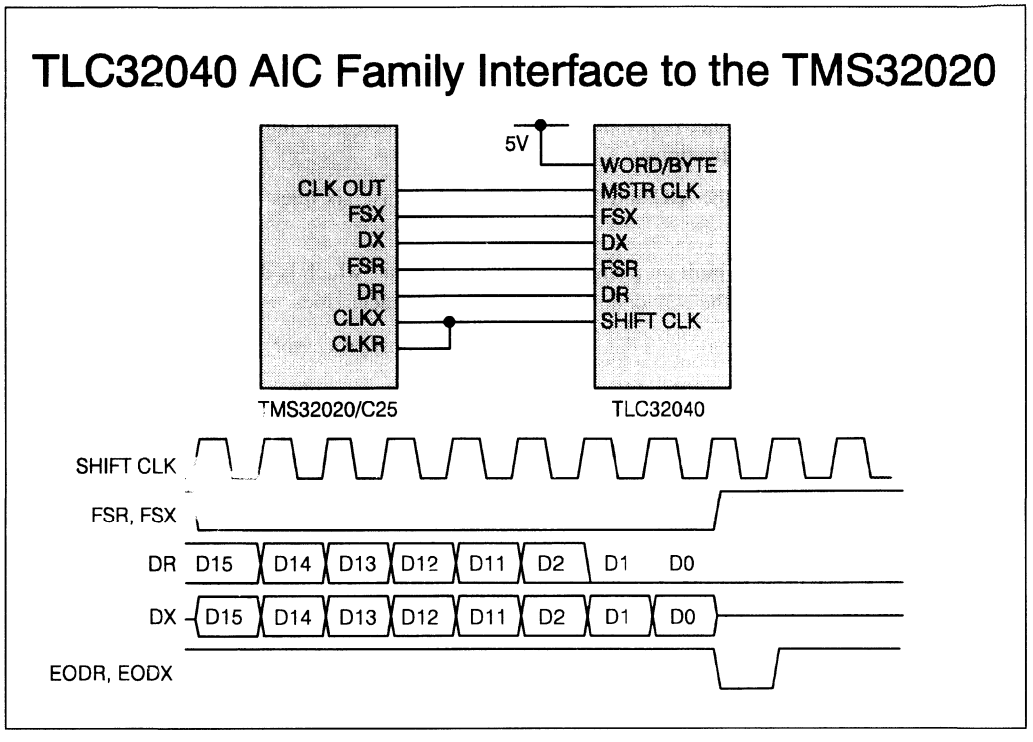


Figure 3.3.7 - TLC32040 Family Interface to the TMS320 DSP

3.2.3. TLC32040 Interface to the TMS32020

Hardware

Because the TLC32040 is designed specifically to interface with the serial port of the TMS32020/C25, the interface requires no external hardware. Except for CLKR and CLKX, there is a one-to-one correspondence between the serial port control and data pins of TMS32020 and TLC32040. CLKR and CLKX are ties together since both the transmit and the receive operations are synchronized with SHIFT CLK of the FLC32040. The interface circuit, along with the communication program (page 10-33), allows the AIC to communicate with the TMS32020/C25 in both synchronous and asynchronous modes.

Software

The program listed in Appendix B of "Linear Circuits data Book, Volume 2, 1992" allows the AIC to communicate with the TMS32020 in synchronous or asynchronous mode. Although originally written for the TMS32020, it will work just as well for the TMS320C25.

Initializing the TMS32020/C25

This program starts by calling the initialization routine. The working storage registers for the communication program and the transmit and receive registers of the DSP are cleared, and the status

registers and interrupt mask register of the TMS32020/C25 are set (see program flow charts in Appendix B). The addresses of the transmit and receive interrupt subroutines are placed in their storage locations, and the addresses of the routines which ignore the first transmit and receive interrupts are placed in the transmit and receive subroutine pointers (XVECT and RVECT). The TMS32020/C25 serial port is configured to allow transmission of 16-bit data words (FO), the serial port format bit of the TMS32020/C25 must be set to zero) with an externally generated frame synchronization (FSX and FXR are inputs, TXM bit is set to 0).

Communicating with the TLC32040

After the TMS32020/C25 has been initialized, interrupts are enabled and the program calls subroutine IGR. The processor is instructed to wait for the first transmit and receive interrupts (XINT and RINT) and ignore them. After the TMS32020 has received both a receive and transmit interrupt, the IGR routine will transfer control back to the main program and IGR will not be called again.

If the transmit interrupt is enabled, the processor branches to location 28 in program memory at the end of a serial transmission. This is the location of the transmit interrupt service routine. The program context is saved by storing the status registers and the contents of the accumulator. The interrupt service routine calls the interrupt subroutine whose address is stored in the transmit interrupt pointer (XVECT).

A similar procedure occurs on completion of a serial receive. If the receive interrupt is enabled, the processor branches to location 26 in program memory. As with the transmit interrupt service routine (XINT, page 10-36, line 226), the receive interrupt service routine (page 10-36, line 194) saves context and then calls the interrupt subroutine whose address is stored in the receive interrupt pointer (VECT). It is important that during the execution of either the receive or transmit interrupt service routines, all interrupts are disabled and must be re-enabled when the interrupt service routine ends.

The main program is the application program. Procedures such as digital filtering, tone-generation and detection, and secondary communication judgment can be placed in the application program. In the program listing shown in Appendix B, a subroutine (C2ND) is provided which will prepare for secondary communication. If secondary communication is required, the user must first write the secondary code to the DXMT register. This data word should have the two least significant bits set high (e.g. >0003). The first 14 bits transmitted will go to the D/A converter and the last two bits indicate to the AIC that secondary communication will follow. After writing to the SXMT register, the secondary communication word should be written to the D2ND register.

This data may be used to program the AIC internal counters or to re-configure the AIC (e.g., to change from synchronous to asynchronous mode or to bypass the bandpass filter). After both data words are stored in their respective registers, the application program can then call the subroutine C2ND which will prepare the TMS32020 to transmit the secondary communication word immediately after primary communication.

Secondary Communicating - Special Considerations

This communication program disables the receive interrupt (RINT) when secondary communication is requested. Because of the critical timing between the primary and secondary communication words and because RINT carries a higher priority than the transmit interrupt, the receive interrupt cannot be allowed to interrupt the processor before the secondary data word can be written to the data-transmit register. If this situation were to occur, the AIC would not receive the correct secondary control word and the AIC could be shut down.

In many applications, the AIC internal registers need only be set at the beginning of operation (i.e., just after initialization). Therefore, the DSP only communicates with the AIC using primary Communication. In cases such as these, the communication program can be greatly simplified.

Analog Interface Circuits Selection Guide

PART NO	RESOLUTION	FEATURES	FILTER B/W	MAX. SAMPLE RATE (KBPS)	VOLTAGE REFERNCE	DIRECT I/F TO DSP	ON-CHIP (SIN X) /X CORRECTION	EXAMPLE APPLICATIONS
TLC32044CN	14 BIT	VOICE-BAND AIC	150-3800 Hz	19.2	INTERNAL	YES	SELECTABLE	SPEECH, MODEMS, DATA ANALYSIS
TLC32045CN	14 BIT	LOW COST VERSION OF TLC32044	150-3800 Hz	19.2	INTERNAL	YES	SELECTABLE	SPEECH, MODEMS, DATA ANALYSIS
TLC32046CN	14 BIT	EXTENDED BANDWIDTH AIC	300-7600 Hz	25	INTERNAL	YES	SELECTABLE	SPEECH, MODEMS, DATA ANALYSIS
TLC32047CN	14 BIT	EXTENDED BANDWIDTH AIC	300-11400 Hz	25	INTERNAL	YES	SELECTABLE	SPEECH, MODEMS, DATA ANALYSIS

Figure 3.3.8 - AIC Selection Guide

4. Video Interface Palettes

4.1. Introduction

Today's computer systems make extensive use of graphics, both in the user interface such as Windows ™ and in the applications S/W such as desktop publications, CAD, etc. In order to service these requirements, high resolution monitors are required together with the circuits that drive them.

Video Interface Palettes

A Video Interface Palette is:-

A complete graphics back-end on a chip

It interfaces the Video Controller / VRAM of a PC or workstation with the graphics display monitor.
It contains a combination of fast logic functions and video DAC's to transform the stored information into an analog waveform for input to the monitor.

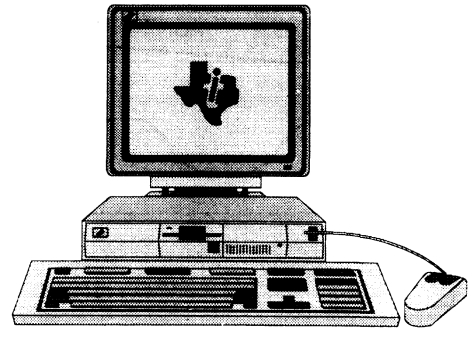


Figure 3.4.1 - Video Interface Palettes - Introduction

4.2. Image Composition

An image is made up from individual picture elements (pixels). Images are formed on a CRT screen when the electron beam sweeps horizontally across the screen and vertically down, illuminating the pixels one at a time, until it has swept through the entire array. Return of the beam from right to left occurs during the horizontal retrace time and from bottom to top during the vertical retrace time. During the retrace time the screen is blanked by horizontal and vertical blanking pulses. This horizontal and vertical sweeping of the beam is called raster scanning. It is the most widely used display method and facilitates the use of bit-mapped graphics.

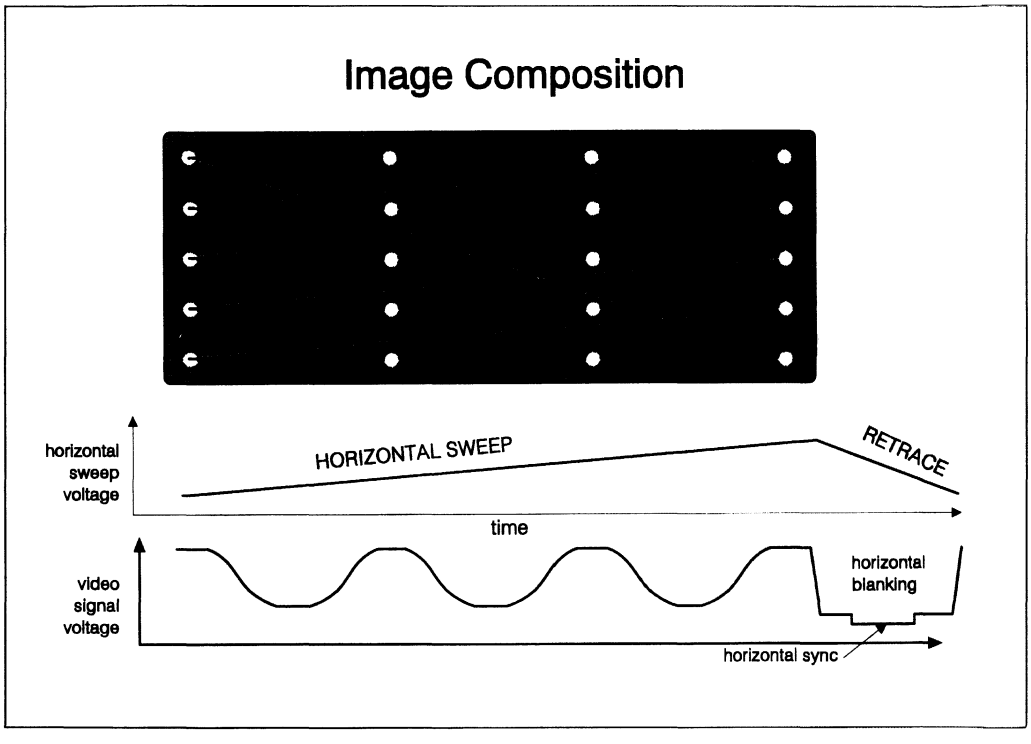


Figure 3.4.2 - Image Composition

The Hsync and Vsync pulses, which occur during the appropriate blanking period, assure the proper beam start position for each scan. During the beam scanning, the individual pixel data is sequentially timed with the beam position by the pixel clock so that the image appears in the proper position on the screen.

Each pixel is made up from red, green and blue intensity information, and a color monitor, typically , has inputs for each of these. The inputs drive 3 separate electron guns which illuminate the appropriate color phosphor at the appropriate time, determined by the sync signals. By varying the intensity of each of these primary colors, any secondary color can be obtained. (Equal red, green and blue intensities would produce white to gray, depending on the overall intensity of the signals applied).

4.3. Graphics Display System

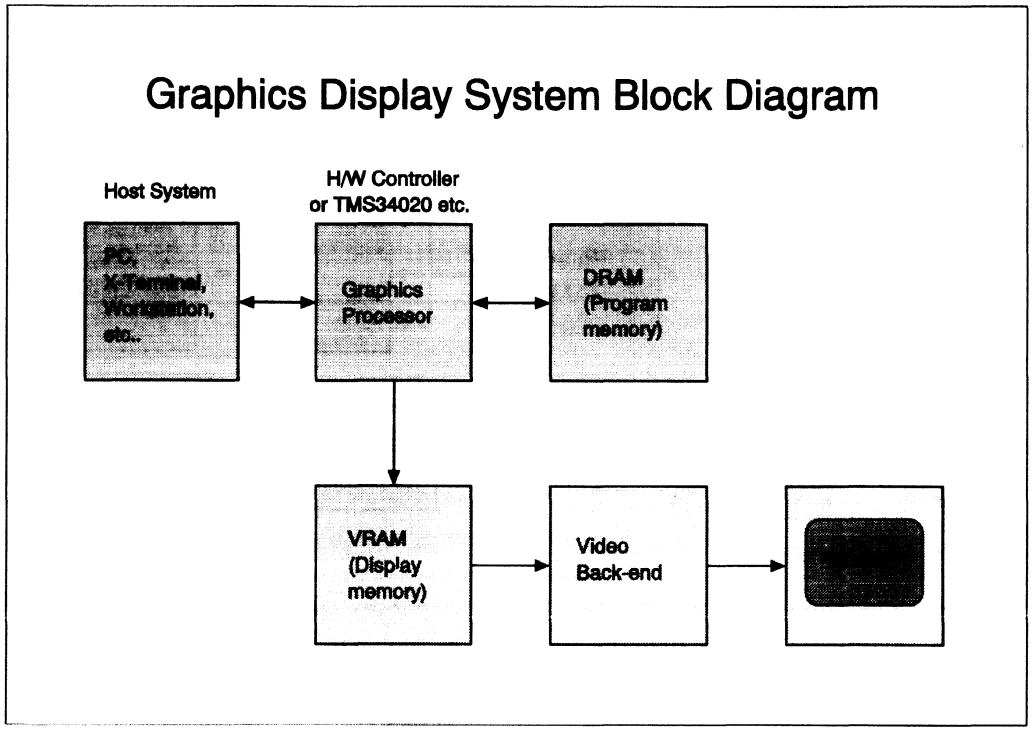


Figure 3.4.3 - Graphics Display System Block Diagram

The generation and manipulation of bit-mapped images in memory is the primary function of a Graphics Display System. A graphics processor carries out the routine display tasks by handling the data updates, bit manipulation and synchronising functions for the screen display. This relieves the host system processor of these functions, making the total system much faster. A typical graphics display system consists of:

- **Graphics processor**
- **Program memory**
- **Display memory**
- **Video back-end**
- **Display monitor**

There are two ways to handle the graphics processor: Either by using a dedicated hardware processor or, alternatively, a high speed S/W based graphics processor, such as the TMS34020.

The graphics back-end is the circuitry between the frame store (display memory) and the display monitor. It reads the stored image data from the display memory (VRAM or DRAM) and converts it into a high speed analog signal to drive the monitor. It also provides many of the timing signals required to perform this task.

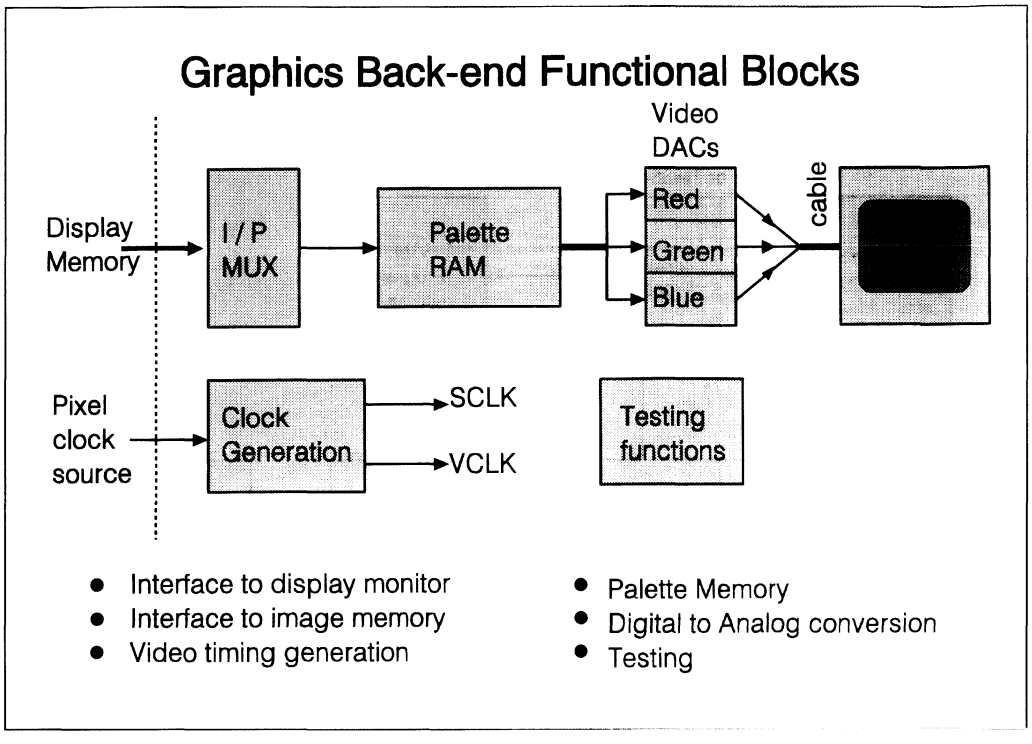


Figure 3.4.4 - Graphics Back-End Functional Blocks

- **Interface to the display monitor**
- **Interface to the display memory**
- **Video timing generation**
- **Palette memory**
- **Digital-to-analog conversion**
- **Testing circuitry**

4.4. The TLC34076 Video Interface Palette (VIP)

4.4.1. Resolution and Refresh Rate

Over the years IBM VGA (Video Graphics Array), which has a resolution of 640 x 480, has dominated the overall graphics board design. However, as the technology advances, and with the introduction of IBM XGA, resolutions of 1024 x 768 and higher (such as 1280x1024 and 1600x1280) become the general design target.

There is also a requirement for high refresh rates, to eliminate the annoying flicker effect. The current European Community standard is 72Hz non-interlaced and in the U.S. the standard is 60Hz non-interlaced, but more designers are now considering 76Hz, 85Hz and even higher.

This combination of high resolution and high refresh rate demands a very fast pixel clock (dot clock).

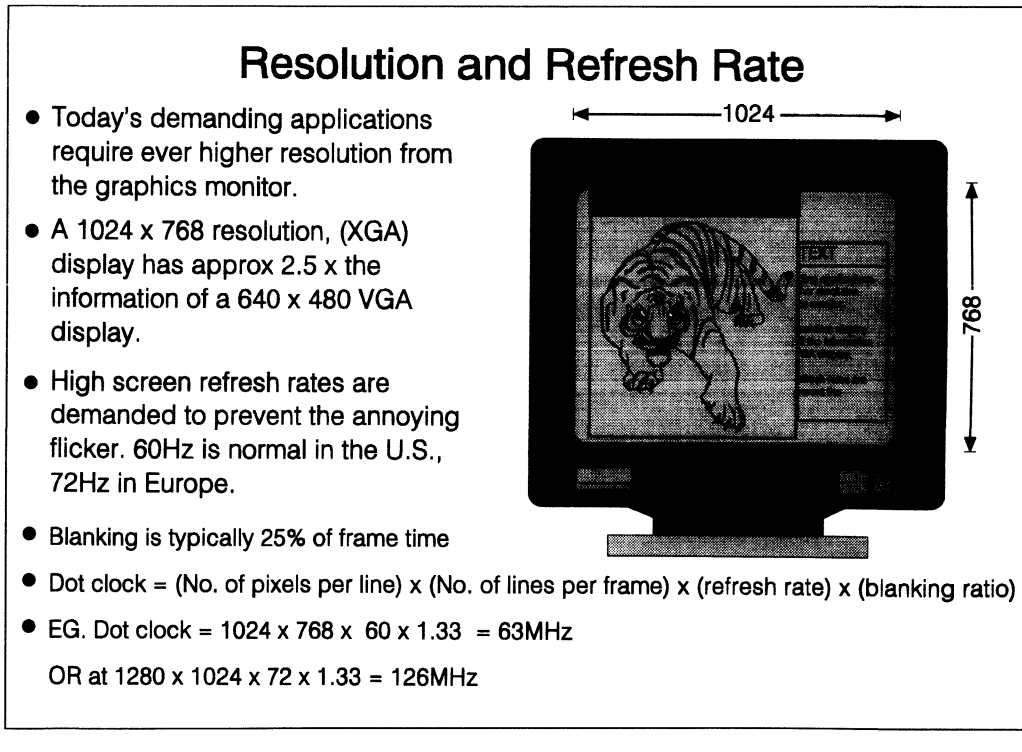


Figure 3.4.5 - Resolution and Refresh Rate

4.4.2. Calculation of Required Pixel Clock Frequency

The required pixel clock frequency is determined by the resolution and refresh rate of the system. It is given by:

$$f_{pixel} = (N^{o} \text{ of pixels per line }) \times (\text{No of lines per frame}) \times (\text{refresh rate}) \times 1.33$$

The last term allows for blanking during horizontal and vertical retrace.

eg. for a 1280 x 1024 resolution display at 72 Hz refresh rate, the pixel rate would be:

$$f_{pixel} = 1280 \times 1024 \times 72 \times 1.33 = 125\text{MHz (approx.)}$$

The TLC34076 is available in 66MHz, 85MHz, 110MHz, 135MHz and 170 MHz speed versions and the TLC34076-135 satisfies the above requirement with a reasonable safety margin.

4.4.3. Color Depth, Resolution and Frame Store Size Relationship

High resolution displays such a VGA and beyond use 8 bits per color for intensity data. This means that over 16 million ($2^8 \times 2^8 \times 2^8$) colors are available. However many graphics applications only require 256 or less colors and the amount of memory in the frame buffer required to support 16 million colors at high resolution would be prohibitively expensive for these applications. So Video Interface palettes like TI's TLC34076 have an I/P multiplexer, which allows different numbers of bits-per-pixel to be chosen under S/W control, and programmable counters to accommodate different screen resolutions.

Resolution and Frame Store Size

MIN. NUMBER OF PIXELS PER TRANSFER *	FRAME RATE	APPROX DOT CLOCK	SCREEN RESOLUTION	MINIMUM FRAME STORE SIZE FOR NUMBER OF COLORS (MBITS)						
1	60Hz	38MHz	800 × 600	2	3	4	8	8	12	16
	72Hz	46MHz								
2	60Hz	63MHz	1024 × 768	2	4	8	16	16	20	28
	72Hz	76MHz								
4	60Hz	105MHz	1280 × 1024	3	6	12	24 **	24 **	***	***
	72Hz	126MHz								
4	60Hz	164MHz	1600 × 1280	4	8	16	32 **	32 **	***	***
	72Hz	197MHz								

* AT APPROX 45MHz VRAM SERIAL PORT SPEED
** NEEDS PALETTE WITH 64-BIT PIXEL PORT OR EXTERNAL MUX
*** NEEDS PALETTE WITH MORE THAN 64-BIT PIXEL PORT AT PRESENT VRAM SPEED OR EXTERNAL MUX

Figure 3.4.6 - Resolution and Frame Store Size

In the 1, 2, 4 or 8 bits-per-pixel modes the pixel data, from the Frame Buffer goes, not to the DACs, but addresses a 256 location x 24 bit palette RAM within the TLC34076. This allows up to 256 colors to be resident at any one time with the 24 bits being composed of 8 bits each of red, green and blue data. The 256 colors chosen are downloaded by the host depending on the application. (A palette page-register provides additional bits of palette address when 1, 2 or 4 bit transfers are used, allowing screen colors to be changed with only one MPU write cycle).

The TLC34076 also supports 16-bit and 24-bit true color modes, where the data from the Frame Buffer goes directly to the video DACs. This is usually used to present "real" images to the screen, the 24-bit mode providing "photo-realistic" images.

Because the VRAM read port speed is limited to approximately 45MHz, then for dot clock speeds above 45MHz, more than 1 set of pixel data has to be transferred in each read. The TLC34076 has a 32-bit wide pixel bus and supports 1, 2, 4, 8, 16 or 32 pixels per transfer, giving 24, 16, 8, 4, 2 or 1 bits per pixel. (In the 24 bits-per-pixel mode, the remaining 8 bits provide an overlay function).

As more colors are demanded at higher and higher resolution then wider pixel busses are required to effect the transfer to effectively increase the bandwidth of the pixel bus.

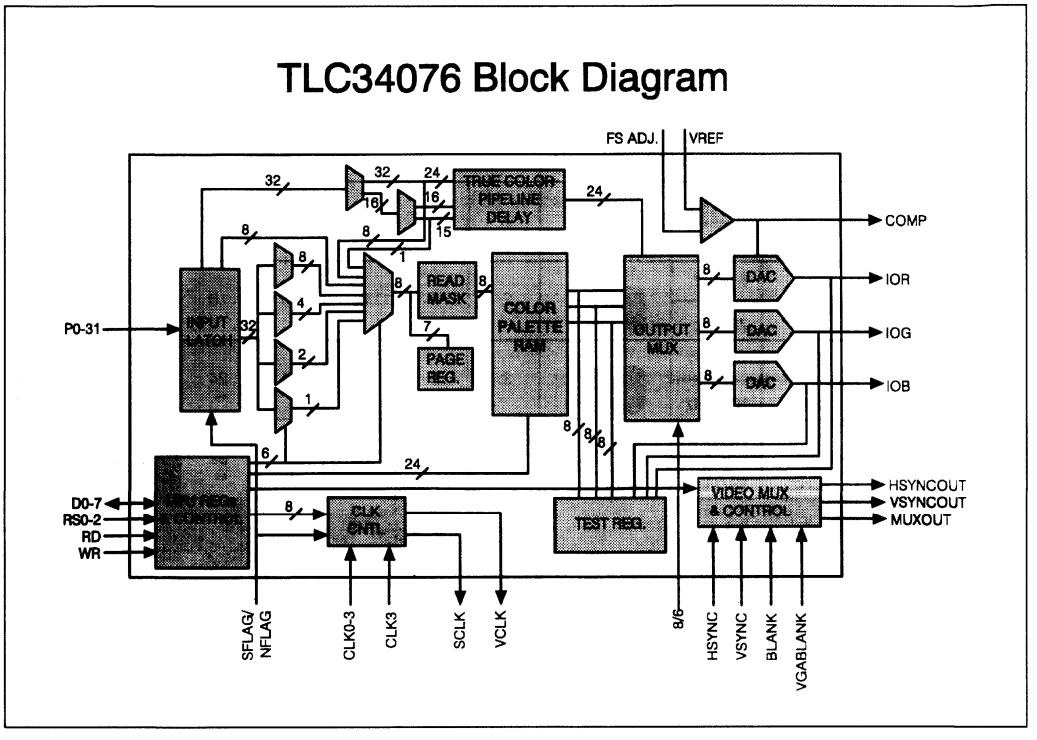


Figure 3.4.7 - TLC34076 Functional Block Diagram

Pixel clock is the fundamental clock source to shift data out to the monitor through the DACs. All other data path and video control logic have to be synchronous to the pixel clock but at lower frequencies. **VCLK** is typically used for sync and blank signal generation and is simply pixel clock divided by 1, 2, 4, 8, 16 or 32 plus disable. **SCLK** is the VRAM shift clock which allows the VIP to be interfaced to the VRAM without any external glue logic. It is gated off during blanking and will support "split shift register transfer cycles" . This allows more efficient use of the VRAM.

The TLC34076 features a separate VGA bus that allows data from the feature connector on a PC to be taken directly to the palette without the need for any external multiplexing. This allows a replacement graphics board to remain downwards compatible by using the existing graphics circuitry which is often located on the mother-board.

Another feature of the TLC34076 is that it supports both Little-Endian (Intel™ microprocessor based format) and Big-Endian (Motorola™ microprocessor based format) operation of the pixel bus. The difference is that the data fields, representing the individual pixels, in the Big-Endian format are in the reverse order to those in the Little-Endian format.

4.5. The TLC34077 Video Interface Palette

Some controllers, like the 68800 from ATI, interface directly with both the read and write ports of the VRAM and have a separate VIP interface port. For these controllers it would be an un-necessary expense to provide all the VRAM control functions and pixel data paths that the controller does not need. So TI has introduced the TLC34077 VIP (which is a cost optimised derivative of the popular TLC34076) especially to work with this type of controller.

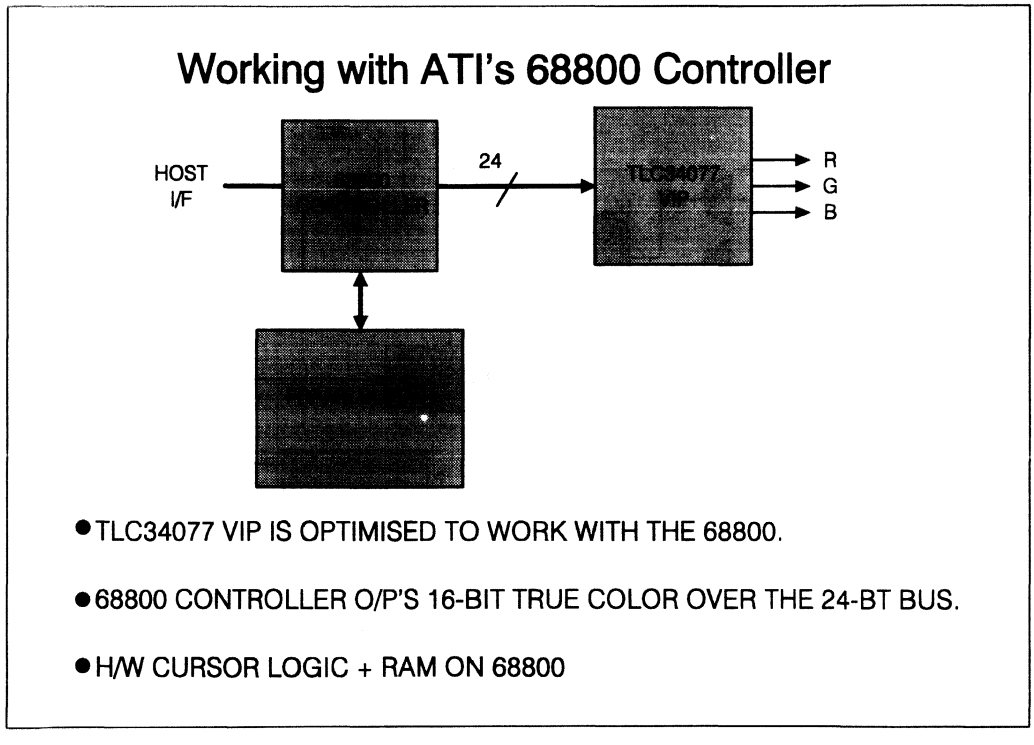


Figure 3.4.8 - Working with ATI's 68800 Controller

4.6. The TLC34074 Monochrome Video Interface Device

The TLC34074 is a version of the TLC34076 optimized for monochrome or grey-scale display systems. It is the first monochrome Video Interface Device to offer up to 200MHz dot clock, together with the pixel timing, multiplexing and control options previously only available on color Video Interface Palettes. It is pin compatible with the TLC34076 thus allowing easy system upgrade to color.

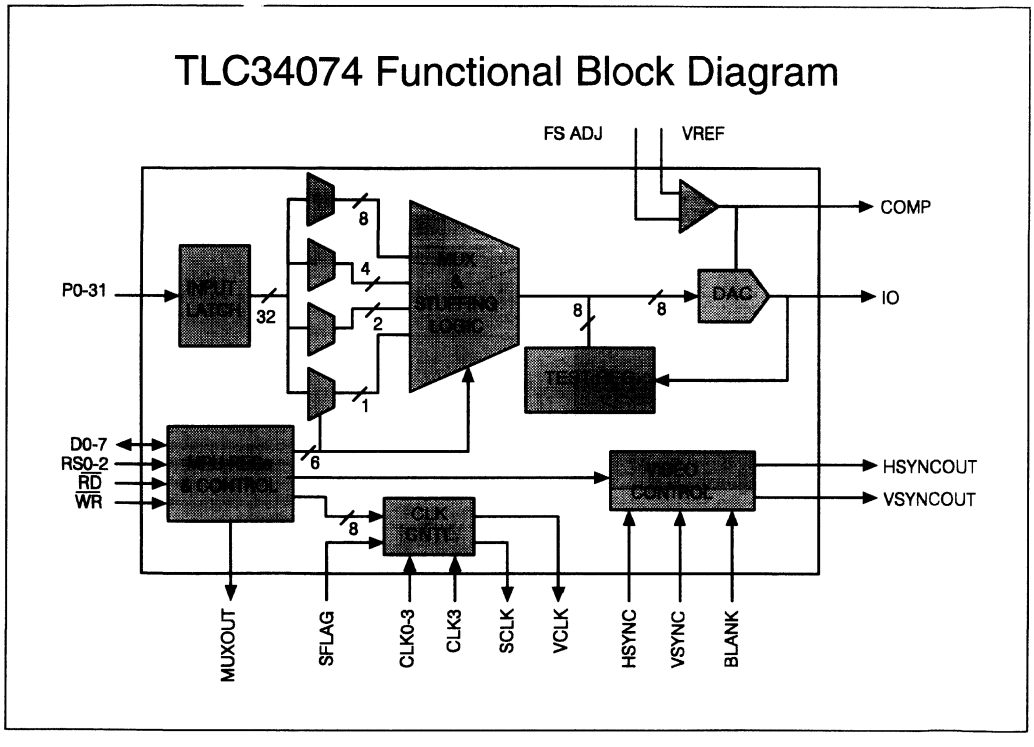


Figure 3.4.9 - TLC34074 Functional Block Diagram

Major features of the TLC34074 include:-

- **Pin compatible with the TLC34075 and TLC34076 VIPs allowing easy system upgrades to color**
- **Up to 200 MHz operation enables 1600 X 1280 resolution at 72 Hz refresh**
- **No palette RAM or VGA interface and only a single DAC for streamlined grey-scale or monochrome performance**
- **Versatile multiplexing interface allows lower pixel bus rates, programmable bit-plane widths, and multiple resolutions**
- **Works with virtually any video controller architecture**
- **On-chip SCLK generation allows direct interface to VRAM, and supports split-shift register transfers**
- **Supports Big and Little Endian data formats on the pixel input bus, allowing Big Endian designs (AMD29K™, Motorola 68000™, Apple MacIntosh™) to get the benefit of the versatile multiplexing interface as well as Little Endian (Intel™ format) designs**

4.6.1. X-Terminals

X-windows terminals are a derivative of network computing, since they execute applications that are typically not "local", but reside on a "remote" host computer system. X-terminals feature a graphical windowing system which is ported to a specially designed terminal optimized for graphics performance. These terminals then execute X-server software over a network, enabling them to run workstation like applications in a distributed computing environment. A generic X-windows terminal typically includes a microprocessor/graphics processor system, a main-memory system, video memory, a network controller, a peripheral controller (mouse, keyboard, etc.) and video D/A converters.

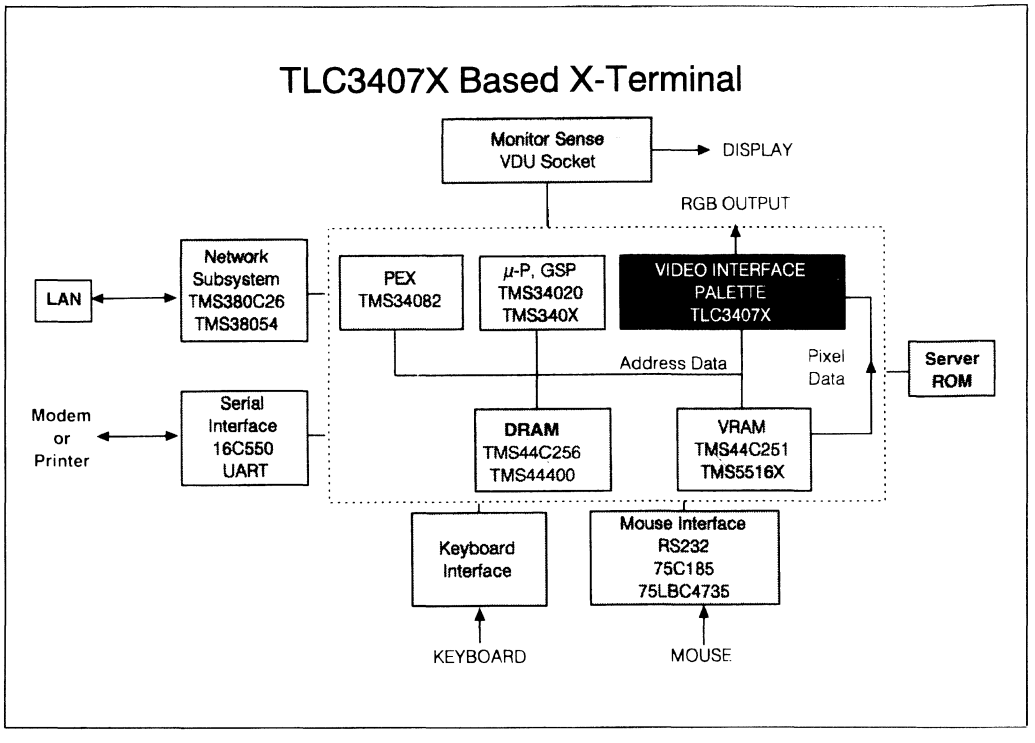


Figure 3.4.10 - TLC3407X based X-Terminal

The above figure demonstrates a generic X-terminal system. Texas Instruments offers state-of-the-art solutions for all major components of the X-windows terminal.

The TLC3407X family of pin-compatible Video Interface Palettes allows the X-terminal system designer to make cost/performance tradeoffs while maintaining a common architecture. By selecting the TLC34076, a high performance design can be created that supports monochrome through 16- and 24-bit true color. On the other hand by using the same hardware architecture, a cost effective, high performance monochrome or grey-scale X-terminal can be created utilizing the TLC34074.

4.7. TLC34076 Analog System

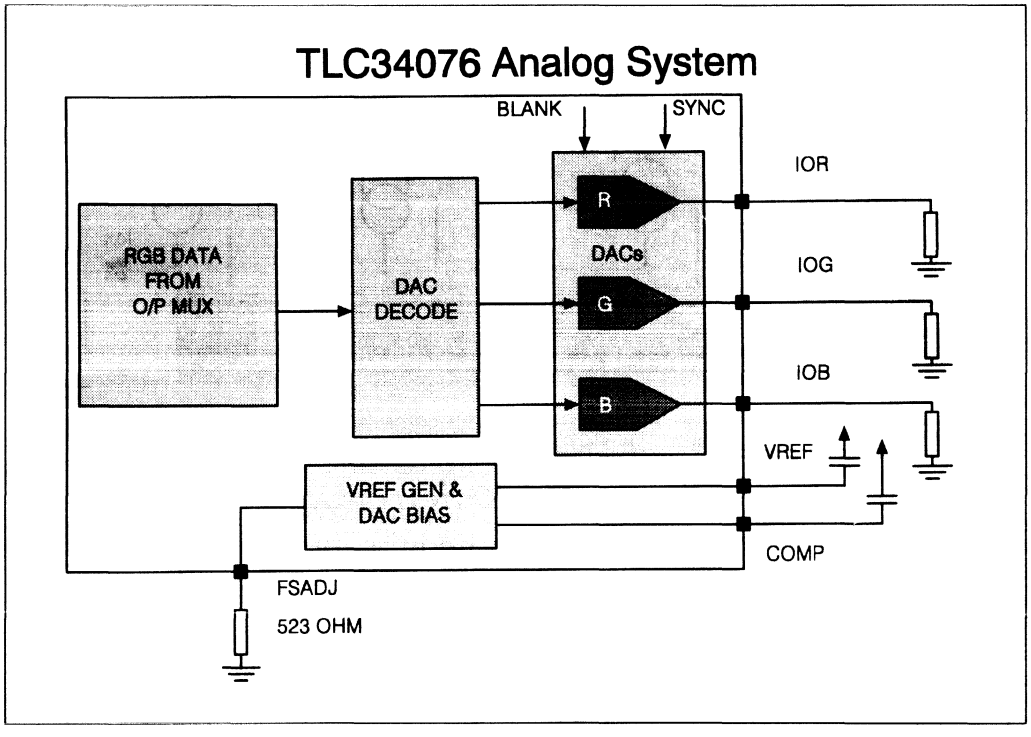


Figure 3.4.11 - TLC34076 Analog System

Color and brightness information are sent to the monitor as a continuously variable voltage. Therefore the digital information stored in the frame buffer or palette RAM must be converted to voltage levels that can be used by the monitor. This is the function of the output DACs and since color is represented by a mix of the three primary colors, red, green and blue, there is a DAC for each of these.

Most RGB monitors have a 75 ohm input impedance and the analog output circuits must be able to drive this from a 75ohm source impedance (for a properly balanced line). The TLC34076 integrates this video output stage, being capable of driving video signals into a doubly terminated 75ohm line conforming to the RS-343A specification. Sync generation is incorporated into the green output for monitors which require sync-on-green.

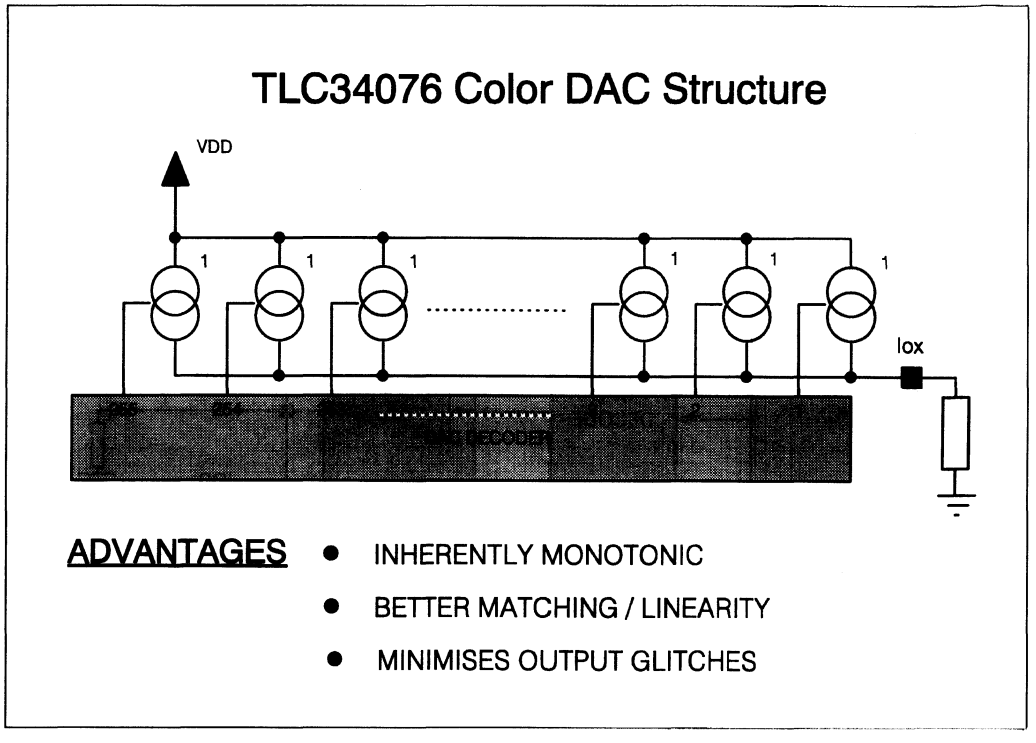


Figure 3.4.12 - TLC34076 Color DAC Structure

At a palette speed of 135MHz there is only 7.4 ns available to settle to the new analog output value, so careful attention has to be paid to the design of the DACs. Instead of the normal, 8 binary weighted current sources, the TLC34076 has 255 equally weighted current sources. This system is inherently monotonic, has better linearity and matching and reduces output glitches, particularly around half scale.

4.8. Video Interface Palettes Roadmap

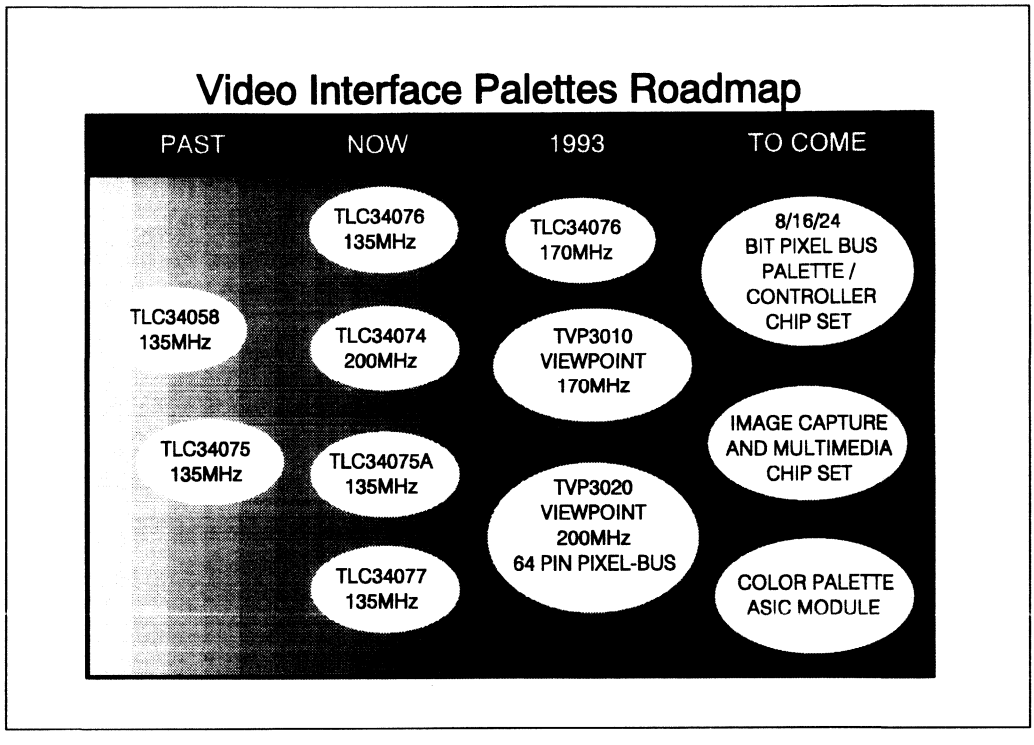


Figure 3.4.13 - Video Interface Palettes Roadmap

Data Conversion Appendix 1

Contents

1. Designing with Data Converters

This appendix discusses the way the specifications for a data converter are defined on a manufacturers data sheet and considers some of the aspects of designing with data conversion products. It covers the sources of error that change the characteristics of the device from an ideal function to reality.

1.1. The Ideal transfer function

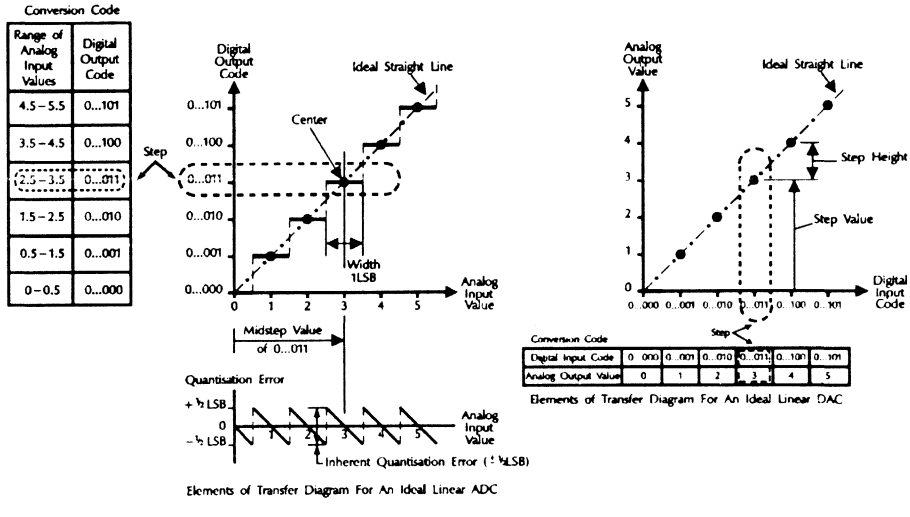


Figure 3.A1 - The Ideal transfer function

1.1.1. Analog to Digital Converter (ADC)

An ideal ADC uniquely represents all analog inputs within a certain range by a limited number of digital output codes. The diagram shows that each digital code represents a fraction of the total analog input range. Since the analog scale is continuous, whilst the digital codes are discrete, there is a quantisation process that introduces an error. As the number of discrete codes increases, the corresponding step width gets smaller and the transfer function approaches an ideal straight line. The

steps are designed to have transitions such that the midpoint of each step corresponds to the point on this ideal line.

The width of one step is defined as 1 LSB (one Least Significant Bit) and this is often used as the reference unit for other quantities in the specification. It is also a measure of the resolution of the converter since it defines how many portions the full analog range is divided into. Hence, 1/2 LSB represents an analog quantity equal to a half of the analog resolution.

The Resolution of an ADC is usually expressed as the number of bits in its digital output code. For example, an ADC with an n-bit resolution has 2^n possible digital codes which define 2^n step levels. However, since the first (zero) step and the last step have only half the full width, the Full-Scale-Range (FSR) is divided into $2^n - 1$ step widths. Hence

1 LSB = FSR / $(2^n - 1)$ for an n-bit converter

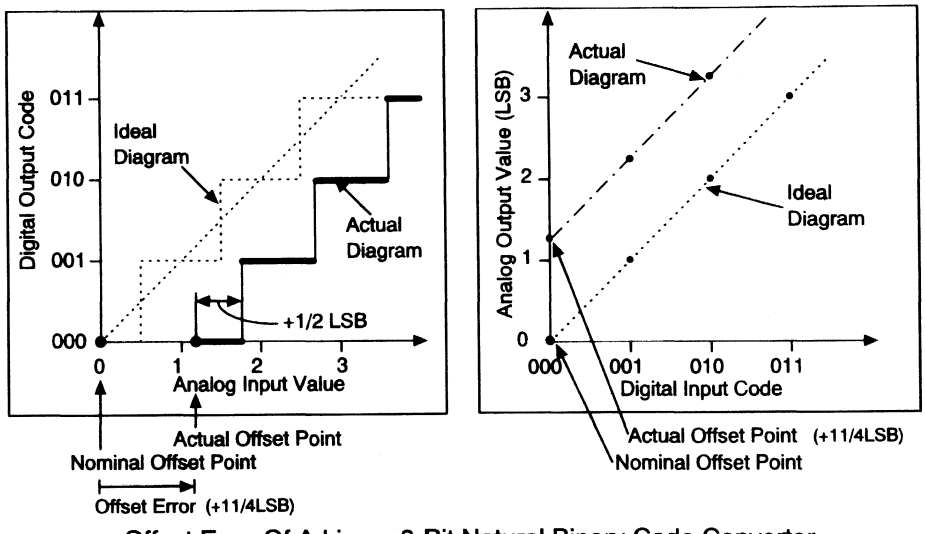
1.1.2. Digital to Analog Converter (DAC)

A DAC represents a limited number of discrete digital input codes by a corresponding number of discrete analog output values. Therefore, the transfer function of the DAC is a series of discrete points . For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. A DAC can be thought of as a digitally controlled potentiometer whose output is a fraction of the full scale analog voltage determined by the digital input code.

1.2.Sources of Static error

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (D.C.) signals, can be completely described by just four terms. These are ***Offset*** error, ***Gain*** error, ***Integral nonlinearity*** and ***Differential nonlinearity***. Each can be expressed in LSB units or sometimes as a percentage of the FSR. For example, an error of 1/2 LSB for an 8 bit converter corresponds to 0.2% FSR.

1.2.1. Offset error

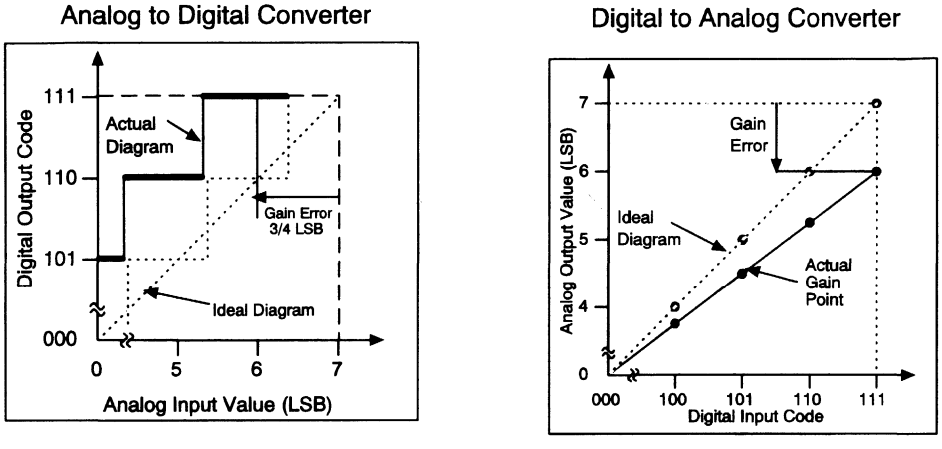


Offset Error Of A Linear 3-Bit Natural Binary Code Converter
(Specified at Step 000)

Figure 3.A2 - Offset error

The offset error is defined as the difference between the nominal and actual offset points as shown . For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero scale error.

1.2.2. Gain error

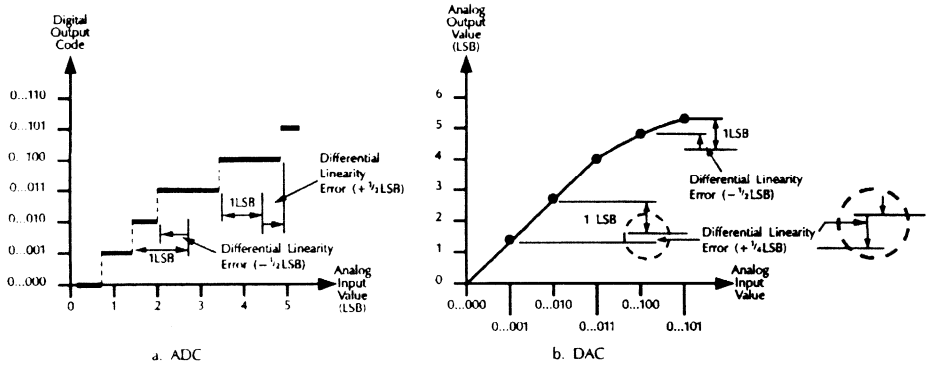


Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After correction of the Offset Error

Figure 3.A3 - Gain error

The gain error is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

1.2.3. Differential Non-Linearity (DNL) Error

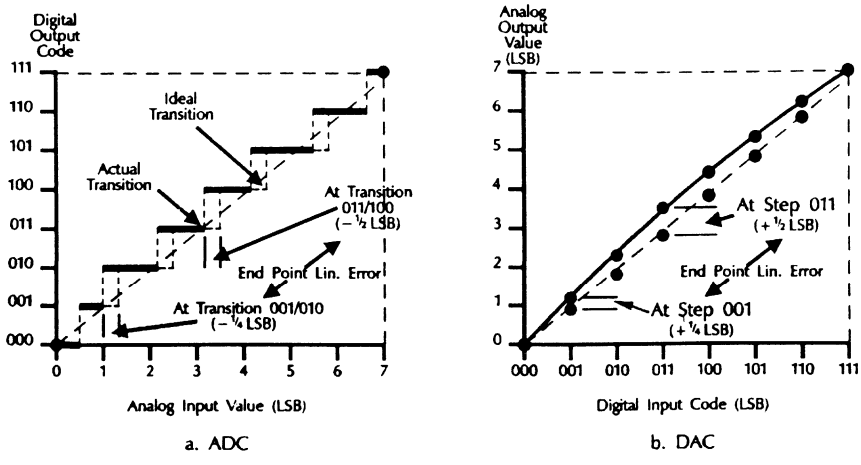


Differential Linearity Error of a Linear ADC or DAC

Figure 3.A4 - Differential Non-Linearity (DNL)

The differential non-linearity error (sometimes seen as simply "differential linearity") is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential non-linearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter may become non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there will be missing codes i.e. one or more of the possible 2^n binary codes are never output.

1.2.4. Integral Non-Linearity Error (INL)



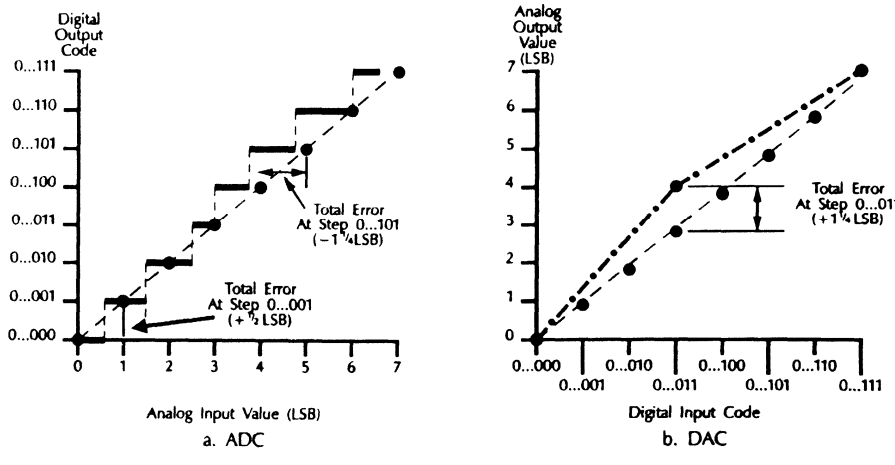
End–Point Linearity Error of a Linear 3–Bit Natural Binary–Coded ADC or DAC
(Offset Error and Gain Error are Adjusted to the Value Zero)

Figure 3.A5 - Integral Non-Linearity (INL)

The integral non-linearity error (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a "best straight line" which is drawn so as to minimise these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called "end-point" linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name "integral non-linearity" derives from the fact that the summation of the differential non-linearities from the bottom up to a particular step, determines the value of the integral non-linearity at that step.

1.2.5. Absolute accuracy error (Total Error)



Absolute Accuracy Error, Total Error of a Linear ADC or DAC

Figure 3.A6 - Absolute accuracy error

The absolute accuracy error or total error of an ADC is the maximum value of the difference between an analog value and the ideal midstep value. It includes offset, gain and integral linearity errors and also the quantisation error in the case of an ADC.

1.3. Aperture error

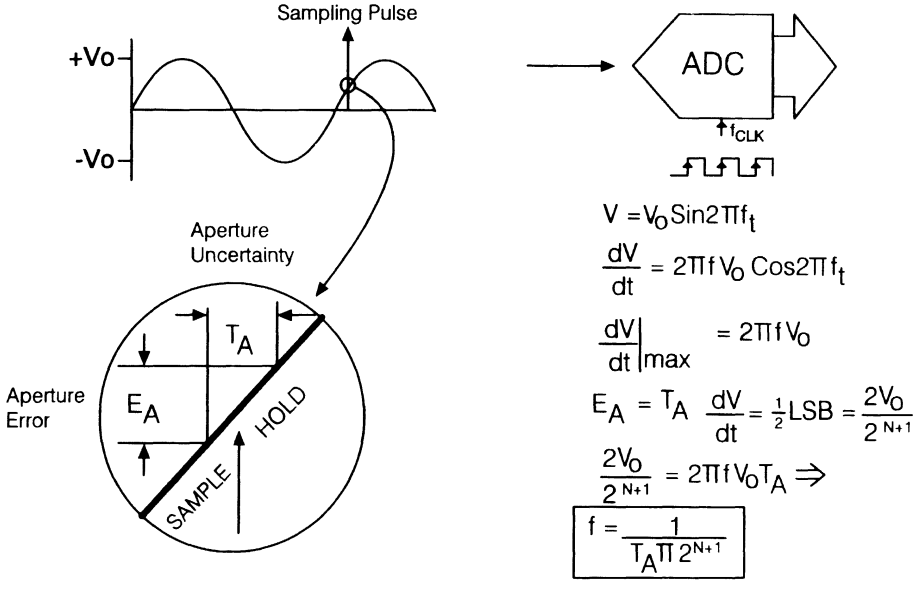


Figure 3.A7 - Aperture error

Aperture error is caused by the uncertainty in the time at which the sample/hold goes from sample mode to hold mode. This variation is caused by noise on the clock or the input signal. The effect of the aperture error is to set another limitation on the maximum frequency of the input sinewave because it defines the maximum slew rate of that signal. For a sinewave input as shown, the value of the input V is defined as:-

$$V = V_0 \sin 2\pi ft$$

The maximum slew rate occurs at the zero crossing point and is given by:-

$$\left.\frac{dv}{dt}\right|_{MAX} = 2\pi f V_0$$

If the aperture error is not to affect the accuracy of the converter, it must be less than 1/2 LSB at the point of maximum slew rate. For an N bit converter therefore:-

$$E_A = t_A \frac{dV}{dt} = \frac{1}{2} LSB = \frac{2V_0}{2^{n+1}}$$

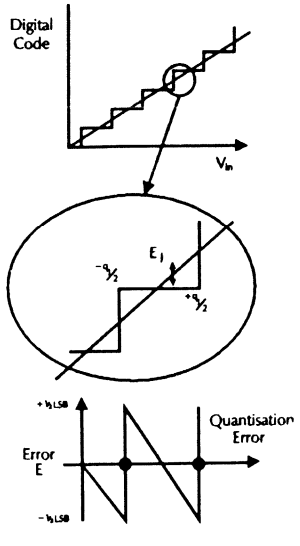
Substituting into this gives

$$\frac{2V_0}{2^{n+1}} = 2\pi f V_0 t_A$$

So that the maximum frequency is given by

$$f_{MAX} = \frac{1}{t_A \pi 2^{n+1}}$$

1.4. Quantisation effects



Error at the jth step

$E_j = (V_j - V_{in})$

Mean square error over the step

$$\bar{E}_j^2 = \frac{1}{q_j} \int_{-\frac{q}{2}}^{+\frac{q}{2}} E_j^2 \, dE = \frac{q^2}{12}$$

Assuming equal steps, total error

$\bar{N}^2 = \frac{q^2}{12}$ (Mean square quantisation noise)

For an input sinewave F(t) = A Sinωt, signal power

$$\bar{F}^2(t) = \frac{1}{2\pi} \int_0^{2\pi} A^2 \sin^2 \omega t \, d\omega t = \frac{A^2}{2}$$

and $q = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$

$$SNR = 10 \log\left(\frac{\bar{F}^2}{\bar{N}^2}\right) = 10 \log\left(\frac{A^2/2}{A^2/3 \times 2^n}\right)$$

$$SNR = 6.02n + 1.76 \text{ dB}$$

Figure 3.A8 - Quantisation effects

The real world analog input to an ADC is a continous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analog signal that were represented by a different voltage on the

input , are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is ***Quantisation noise***.

If we take an ideal staircase transfer function of the ADC, the error between the actual input and its digital form will have a uniform probability density function if the input signal is assumed to be random. It can vary in the range ±1/2 LSB or ± q/2 where q is the width of one step.

$$p(\varepsilon) = 1/q \quad \text{for } (-q/2 \le \varepsilon \le +q/2)$$

$$p(\varepsilon) = 0 \quad \text{otherwise}$$

The average noise power (mean square) of the error over a step is given by

$$E^2(\varepsilon) = \frac{1}{q}\int_{-q/2}^{+q/2} p(\varepsilon)^2 d\varepsilon$$

which gives $E^2(\varepsilon) = q^2/12$

The total mean square error, N^2, over the whole conversion area will be the sum of each quantisation levels mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = q^2/12$$

Considering a sinewave input F(t) of amplitude A so that

$$F(t) = A\sin\omega t$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = 1/2\pi \int_0^{2\Pi} A^2 \sin^2(\omega t) dt$$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$SNR(dB) = 10Log\left[\left(A^2/2\right)\Big/\left(q^2/12\right)\right]$$

But $q = 1LSB = 2A/2^n = A/2^{n-1}$

Substituting for q gives

$$SNR = 10Log\left[\left(A^2/2\right)\Big/\left(A^2/3x2^{2n}\right)\right] = 10Log\left(3x2^{2n}/2\right)$$

$$\Rightarrow \underline{\underline{6.02n + 1.76dB}}$$

This gives the ideal value for an n bit converter and shows that each extra 1 bit of resolution provides approximately 6dB improvement in the SNR.

In practice, the errors mentioned in section 2 will introduce non-linearities that lead to a reduction of this value. The limit of a 1/2 LSB differential linearity error is a missing code condition which is equivalent to a reduction of 1 bit of resolution and hence a reduction of 6dB in the SNR. This then gives a worst case value of SNR for an n-bit converter with 1/2 LSB linearity error.

$$\text{SNR (worst case)} = 6.02n + 1.76 - 6 = 6.02n - 4.24 \text{ dB}$$

Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR.

1.5. Ideal sampling

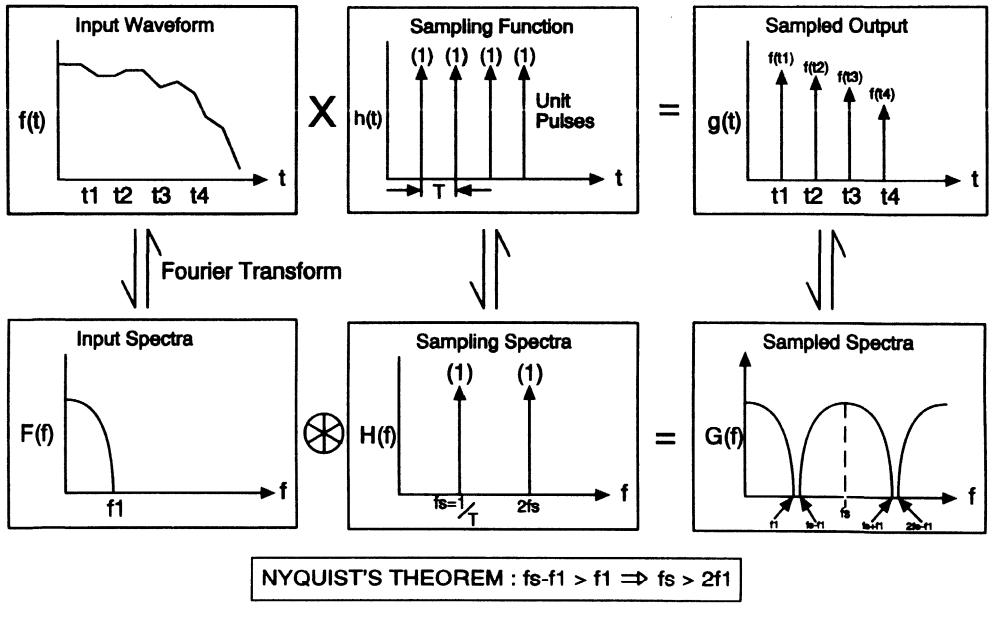


Figure 3.A9 - Ideal sampling

In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, sampling takes the form of a pulse train of impulses

which are infinitessimally narrow yet have unit area. The reciprocal of the time between each impulse is called the sampling rate. The input signal too is idealised by being truly bandlimited, containing no components in its spectrum above a certain value.

The ideal sampling condition is shown here, represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectra of the input signal with that of the pulse train to produce the combined spectrum shown , with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion which is called aliasing.

If we assume the input signal is bandlimited to a frequency f1 , and is sampled at frequency f_S it is clear from the diagram that the overlap (and hence aliasing) will not occur if

$$f1 < f_s - f1 \qquad \text{ie.} \quad 2f1 < f_s$$

Therefore if sampling is done at a frequency at least twice as great as the maximum frequency of input signal, no aliasing will occur and all the signal information can be extracted. This is ***Nyquist's Sampling Theorem***, and it provides the basic criteria for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

1.6. Real sampling

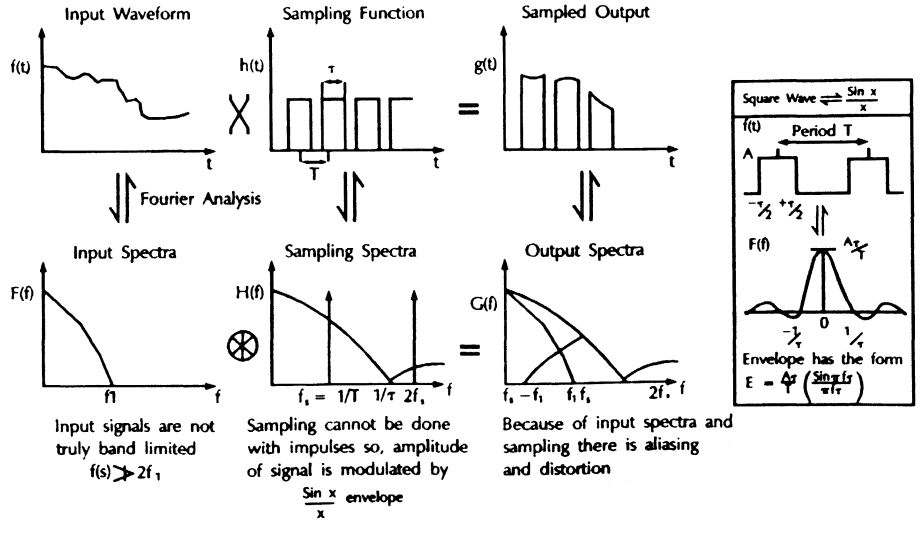


Figure 3.A10 - Real sampling

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal will be a series of pulses of period equalling the reciprocal of the sampling frequency. The result of sampling with this pulse train is a series of amplitude modulated pulses.

Examining the spectrum of the square wave pulse train shows a series of discrete frequencies, as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by (sinx) /x (sometimes written sinc(x)) where x in this case is πf_S. For a square wave of amplitude A, the envelope of the spectrum is defined as

$$Envelope = A\left(\tau/T\right)\left[\sin\left(\pi f_S \tau\right)\right] \ / \pi f_S \tau$$

The error resulting from this can be controlled with a filter which compensates for the sinc envelope. This can be implemented as a digital filter, in a DSP , or using conventional analog techniques. (The TLC32044 Analog interface circuit featured in section 4 has an on-chip sinc correction filter after its DAC output for this purpose).

1.7. Aliasing effects and considerations

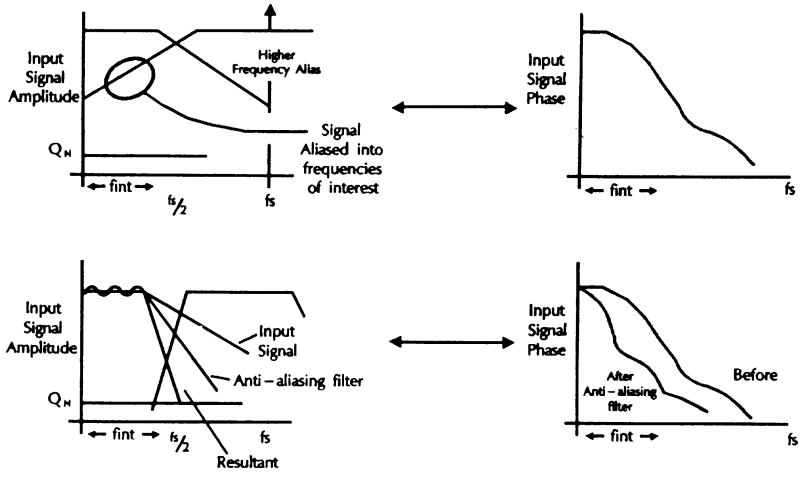


Figure 3.A11 - Aliasing effects and considerations

No signal is truly deterministic and therefore in practice has infinite bandwidth. However, the energy of higher frequency components gets increasingly smaller so that at a certain value it can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As we have seen, the amount of aliasing will be affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution then the noise floor is already relatively high and aliasing may not have a significant effect. However, with a high resolution system , aliasing may increase the noise floor considerably and therefore needs to be controlled more completely.

Increasing the sampling rate is one way to prevent aliasing, as we have seen. However, there will be a limit on what frequency this can be, determined by the type of converter used and also by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analog filters must be used to alter the input signal's spectrum.

1.7.1. Choice of filter

Just as we have already seen with sampling , there is an ideal solution to the choice of filter and a practical realisation that has to make compromises. The ideal filter is a so-called brickwall filter which introduces no attenuation in the passband, and then cuts down instantly to infinite attention in the stopband. In practice , this is approximated by a filter that introduces some attenuation in the passband, has a finite rolloff , and passes some frequencies in the stopband. It may also introduce phase distortion as well as amplitude distortion. The choice of the filter order and type must be decided upon so as to best meet the requirements of the system.

1.7.2. Types of filter

The basic types of filter available to the designer are briefly presented here for comparison. This is not intended to be a full analysis of the subject and the reader should refer to other texts for more details.

Butterworth filter

A Butterworth (maximally flat) filter is the most commonly used general purpose filter. It has a monotonic passband with the attenuation increasing up to its 3-dB point which is known as the natural frequency. This frequency will be the same whatever the order of the filter is . However, by increasing the order of the filter, the roll-off in the passband moves closer to its natural frequency and the roll-off in the transition region between the natural frequency and the stopband becomes sharper.

Chebyshev filter

The Chebyshev equal ripple filter distributes the roll-off accross the whole passband . Hence, it introduces more ripple in the passband but provides a sharper roll off in the transition region. This type of filter has poorer transient and stepping responses due to its higher Q values in stages of the filter.

Inverse Chebyshev filter

Both the Butterworth and Chebyshev filters are monotonic in the transition region and stopband. By allowing ripple in the stopband it is possible to make the roll-off sharper still. This is the principle of the Inverse Chebyshev, based on the reciprocal of the angular frequency in the Chebyshev filter response. This filter is monotonic in the passband, and can be flatter than the Butterworth filter whilst providing a greater initial roll-off than the Chebyshev filter.

Cauer Filter

The Cauer or (Elliptic) filter is non-monotonic in both the pass and stop bands, but provides the greatest roll-off in any of the standard filter configurations.

Bessel-Thomson Filter

All the types mentioned above introduce non-linearities into the phase relationship of the component frequencies of the input spectrum. This can be a problem in some applications when the signal is reconstructed. The Bessel-Thomson or linear delay filter is designed to introduce no phase distortion but this is acheived at the expense of a poorer amplitude response.

In general, the performance of all of these types can be improved by increasing the number of stages i.e. the order of the filter. The penalty for this of course is the increased cost of components and board space required. For this reason, it may be appropriate to use an integrated solution using switched capacitor filter building blocks which provide comparable performance with a discrete solution over a

range of frequencies from about 1kHz to 100kHz They also provide the designer with a compact and cost effective solution .

1.7.3. TLC04 Anti-aliasing Butterworth filter

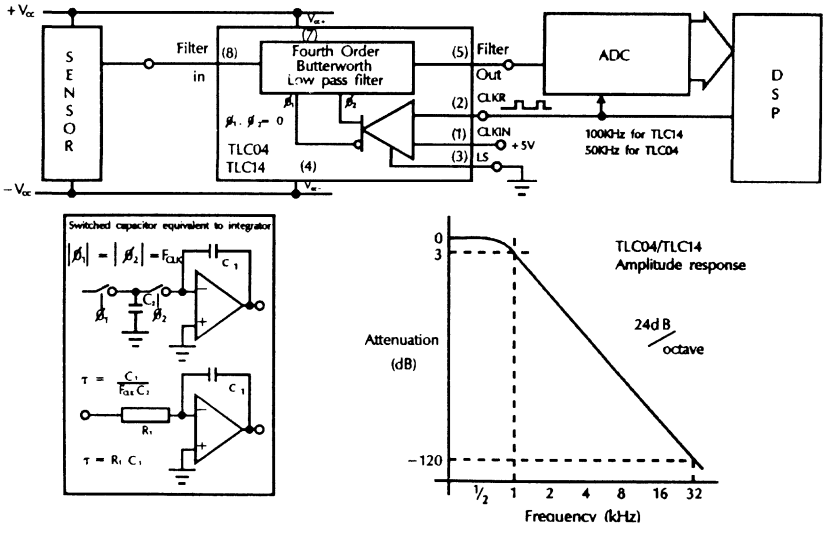


Figure 3.A12 - TLC04 Anti-aliasing Butterworth filter

As detailed previously the Butterworth filter generally provides the best compromise in filter configurations and is by far the easiest to design. The Butterworth filter's characteristic is based on a circle which means that when designing filters, all stages to the filter will have the same natural frequency enabling simpler filter design. Most modern designs which use op-amps are based on building the whole transfer function by a series of second order numerator and denominator stages (a Biquad stage). The Butterworth design is simplified, when using these stages, because each stage has the same natural frequency. This can easily be converted to a switched capacitor filter (SCF) which has very good capacitor matching and accurately synthesized RC time constants.

The Switched capacitor technique is demonstrated in the diagram. Two clocks operating at the same frequency but in complete antiphase, alternately connect the capacitor C2 to the input and the inverting input of an op-amp. During Φ_1, charge Q flows onto the capacitor equal to VinC2. The switch is considered to be ideal so that there is no series resistance and the capacitor charges instantaneously. During Φ_2, the switches change so that C2 is now connected to the virtual earth at the op-amp input. It discharges instantaneously delivering the stored charge Q.

The average current that flows Iav depends on the frequency of the clocks T so that

$$I_{AV} = Q/T = V_{IN}\, C_2/T = V_{IN} C_2 F_{CLK}$$

Therefore, the switched capacitor looks like a resistor of value

$$R_{eq} = V_{IN}/I_{AV} = 1/C_2 F_{CLK}$$

TLC04 Fourth order Butterworth filter

- **Low Clock to Cutoff frequency error ... 0.8%**
- **Cutoff depends only on stability of external clock**
- **Cutoff range 0.1Hz to 30kHz**
- **5V to 12V operation**
- **Self clocking or both TTL and CMOS compatible**

The advantage of the technique is that the time constant of the integrator can be programmed by altering this equivalent resistance, and this is done by simply altering the clock frequency. This provides precision in the filter design, because the time constant then depends on the ratio of two capacitors which can be fabricated in silicon to track each other very closely with voltage and temperature. Note that the analysis assumes Vin to be constant so that for an a.c. signal , the clock frequency must be much higher than the frequency of the input .

The TLC04 is one such filter which is internally configured to provide the Butterworth lowpass filter response, whose cut-off frequency is controlled by a digital clock. For this device, the cut-off frequency is set simply by the clock frequency so that the clock to cut-off frequency ratio is 50:1 with an accuracy of 0.8%.This enables the cut-off frequency of the filter to be tied to the sampling rate, so that only one fundamental clock signal is required for the system as a whole. Another advantage of SCF techniques means that fourth order filters can be attained using only one integrated circuit and they are much more easily controlled.

The response of an nth order Butterworth filter is described by the following equation.

$$Attenuation = \left[1 + \left(f/f_C\right)2^n\right]^{1/2}$$

For the fourth order realisation in the TLC04, this corresponds to the table below.

frequency	attenuation (factor)	attenuation (dB)	phase (deg)
$F_c/2$	0.998	0.02	26.6
F_c	0.707	3	45
$2F_c$	0.0624	24	63.4
$4F_c$	0.00391	48	76
$8F_c$	0.000244	72	82.9
$12F_c$	0.000048	86	85.2
$16F_c$	0.000015	96	86.4

This means that sampling at 8 times the centre frequency gives an input to aliased signal ratio of 67dB, which is less than ten bit quantisation noise distortion.

1.7.4. The TLC10 as an antialiasing Cauer filter.

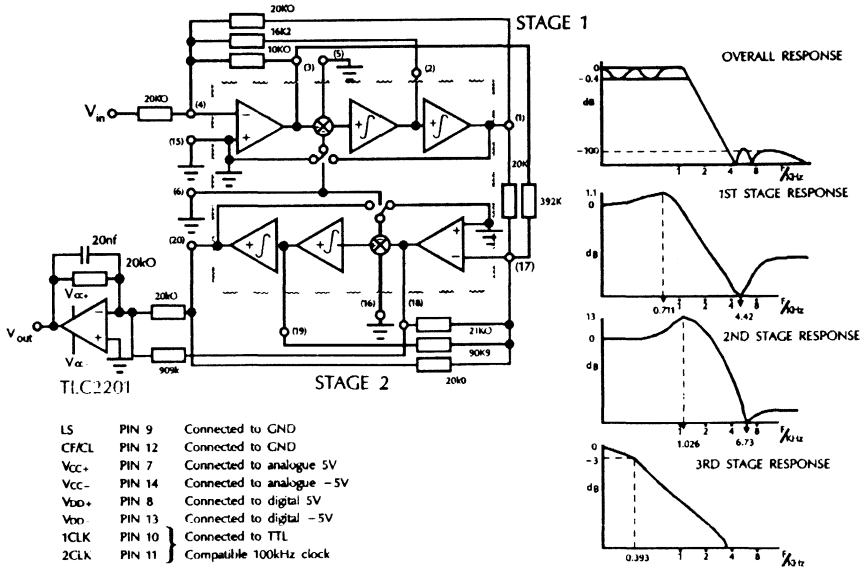


Figure 3.A13 - The TLC10 as an antialiasing Cauer filter.

If a smaller roll-off in the passband and a faster roll-off in the transition region is required so that the signals aliased back into the passband are more attenuated, the Cauer filter can be used to provide this with a smaller order filter.

Switched capacitor filters can be used for this too. The TLC10 is a general purpose SCF building block that contains two independent active filter sections, each of which is designed to provide the response of a second order filter. These can be configured to produce any of the filter types listed in foil 20. In this example , it is configured to realise the Cauer filter configuration.

The Cauer filter has non-monotonic response in both the passband and the stopband. In this application , it is built up from two notch filters and a final low pass filter. The two halves of the TLC10 are used to build the notch filters which are realised as a combination of a low pass filter and a high pass filter . For the first stage, these two components are summed at the input of the second stage. Likewise, for the second stage, the high and lowpass functions are summed using an external summing amplifier built around the TLC2201. This also provides the benefit of further filtering so that the combination becomes a fifth order filter.

TLC10 Universal Dual Switched-capacitor filter

- **Low Clock to Cutoff**
- **frequency error ... 0.6%**
- **Cutoff depends only on stability of external clock**
- **Cutoff range 0.1Hz to 30kHz**
- **+/-4V to +/-6V operation**

As in most filters the lowest Q factor stage is placed first so as to minimise overshoot caused by high frequency elements in the input signal. To enable the op-amps to function properly and without excess distortion, the smallest resistor value is set to be 10k to minimise the current loading.

The fifth order Cauer filter shown is designed to have the following characteristics:

Passband ripple: 0.5 dB
Cut-off frequency: 1 kHz
Stopband frequency: 4 kHz
Stopband attenuation: 97.5 dB

The zeroes and poles are set in the following positions:

1st stage	f1=0.7112KHz	Q1=1.1403	Z1=4.4199
2nd stage	f2=1.0260KHz	Q2=4.4386	Z2=6.7342
3rd stage	f3=0.3933KHz		

1.8. Grounding techniques

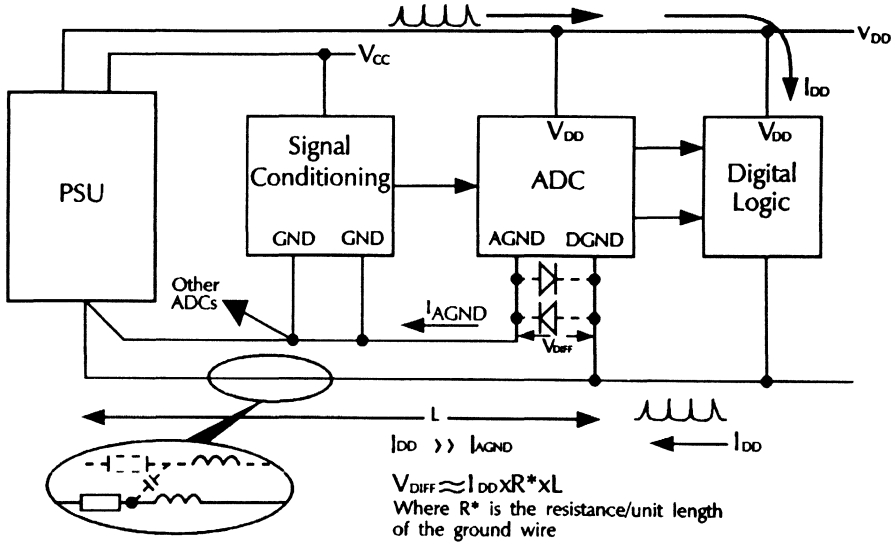


Figure 3.A14 - Grounding techniques

One more area that needs careful consideration is the system of grounding used. It must be remembered that every wire or track on a PCB has a small, but finite, series resistance and inductance plus some equivalent shunt capacitance.

Principle: Think where the currents will flow!

In a mixed analog and digital system, it is likely that the digital processor and associated logic will draw the majority of the current. If the return paths for the digital and analog portions are linked into the same ground rail, the large dc current may cause significant "IR" voltage drops so that the voltage at the various ground points is different. In a high resolution converter such as the 10 bit TLC1540, 1/2 LSB at 5V reference corresponds to only 2.5mV, which can easily be exceeded.

Linking the digital and analog grounds together also introduces the possibility of current spikes from the high speed switching feeding through to the analog ground. It is therefore recommended as a minimum that the analog and digital grounds should be kept separate and should be terminated at the ground of the Power supply unit (PSU). Even better is to provide separate return paths for all currents , tied together only at a single analog ground reference point.

However, this causes a potential hazard in that the level of the analog and digital grounds at the ADC may be different. This allows the situation whereby the internal diodes may become forward biased and hence cause damage to the device. To prevent this, the analog and digital grounds at the ADC should be tied together using "nose on tail" diodes. This creates a maximum differential of 1 Vbe drop between the rails, or 0.4V if Shottky diodes are used.

Section 4
Data Transmission

Section Contributions by:

Geoffrey Arnold

Kevin Gingerich

Andrew Faulkner

Tim Ardley

Alun Webber

Contents Section 4.

1. Introduction

1.1. Data Transmission

It may seem strange that TI's 'Data transmission' products are included within the Linear seminar. Data Transmission as part of TI's Linear Products portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are

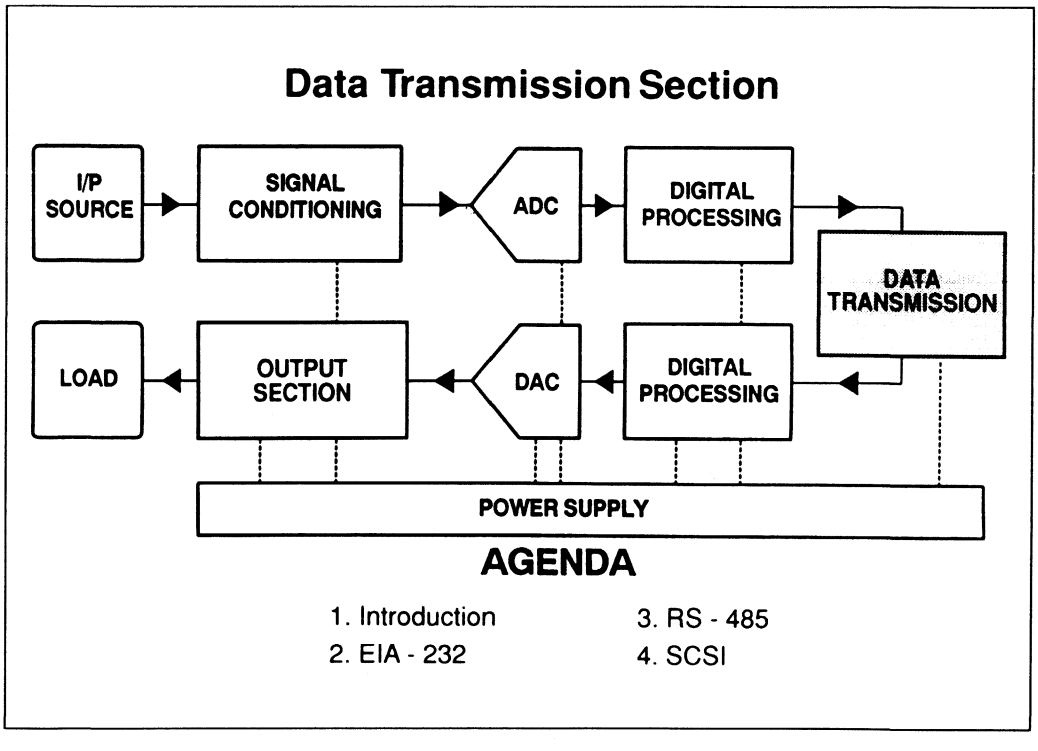


Figure 4.1 - Data Transmission

primarily of an analog more than a digital nature. Likewise the design of data transmission ICs requires experienced analog engineers to implement functions such as slew rate limiting, receiver filtering and common-mode protection.

In this year's seminar we will concentrate on two very popular transmission standards, RS-232 or as it is now known EIA/TIA-232-E, and the multi-point, half duplex RS-485 standard. The last section covers the physical layer of the increasingly popular Small Computer Systems Interface Standard (SCSI).

1.1.1. The Need for Transmission Standards

Data transmission standards evolved for two main reasons: From the need to transmit data reliably over long distances, and to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/Logic signal levels and products can be used, they generally lack the power handling capabilities, robustness and noise margins required for reliable transmission. Indeed for backplane equipment, TTL is no longer specified for the newer high speed standards, such as Futurebus+ which uses BTL transceivers. In general the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness and higher power outputs than can be delivered using conventional 'Logic' products. Similarly the sub-micron technologies used in the fabrication of today's logic devices cannot provide the power handling and robustness necessary for successful long distance transmission.

1.1.2. Specialist Technologies

This leads to the need for specialist ICs, and technologies, to meet the exacting requirements of these transmission standards. The traditional technological answer has been to utilise the inherent robustness afforded by bipolar technologies, however the additional need for low power consumption and high levels of integration no longer makes this attractive. SC manufacturers are now having to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology combining the robustness of bipolar together with the power consumption and integration afforded by CMOS. Other manufacturers are using pure CMOS and integrating shottky diodes to the same end. The result is very specialised and reliable products that are able to withstand the harsh environment unique to data transmission products.

Texas Instruments has been a leading supplier of data transmission products for many years, and is continually innovating new fields. Although the following sections are limited to the more common

interface standards, TI is actively involved in many new emerging standards and markets, for example Futurebus+, a backplane standard with virtually no ceiling on data rate, the high speed serial data link evolving from the P1394 committee and multiplex wiring systems such as ABUS, CAN and VAN. The reader is advised to contact a TI representative for information on these product areas.

With the considerable expertise in design, product definition and range of technologies Texas Instruments is the ideal choice for supplying your data transmission product requirements.

1.1.3. About This Section

This Section is split into four distinct sections each of which provides a practical rather than theoretical approach to in an attempt to give the reader an insight into three popular data transmission standards, EIA/TIA-232, RS-485 and the SCSI standard. The Section is split as follows:

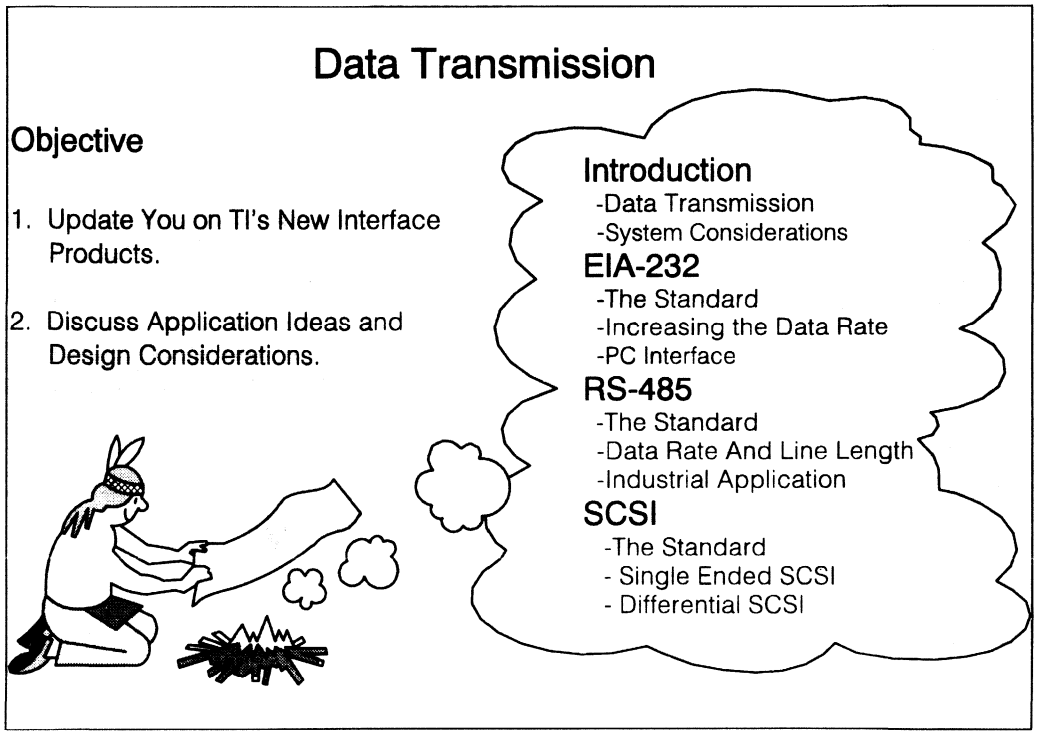


Figure 4.2 - Data Transmission Agenda

1. Introduction: An overview of the various factors that affect any data transmission system. Under discussion is the line length versus data rate trade-off, noise sources, correct line termination and network topology in addition to explaining the use of eye patterns as a tool to measure transmission quality.
2. EIA-232: A discussion of the standard with particular attention paid to the changes made in the 'E' revision. Also covered is the use of '232' at higher data rates, up to 116 kbps (kilo bits per second) and an application focus on the popular DB9 PC interface. Particular attention is paid to TI's new products throughout the section. The generic '232' standard will be referred to in this book as EIA-232, where a parameter is unique to a specific revision the EIA-232 reference will be used.
3. RS-485: An overview of the RS-485 specification followed by a design example. We use an industrial control application to understand the factors that need to be taken into account when

designing an RS-485 system. Highlighted throughout the section will be TI's new products compliant with this standard.

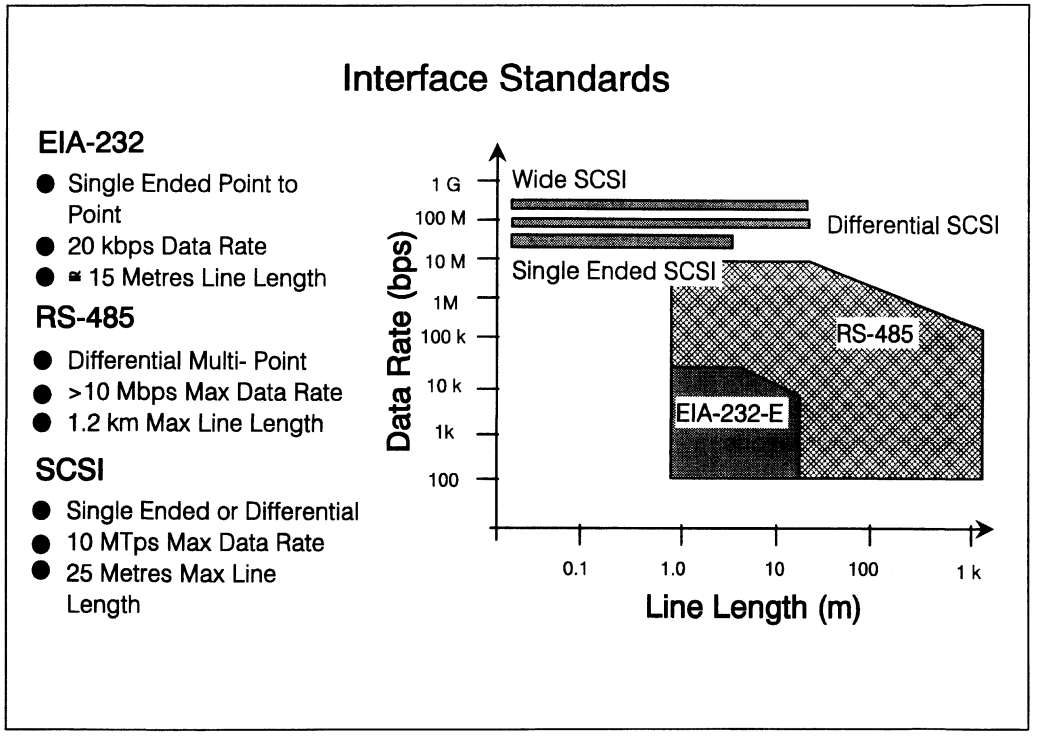


Figure 4.3 - Interface Standards

4. SCSI: We will consider the physical layer of this standard that concern both single ended and differential transmission. For single ended transmission we will look specifically at optimising the line termination to achieve maximum transmission rate over the 6 metre distance as specified in the standard. The differential SCSI system increases the line length to 25 metres and uses the RS-485 standard to achieve this. We will look at TI's new nine channel RS-485 transceiver which minimises the problems caused by the 18 line wide bus as defined by the standard.

1.2. Overview of the Interface Standards

Referring to Figure 4.3 we can see the relationship of each transmission standard when comparing data rate and line length.

1.2.1. EIA/TIA-232

EIA-232 or 'Recommended Standard' 232 is defined in the ANSI (American National Standard Institution) specification as "The Interface Between Data Terminal Equipment and Data Circuit-

Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a Computer Terminal (DTE) and a modem (DCE). The standard has evolved over the years with the latest 'E' revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association.

As with previous revisions of the standard the maximum data rate is defined as 20 k bits per second (kbps) although there are now a number of software applications that now push this data rate up to 116 kbps, well outside the standard. The 'C' revision defined the maximum line length as 15 metres however this failed to comprehend the type of cable used and consequently the load capacitance on the line driver. Both the 'D' and 'E' revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF that translates using standard cables to between 15 and 20 metres. Line length and data rate are limited as the standard employs single ended communication which is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

1.2.2. RS-485

RS-485 was primarily an upgrade to the EIA RS-422-A standard utilising the same signal levels but facilitating half duplex multi-point communication. The standard is less complex than the EIA-232 standard as it only specifies the physical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24 AWG cable based on 6 dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time which is influenced both by the line driver and the line length and the line loading. In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

1.2.3. Small Computer Systems Interface (SCSI)

SCSI is an industry-standard interface, defined by the ANSI, for the interchange of data between computer and computer peripherals. Standard SCSI is a byte wide parallel interface for high speed data transfer over relatively short distances. The SCSI bus is bi-directional and is terminated at both ends of the cable to reduce reflections. For the single ended interface the standard specifies a maximum line length of 6 metres. The maximum data rate is not specified but at present 5 Million Transfers per second (MTps) is achievable using active termination. This can be increased up to 10 MTps using innovative termination as we will discuss later. For longer line length applications, up to 25 metres, the SCSI standard defines the interface using the RS-485 standard as the physical layer. This pushes the data rate to 10 MTps over the full 25 metres which equates to 80 Mbps. A further development of SCSI is 'Wide' SCSI which increases the data bus to 16 bits wide. Using the 10 MTps differential interface this increases the bit rate to 160 Mbps.

1.2.4. Summary of EIA Interface Standards

Parameter		EIA-232	RS-423-A*	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output	Unloaded	±5	±3.6	±2	±1.5
Levels (V)	Loaded	±15	±6	±5	±5
Driver Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/µs (Max.)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to –7 or 12 V
Driver Output Resistance -	Power on	NA	NA	NA	12 k
High Z state (Ω)	Power off	300	60 k	60 k	12 k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

1.3.System Influences

Noise, distortion and attenuation are always present in data transmission systems and strictly limit performance. We will consider each one of these in turn although there is some overlap i.e. noise can cause distortion.

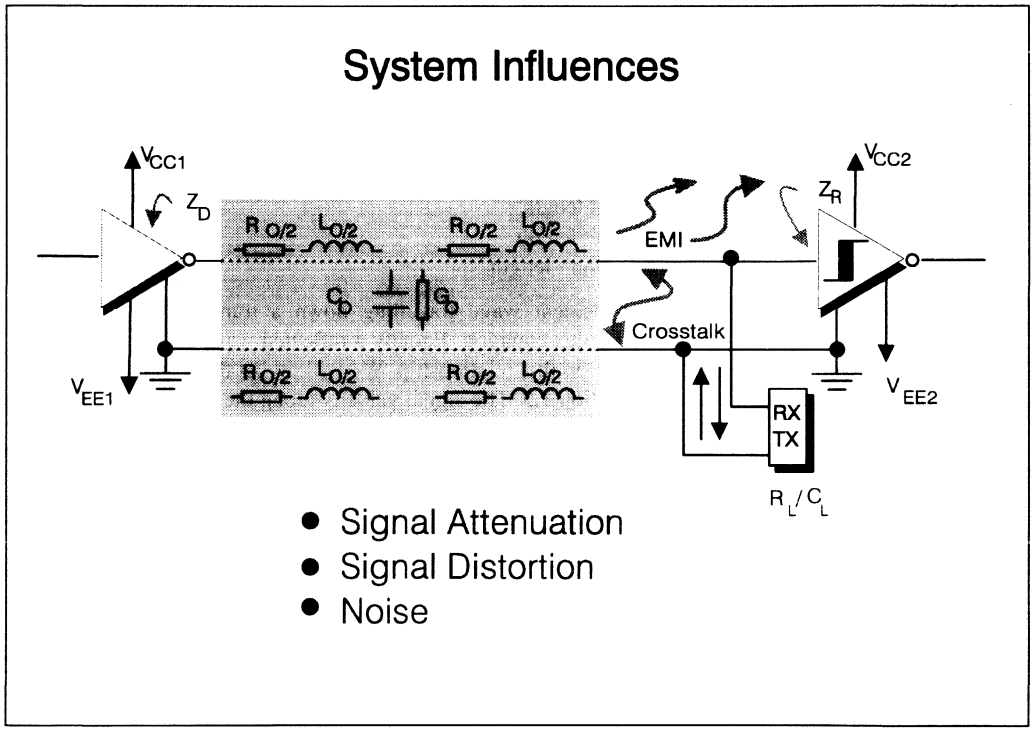


Figure 4.4 - System Influences

1.3.1. Signal Attenuation

Any data transmission over wire experiences losses and distortion due to distributed constants present along the cable: distributed series inductance, distributed shunt capacitance, distributed series resistance and distributed shunt conductance. Attenuation of the signal in a cable is affected by each of the these components. The series resistance, **R**, is frequency dependent and is a result of the DC resistance of the cable and the skin effect. Skin effect is a term which refers to the tendency of electrons to travel to the surface of a conductor at higher frequencies, thereby reducing the overall cross sectional area and increasing the resistance. The series inductance, **L**, represents the opposition to change in current levels caused by the collapsing and expanding magnetic fields created due to fluctuating current levels. The shunt capacitance, **C** ,is created by the two conductors in close proximity and separated by a dielectric. As the signal frequency increases the capacitive reactance

decreases, consequently reducing the opposition to current flow. The final component, shunt transconductance or **G**, is a function of the dielectric loss of the insulation around each conductor which allows some leakage current to pass between conductors. In modern dielectrics this is often assumed to be negligible.

The overall effect of these distributed constants is called the characteristic impedance of the line, $\mathbf{Z_0}$, and is expressed as:

$$\mathbf{Z_0} = \sqrt{\frac{\mathbf{R} + \mathbf{j}2\pi\mathbf{fL}}{\mathbf{G} + \mathbf{j}2\pi\mathbf{fC}}}$$

Where: **L** is in henries/unit length
R is in ohms/unit length
C is in farads/unit length
G is on siemens/unit length

The current/voltage relationship of an incident wave travelling down a transmission line in the direction of the load will be determined by this equation. Equally a reflected wave travelling from the direction of the load will also be dependent on this relationship. We will revisit this equation when we discuss transmission line termination in section 1.5. The signal velocity along the transmission line and the attenuation depends upon the propagation constant γ of the line. The propagation constant, when separated into its real and imaginary parts, is symbolised by $\alpha + j\beta$ where α is known as the attenuation constant and β as the phase constant. α determines the rate of attenuation and has units of nepers per unit length, and β determines the phase velocity, where:

Phase velocity,

$$\mathbf{Vp} = \frac{\omega}{\beta}$$

Where ω is the angular velocity.

Additionally, the propagation constant,

$$\gamma = \alpha + j\beta = \sqrt{(\mathbf{R} + \mathbf{j}\omega\mathbf{L})(\mathbf{G} + \mathbf{j}\omega\mathbf{C})}$$

In practice the attenuation of a particular cable can be determined from manufacturers data where usually a curve of bit rate or frequency is plotted against dB, usually quoted per 100 ft or 30 metres. The attenuation constant, β, can be converted to dBs by multiplying by 8.686.

The maximum attenuation allowable will be dependent on the system configuration but a figure of 6 dBV maximum is a good guide. Actual curves are discussed later in the RS-485 section.

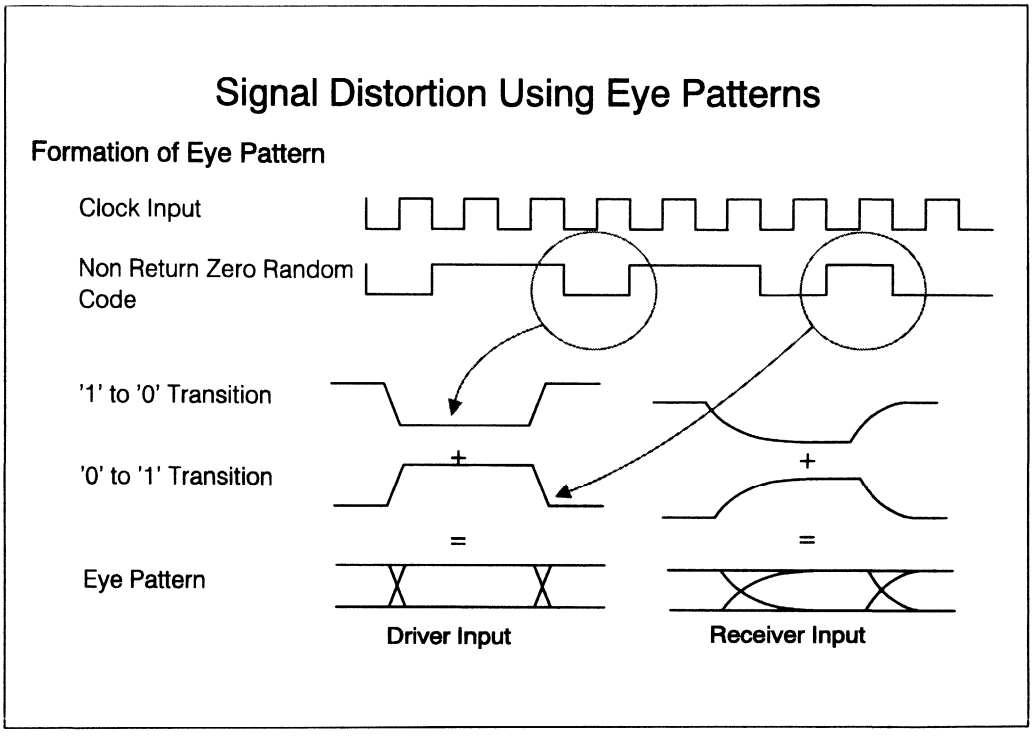


Figure 4.5 - Signal Distortion Using Eye Patterns

1.3.2. Signal Distortion

One of the primary causes of signal distortion is the effect known as frequency dispersion. As discussed in 1.3.1. phase velocity and attenuation are both frequency dependent and whose effect is to distort and delay the signal pulse. The high frequency components contained in the leading and lagging edges of a pulse experience minimum delay but experience maximum attenuation. The pulse top and low frequency components are subjected to increased delays. The result is that various parts of the pulse arrive at the receiving end at different times and at differing levels causing distortion of the original signal. It follows the longer the line length the more the bit rate must be reduced. In many transmission systems it is this factor alone which determines the maximum signalling rate.

Once again cable manufacturers sometimes specify a bit rate versus line length curve but a better way to check signal distortion of your system is by the use of eye patterns or eye diagrams. Indeed cable manufacturers generate their bit rate/distance curves using eye pattern measurements. Eye patterns allow you to visibly see and measure signal distortion as a function of data rate. See later sections on how to implement Eye Patterns.

1.3.3. Noise

Noise is generated from a variety of sources and can strongly influence how you implement your data transmission system. All extraneous signals appearing at the receiving end of the transmission circuit that are not due to the input signal are considered as noise. The two most likely sources of noise that will affecting data transmission systems in the context of this Section are common-mode voltages and cross talk. We will discuss both these types of noise and how the relate to the type of transmission system in section 1.6.

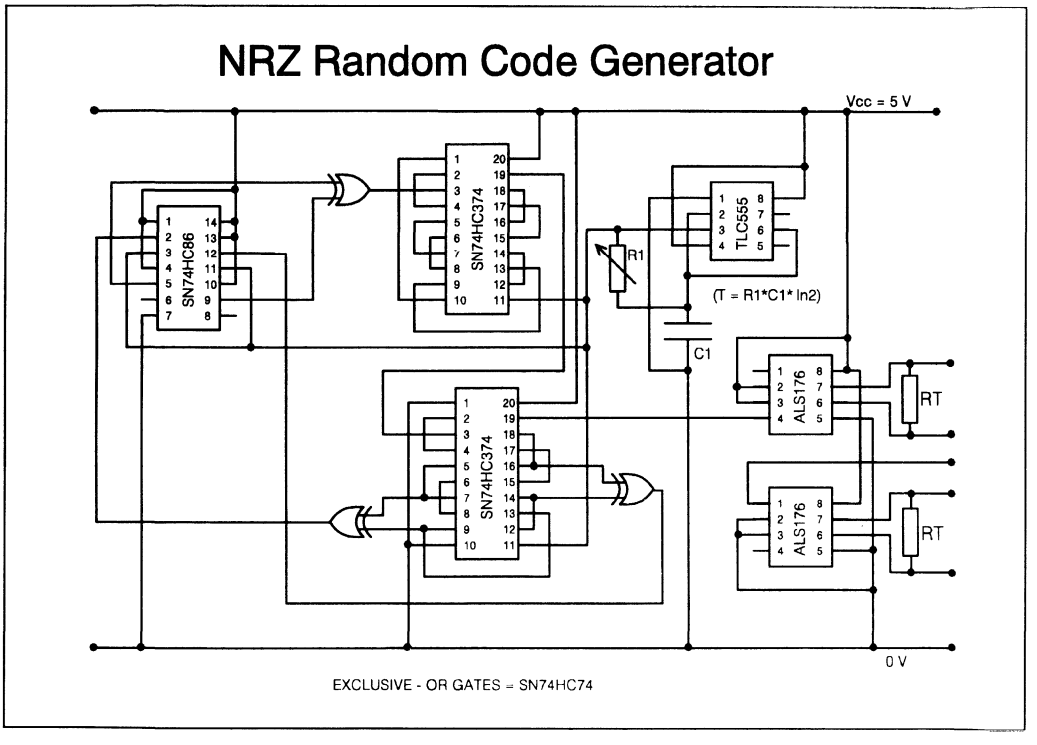


Figure 4.5.1 - NRZ Random Code Generator

1.4. Eye patterns

To determine the effects of signal distortion, noise etc. on Intersymbol interference (ISI) in a data transmission system the eye pattern is used. ISI is the effect of neighbouring pulses in a pulse train spilling over into adjacent pulses and forces a reduction in the allowable permitted pulse rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope with the term 'Eye' coming from the appearance of the trace on the CRT.

1.4.1. Setting up the eye pattern

The eye pattern is obtained by applying a random non return zero (NRZ) code down the transmission line under test. This represents all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the 'scope triggered using the synchronisation clock to the NRZ code generator on a separate trace. See figure 4.5 Over any one unit interval the random code generator should produce a combination of signals. The resulting signals can then be viewed on the oscilloscope over one unit interval, each unit interval should resemble an eye, similar to figure 4.6. For differential transmission both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

Figure 4.5.1 shows a circuit to generate the NRZ code. In this case we have used it to test the RS-485 SN75176 type transceiver.

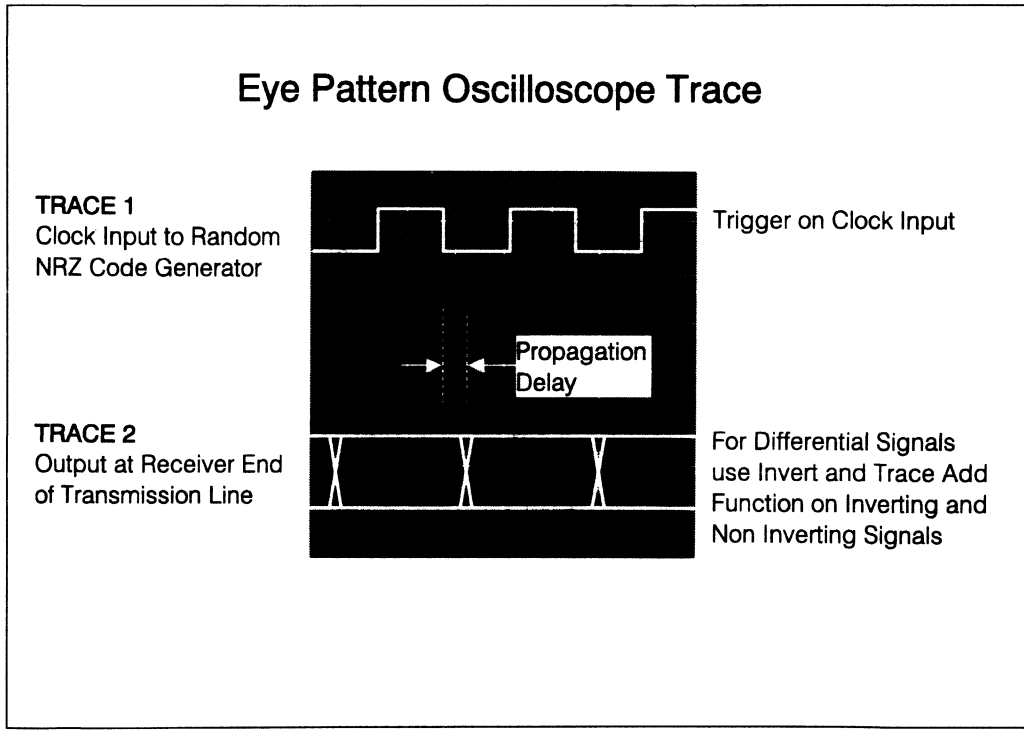


Figure 4.6 - Eye Pattern Oscilloscope Trace

1.4.2. Taking Measurements from Eye Patterns

Before considering actual measurements the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The 'openness' of the eye is an indication of

the 'quality' of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

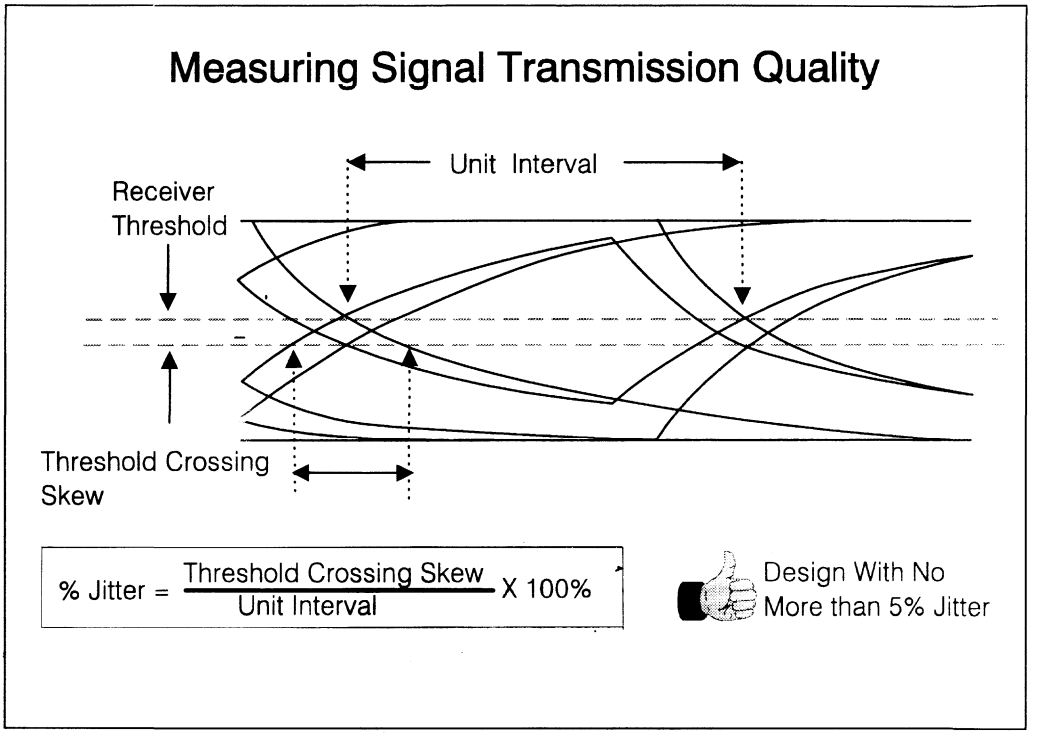


Figure 4.7 - Measuring Signal Transmission Quality

For actual measurements the decision points of the transceiver should be superimposed upon the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum jitter tolerance of the system. A good guide, and one that is used by cable manufacturers to determine data rate versus line length curves, is to design with no more than 5% jitter. Where % jitter is defined as the ratio of Threshold crossing Skew to unit interval as shown in Figure 4.7. Jitter is caused by a number of factors including , signal frequency, noise and cross talk. (Noise frequency can modulate the transmitted signal, for example 50 Hz hum or from other low frequency sources). It should also be noted at this point the effect of threshold misalignment which can cause severe problems with the received signal, reducing the detected pulse width considerably.

1.5. Line Termination

The behaviour of the transmitted signal and the integrity of the data at the receiving end depends upon the data rate and line length of the cable. There are two behavioural models; of a transmission cable:

i. **Lumped parameter model (Short wire) .**

ii. **Distributed parameter model (Transmission line)**

As discussed in section 1.3.1 the distributed parameter model models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections and as a result the transmission line is said to have a characteristic impedance, Z_0. Z_0 is independent of distance along the line and represents the voltage and current relationship for an incident wave at any point as it travels along the line.

1.5.1. Transmission Line Test

Classifying as a Lumped or Distributed Parameter Model

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings.

Consider a signal propagating down a simple data link comprising two wires. When the signal starts to change at the transmitter output the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter terminals.

If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system.

A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated; If the rise time , t_T, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given in figure 4.8 where a safety margin is built in to the propagation delay/rise time relationship.

1.5.2. Transmission Line Considerations & Effects

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. This extra load decreases the line impedance and reduces the speed of the signal along the line.

In the case of the lumped parameter model the line represents a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of the transmitter (assuming it can supply a finite amount of current to the line).

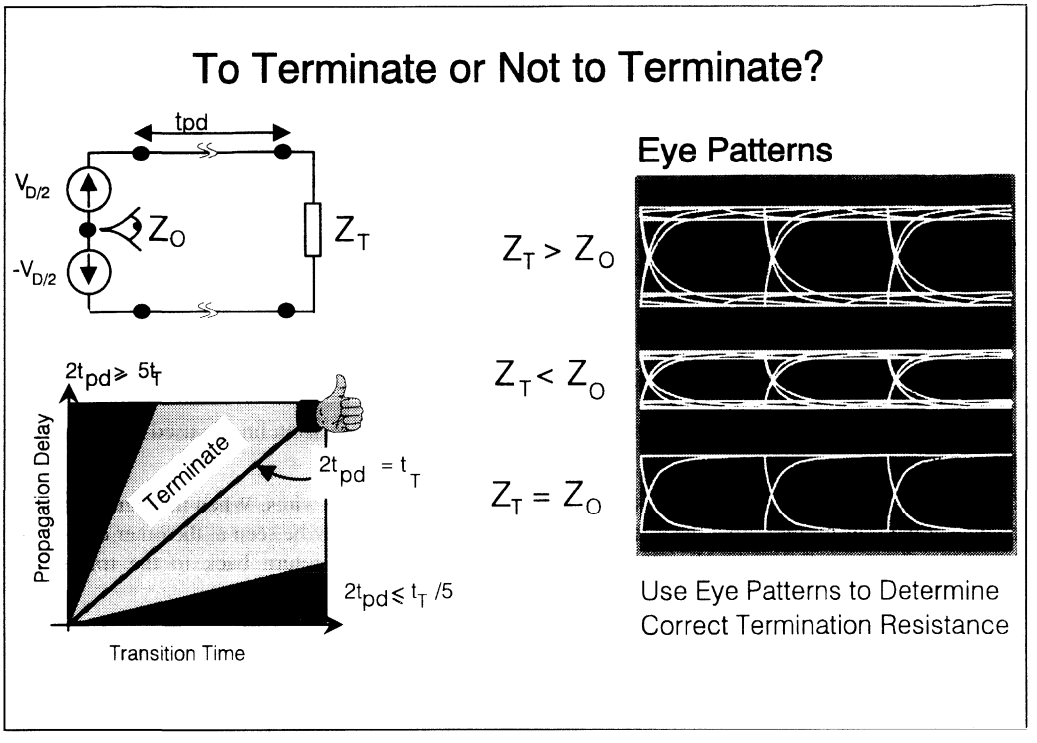


Figure 4.8 - To Terminate or Not to Terminate?

1.5.3. Transmission Line Reflections

Consider a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This will cause the voltage at the output of the driver circuit to reduce as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

At any point along the line the ideal source impedance will appear as Z_O and the ideal load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source of twice the magnitude of the line voltage.

When the signal reaches the receiving end of the line it sees a terminating impedance equal to the impedance (Z_O) of the line that it is already travelling on. It interprets this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is dis-similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size

of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line.

Reflections at each end of the line will eventually settle and leave a constant dc voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False receiver triggering can occur and repeated signal reflections will cause signal wave distortion.

1.5.4. Using Eye Patterns to Determine Z_0

Referring back to eye patterns, these can also be used to find the characteristic impedance of a transmission line. Figure 4.8 shows three sets of eye patterns, $Z_T > Z_O$, $Z_T < Z_O$, and $Z_T = Z_O$, where Z_T is 200 Ω, 50 Ω, and 100 Ω, respectively. Where $Z_T > Z_O$ the signal is larger with multiple traces, while with $Z_T < Z_O$ the signal is similar but much reduced in amplitude and could cause signal to noise ratio problems at the receiver. With $Z_T = Z_O$, the signal is very clear with a near perfect eye pattern. In practice it is possible to use a variable resistance and the eye pattern to determine the correct termination impedance for zero reflections.

1.6. Noise Influences

There are two main classification of transmission scheme, single ended or differential. Each are affected by noise influences in differing ways - the next two section describe each transmission scheme paying particular attention to the affects of noise. Figure 4.9 details both types of transmission scheme.

1.6.1. Single Ended Line Considerations

Single ended data transmission systems consist of a signal line on which data is sent down, and a ground line through which the current returns. A direct result of this is that the ground line forms part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single ended system is the lowest cost solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise.

Cross talk is also a major concern especially at high frequencies. Cross talk is generated from both capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line

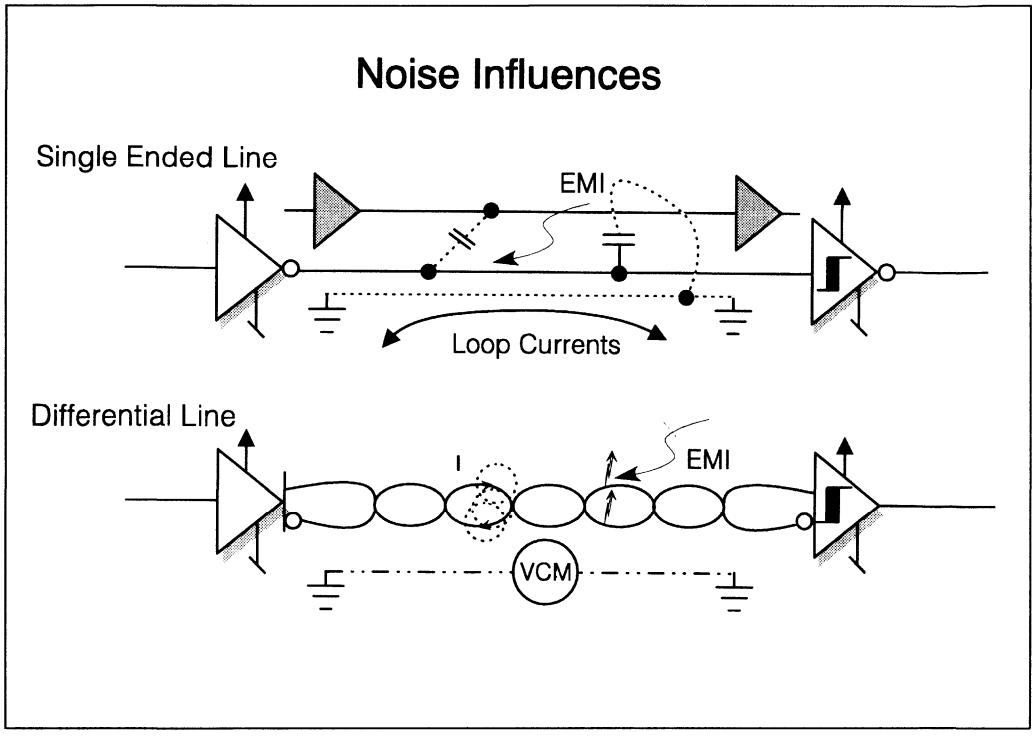


Figure 4.9 - Noise Influences

determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

Cross talk can be reduced by;

i. **Limiting the slew-rate of signals so that they do not cause cross talk to be induced onto other lines**

ii. **Limiting the line length.**

iii. **Shielding the signal conductor.**

While the common-mode noise could be reduced by:-

i. **Isolating the signal ground from power conductors (e.g. keep signal grounds separated as far as possible from power grounds).**

ii. **Ground wires should be as low as impedance as possible.**

iii. **Using star ground system configurations.**

Some of these techniques are used in systems such as EIA-232 e.g. Maximum slew rate of EIA-232 is defined as 30 V/μs while Futurebus+, an emerging high speed backplane standard, uses trapezoidal waveforms to limit cross talk

1.6.2. Differential Line Considerations

A differential communication system involves the use of two signal carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of this is the receiver is only concerned with the ***difference*** in voltage between the two wires. The absolute value of the dc common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

The use of a differential communications interface allows transmission at higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and cross talk are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost but provides superior performance when data is transmitted at high rates over long distances.

The RS-485 and RS-422-A standards both use differential type transmission.

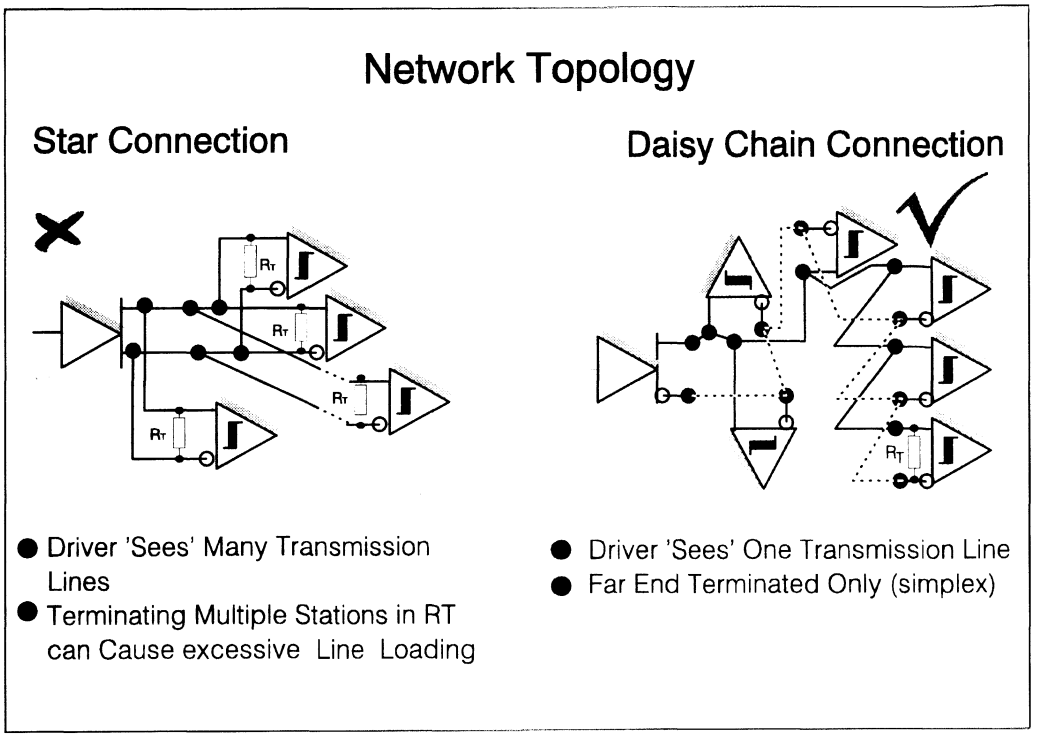


Figure 4.10 - Network Topology

1.7. Network Topology

In addition to considering signal attenuation, the effects of noise, signal distortion and correct line termination, we must also consider the way in which stations are connected to the line. Furthermore the position of the line termination resistor and device positioning must be considered. There are two basic methods of connection, see figure 4.10;

i. **The star connection**

ii. **The daisy chain connection**

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended and is accounted for in each standard. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

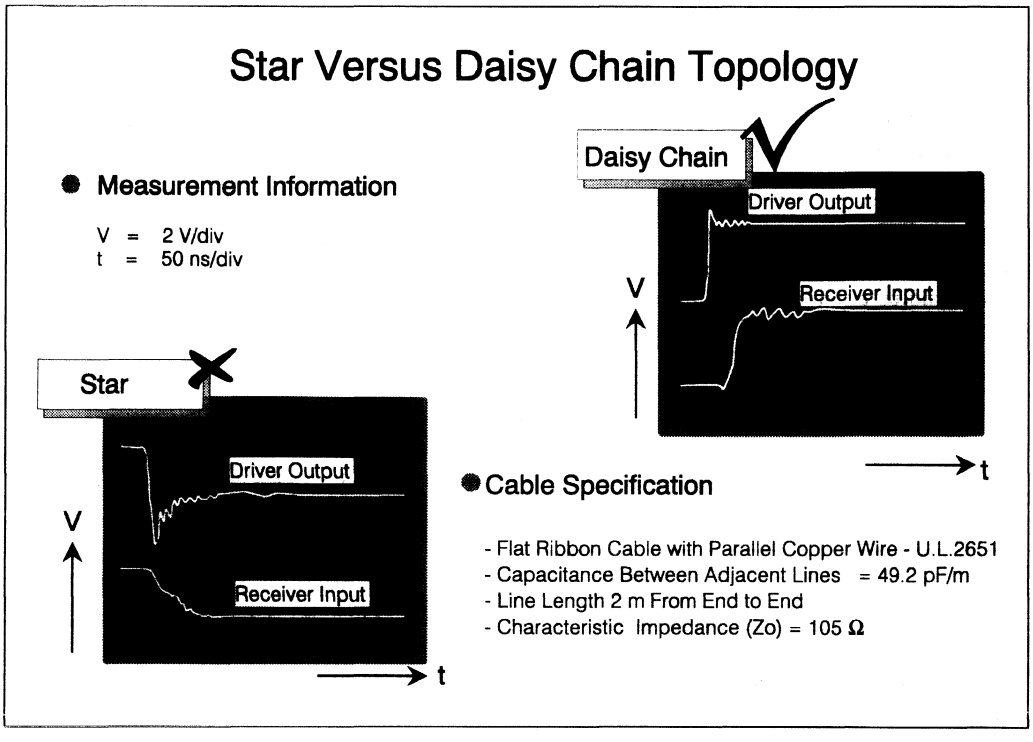


Figure 4.11 - Star Versus Daisy Chain Topology

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

The figure 4.11 shown further confirms the need to keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

1.7.1. How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, t_{pd} ,is more than 5 times the transition times of the driver, t_T. The converse is true if

the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given below.

The rule of thumb states that the transition time of the pulse sent down the line should take ten times the time taken for the pulse to propagate to the end of the stub. As a result, any reflections will be incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, **U**, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used. The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, $\mathbf{L_S}$, as;

$$\mathbf{L_S} = \frac{\mathbf{t_{tD}}}{10}$$

Using the SN75ALS180 and its transition time of 13 ns, a cable with a characteristic impedance of 78Ω and line capacitance of 65pF,:

Using: $Z_O = \sqrt{\frac{L_O}{C_O}}$, as an approximation of the equation shown in section 1.3.1. (In practical situations **jωL>>R** and **jωC>>G**, therefore **R** and **G** can be assumed to be negligible although the **R** component must be considered for long line lengths.)

And: $\mathbf{V_P} = \frac{1}{\sqrt{\mathbf{L_O x C_O}}}$ as an approximation of the phase velocity equation in 1.3.1,

Substitution gives: $\mathbf{V_P} = \frac{1}{\mathbf{Z_O x C_O}}$

Using the values given earlier: $\mathbf{V_P} = \frac{1}{78\mathbf{x}65\mathbf{x}10^{-12}} = 198\mathbf{x}10^{6}\,\mathbf{ms}^{-1}$

Now, using our rule of thumb described earlier: $\mathbf{t_{pd}} = \frac{\mathbf{t_{tD}}}{10}$ and $\mathbf{L_S} = \mathbf{t_{pd}} \mathbf{x} \mathbf{V_P}$

Gives $\mathbf{t_{pd}} = \frac{13\mathbf{x}10^{-9}}{10}$ and therefore $\mathbf{L_S} = 1.3\mathbf{x}10^{-9}\mathbf{x}198\mathbf{x}10^{6} = 257\mathbf{mm} = 10\mathbf{inches}$

This means the length of each stub should be no more than 257 mm. Under this length the stub can be considered as a lumped load and will not cause any unwanted reflections. The main effect of each stub in this case will be a slight increase in the capacitance loading of the line.

2. Interface Circuits for EIA-232

2.1. General Information

This section on EIA/TIA-232, or RS-232 as it has been known in the past, will discuss the electrical aspects of the standard, i.e. the physical layer. Initially we will discuss the latest developments of the 'E' revision upgrade and then cover TI's latest products conforming to this standard. However the reader should note the products under discussion in this section are application specific to the 9-pin DB9 Personal Computer DTE serial interface which is effectively a sub-set of the full EIA-232 standard. As a semiconductor manufacturer we find the majority of EIA-232 applications are moving to this interface. Due to the nature of the signals i.e. 5 receive and 3 transmit lines the older established EIA-232 products no longer provide an optimum solution. This interface is now driving the need for single chip EIA-232 solutions. Additional features such as single supply operation, increased ESD protection, power down modes have moved from the desirable features to the essential features of today's interface. In the later half of this section we will discuss the DB9 interface and TI's products designed specifically for this application.

Looking at the DB9 interface one step back into the digital system, there is in most cases a UART or ACE (asynchronous communication element). The ACE provides the parallel to serial conversion and the necessary start/stop bits, parity bit generation and checking for error free data transmission. TI manufactures a number of ACEs, the most advanced being the TL16C552. This integrates two serial ports with FIFO buffers together with a PC parallel port. Although not specifically covered in this section a selection guide on ACEs is included towards the rear of this section.

2.1.1. Reliability Data

System designers have long been aware the mean-time-between-failure (MTBF) for most systems is limited by the reliability of the line interface circuitry. This is mainly due to the shear power dissipation of such line circuits. The older devices such as the SN75188 quad driver ran at quite high temperatures with obvious degradation on reliability. For today's products the use of low power bipolar and more recently BiCMOS technologies significantly reduces operating temperatures while maintaining the robustness associated with bipolar designs providing for a more reliable interface. This is show by reliability data collected on TI's products.

Life test data collected on a range of EIA-232 devices yielded a failure rate of 1.65 FITS (failures per 10^9 device hours). This was at an ambient temperature of 55°C (to an upper confidence level of 60% and assumes an activation energy of 0.96 eV).

2.2. EIA/TIA-232-E Industry Standard for Data Transmission

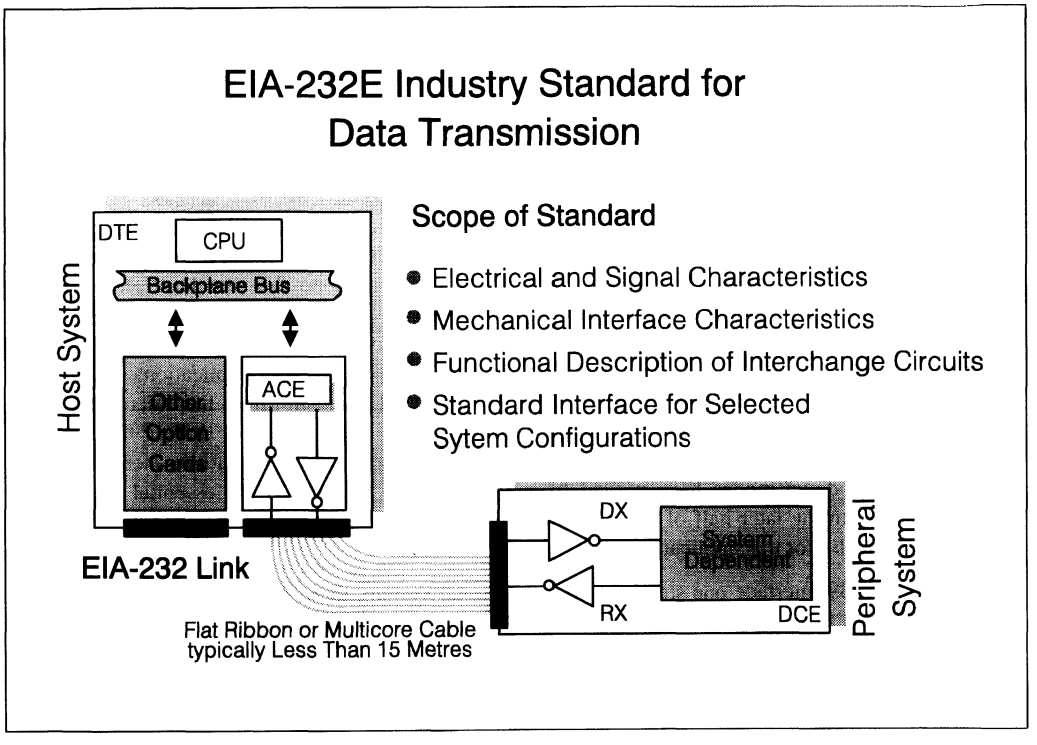


Figure 4.12 - EIA-232-E Industry Standard for Data Transmission

The Electronic Industries Association (EIA) introduced the RS-232 standard in 1962 in an attempt to standardise the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). The DTE comprises the data source, data sink or both. The DCE provides the functions to establish, maintain and terminate a connection, and to code/decode the signals between the DTE and the data channel. Although emphasis was then placed on interfacing between a modem unit and data terminal equipment, other applications were quick to adopt the EIA-232 standard. The growing use of the PC (personal computer) quickly ensured that EIA-232 became the industry standard for all low-cost serial interfaces between the DTE and peripheral. The mouse, plotter, printer, scanner, digitiser, and tracker-ball, in addition to the external modem unit, are all examples of peripherals that

connect to an EIA-232 port. Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

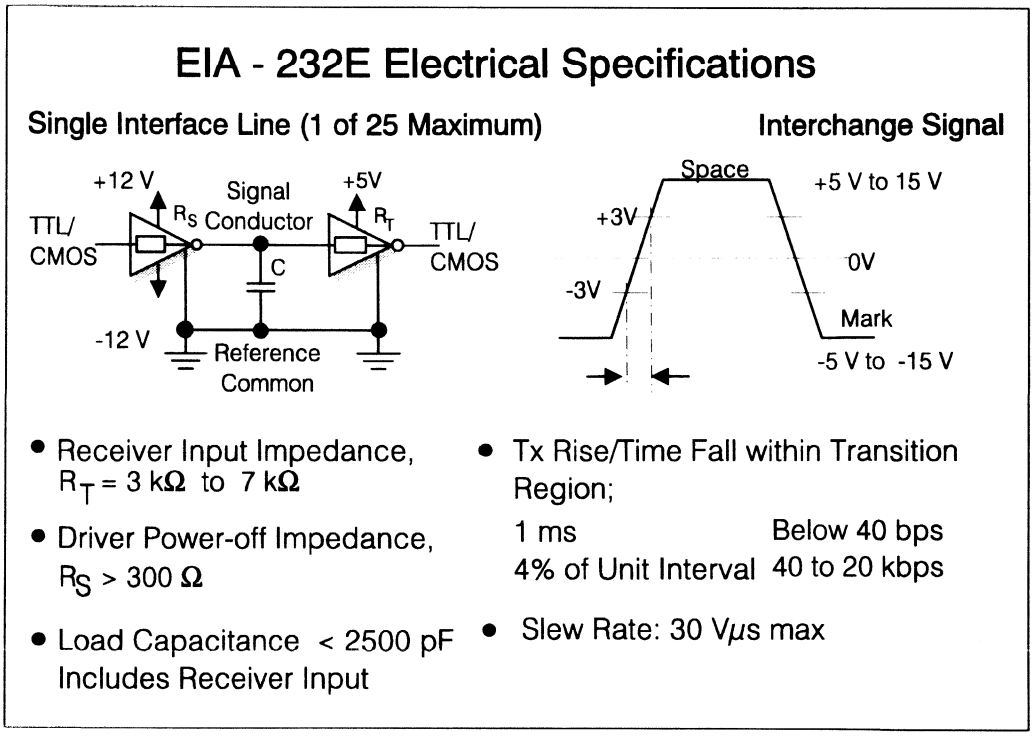


Figure 4.13 - EIA-232-E Electrical Specifications

The EIA RS-232-C standard, revised in 1969, was superseded by EIA-232-D (1986), and recently has been once again superseded by EIA/TIA-232-E which brings it in-line with CCITT V24, V.28 and ISO IS2110. (TIA refers to the Telecommunication Industry Association). The latest revision includes an update on the rise time to unit interval ratio and reverses the changes made by the 'D' revision, see figure 4.14. Although an older standard, with problems like high-noise susceptibility, low data rates and very limited transmission length, EIA-232 fulfils a vital need as a low cost communication system. Consequently new products are being developed at a faster rate than ever.

2.3. EIA-232 Specification

The standard sets out to ensure:

i. Compatible voltage and signal levels

ii. Common pin wiring configurations

iii. A minimum amount of control information between the DTE and DCE.

It accomplishes this by incorporating the following areas in the standard:

Electrical and Signal Characteristics

Electrical and signal characteristics of the transmitted data in terms of signal voltage levels, impedance's, and rates of change.

Mechanical Interface Characteristics

Mechanical interface characteristics defined as a 25-way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25-pin D-type connector, most laptop and desktop PCs, today use a 9-pin "DB9S" connector shown in figure 4.17. The reader should note the DCE equipment connector is male for the connector housing and female for the connection pins. Like wise the DTE connector is a female housing with male connection pins.

Handshake Information

A functional description of the interchange circuit enables a fully interlocked handshake exchange of data between equipment's at opposite ends of the communication channel. However, V24 defines many more signal functions than RS-232, but those that are common are compatible. Twenty two of the twenty five connector pins have designated functions, although few, if any, practical implementations use all of them. The most commonly used signals are also shown in figure 4.17.

It is worth noting that for applications which use the 25-pin D-type connector there is often a problem in communication due to different handshaking signals employed by each system.

2.3.1. EIA-232-E Electrical Specifications

All EIA-232 circuits carry bipolar voltage signals with the voltage at the connector pins not to exceed ±25 V. Any pin must be able to withstand short circuit to any other pin without sustaining permanent damage. Each line should have a minimum load of 3 kΩ and maximum load of 7 kΩ which is usually part of the receiver circuit. A logic '0' is represent by a driven voltage of between +5 V and +15 V and a logic '1' of between -5 V and -15 V. At the receiving end a voltage of between +3 V and +15 V represents a '0' and a voltage of between -3 V and -15 V represents a '1'. Voltages between ±3 V are undefined and lie in the transition region. This effectively gives a 2 volt minimum noise margin at the receiver.

The maximum cable length was originally defined in RS-232C as 15 metres, however this has been revised in EIA-232-D and EIA/TIA-232-E and is now more correctly specified as a maximum capacitive load of 2500 pF. This equates to around 15 to 20 metres line length depending on cable capacitance.

As mentioned in an earlier section, EIA-232 specifies a maximum slew rate of the signal at the output of the driver to be 30 V/μs. This limitation is concerned with the problem of cross talk between conductors in a multiconductor cable. The faster the transition edge the greater the cross talk. This restriction together with the fact of the driver and receiver using a common signal ground and the associated noise introduced by the ground current severely limits the maximum data throughput.

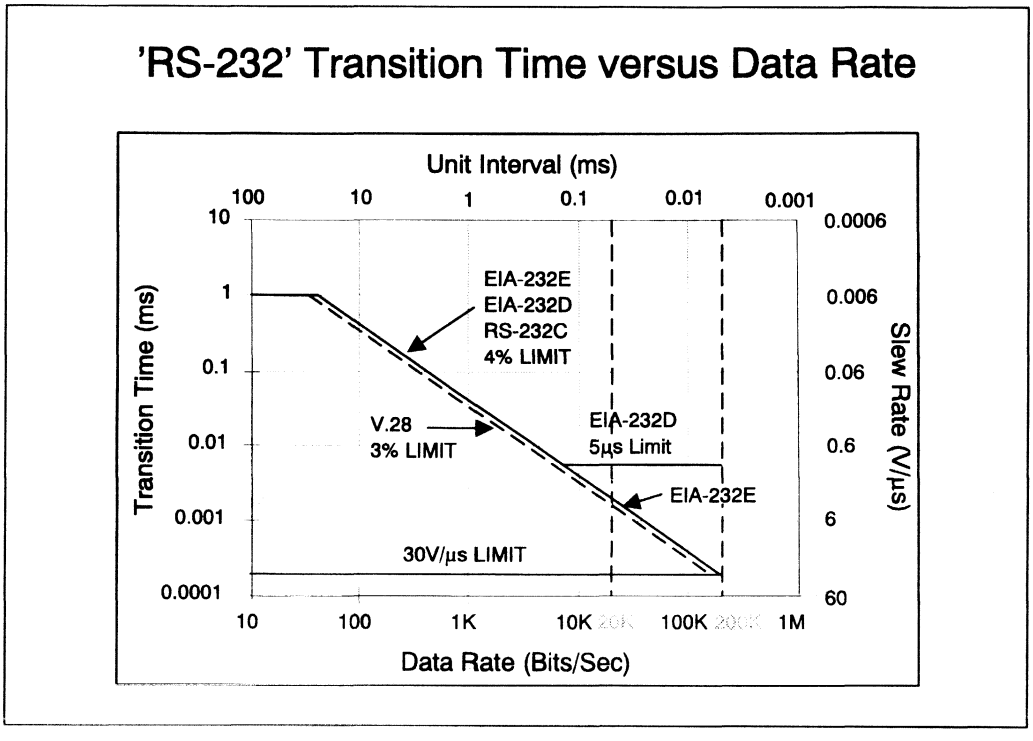


Figure 4.14 - 'RS-232' Transition Time versus Data Rate

For this reason the EIA-232 standard specifies a maximum data rate of 20 kbps. The standard also specifies the relationship between unit interval and rise time through the transition region (+3 V to -3 V) or t_T. This is the main difference between the 'E' and the 'D' revision. This is shown more clearly in figure 4.14. EIA-232-D up to 8 kbps specified the relationship between transition time and unit interval or bit time t_b to be 4% maximum. Above 8 kbps this was relaxed to 5 µs maximum independent of the data rate. Both the 'C' and the 'E' revision specify the ratio of t_T/t_b to be 4% all the way up to 20 kbps. One can extrapolate this further, using the 4% figure and with the maximum slew rate of 30 V/µs, the maximum achievable data rate is 200 kbps however practically this is limited to around 120 kbps. A number of software programs operate at transfer rates of 116 kbps. Furthermore over longer line lengths the maximum drive current or short circuit current of the line driver becomes the dominant feature on data rate as against the 30 V/µs slew rate. As the line length increases the load capacitance also increases requiring more current to maintain the same transition time. The curves shown in figure 4.15 indicate the drive current required to maintain the 4% relationship at different data rates. In today's low power systems, this level of output current is not sustainable at above say 20 kbps. In practice the line length is usually limited to around 4 metres for the higher data rates. Most drivers can handle the higher transmission rates over this line length without seriously compromising supply current.

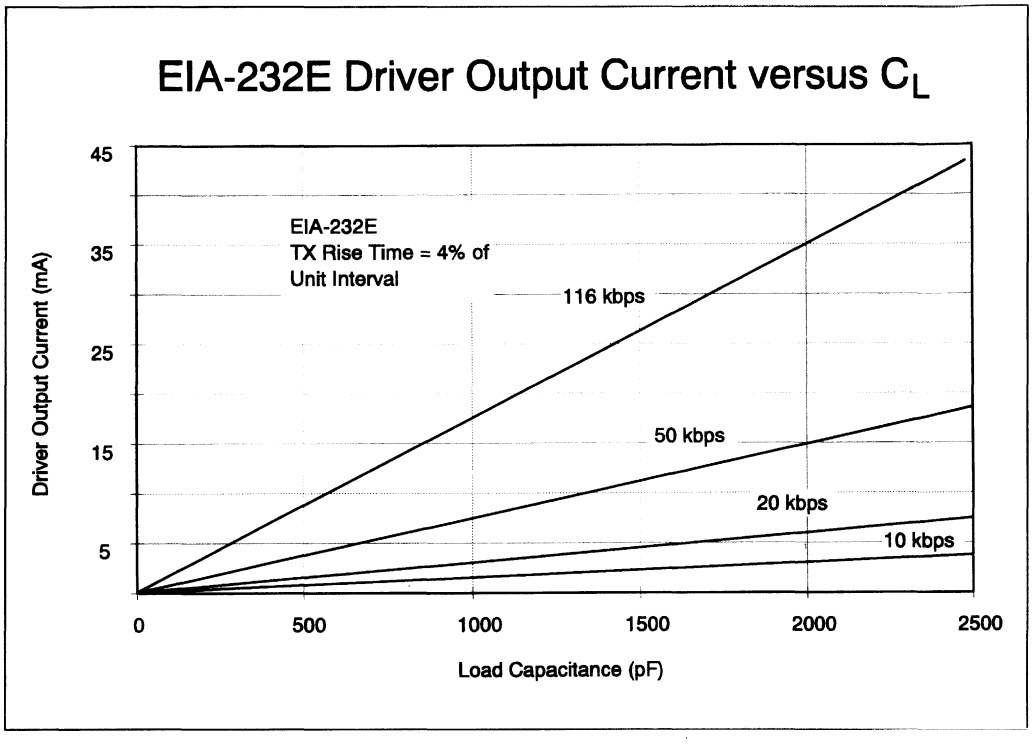


Figure 4.15 - EIA-232-EDriver Output Current versus C_L

The curves shown in figure 4.15 were generated using the following equation which is an approximate equation relating transition time t_T, line capacitance C_l, receiver input impedance R_i, driver short circuit current I_o, and the initial and final line voltage (-3 V and +3 V) of the transition region, V_i and V_f respectively,

$$t_T = R_i \times C_l \times \ln\left[\frac{|R_i \times I_o| + |V_f|}{|R_i \times I_o| - |V_i|}\right]$$

Turning this equation around with respect to C_l, and cancelling R_i, V_i and V_f we get:

$$C_l = \frac{1}{3} \times \frac{t_T}{\ln\left[\frac{I_o + 1}{I_o - 1}\right]} \text{ nF}$$

The voltage levels, V_f and V_i, used in this equation are the extremes of the transition region. Assuming a typical driver short circuit current of 20 mA and a receiver input resistance of 5 kΩ, the typical time taken to pass through the transition region would be :-

$$t_T = 300 \times C_l \quad \text{seconds.}$$

This equation can be manipulated further to gain a relationship of unit interval with line length in terms of load capacitance and short circuit driver current. The equation in figure 4.16 assumes conformance to the 4% rule.

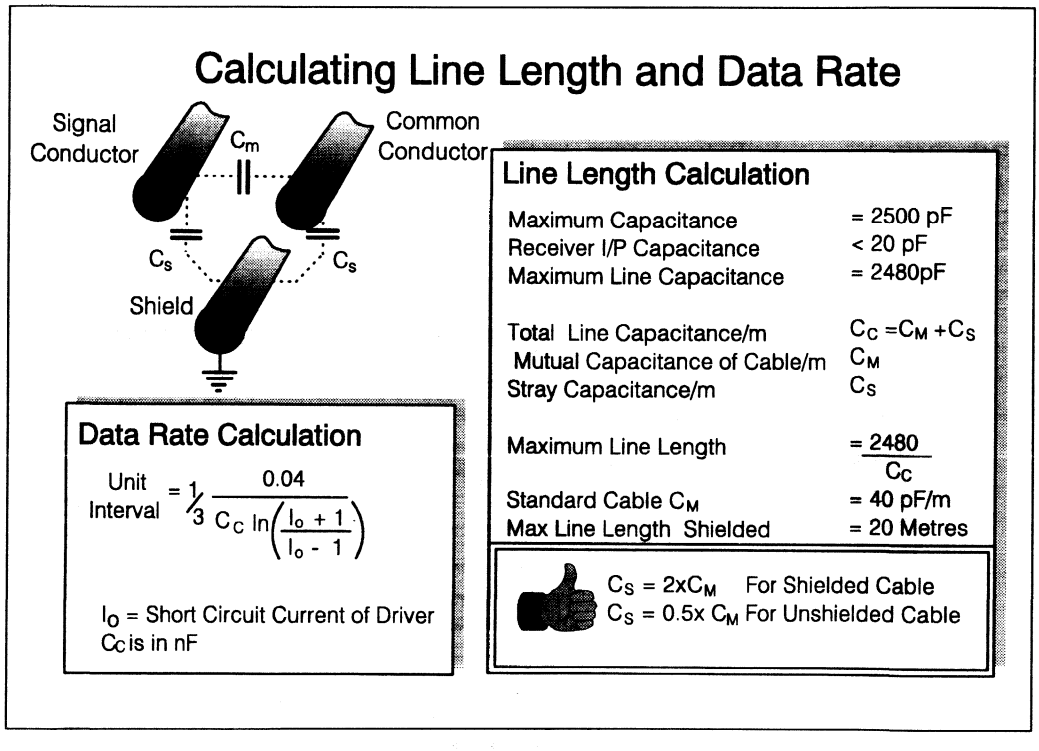


Figure 4.16 - Calculating Line Length and Data Rate

2.3.2. Calculating maximum line length

So far we have discussed line length in terms of load capacitance. For practical purposes we must now consider turning this value for load capacitance into true line length. The standard states a maximum line capacitance of 2500 pF. The input capacitance of a receiver is say 20 pF which leaves 2480 pF as the maximum line capacitance.

We must now consider the type of cable to be used. Standard EIA-232 cable as supplied by a number of manufacturers has a mutual capacitance of approximately 40 pF per metre. In addition to this we must add the stray capacitance. Stray capacitance varies considerably on whether the line is shielded.

For non shielded cable the stray capacitance is approximately half the mutual capacitance, for shielded cable it is double the mutual capacitance. As can be seen from figure 4.16, for shielded cable the maximum line length is 20 metres, with unshielded cable it is over 40 metres.

2.3.3. The DB9S Connector

As mentioned earlier today's notebook and laptop PCs, with their quest for reduced size, no longer use the standard 25-way D-type connector detailed in the standard but have substituted it for a 9-way D-type. This is commonly known as the DB9S connector. Like the 25-way, the DCE equipment connector is a male outer casing with female connection pins, and the DTE is a female outer casing with male connecting pins.

As the interface is now made up of only nine pins the handshaking lines have been reduced accordingly but still are sufficient for most applications. Figure 4.17 shows the pins assignments for the interconnect cable into the DTE connector. An explanation of the function of each signal is given below:

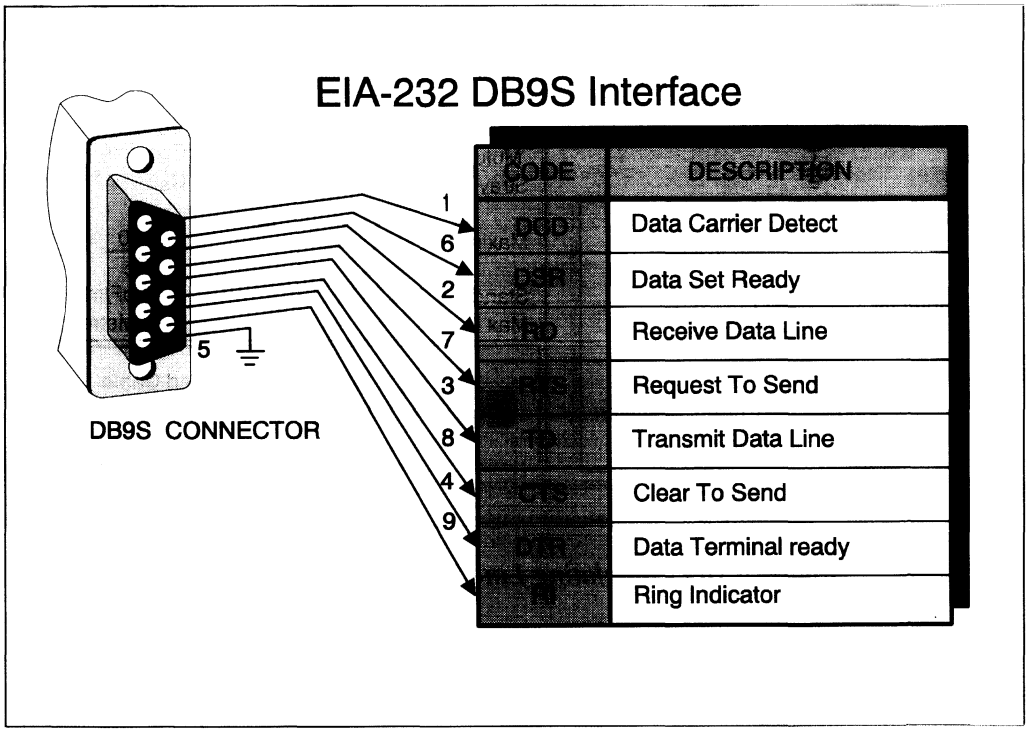


Figure 4.17 - EIA-232 DB9S Interface

Data Carrier Detect (DCD) - Received Line Signal Detector

The ON condition on this signal line as sent by the DCE informs the DTE that it is receiving a carrier signal which meets its suitability criteria from the remote DCE. In modems, this circuit is held on as long as it is receiving a signal that can be recognised as a carrier. On half duplex channels, DCD is held off when RTS is in the on condition.

Data Set Ready (DSR)

This is a signal turned on by the DCE to indicate to the DTE that it is connected to the line.

Receive Data Line (RD)

The signals on the RD line are in serial form . When the DCD signal is in the off condition the RD line must be held in the Mark state.

Request to Send (RTS)

This signal is turned on by the DTE to indicate it is now ready to transmit data. The DCE must then prepare to receive data. In half duplex operation, it also inhibits the receive mode. After some delay the DCE will turn the CTS line on to inform the DTE it is ready to receive data. Once communication is over and no more data is transmitted by the DTE, RTS is then turned from on to off by the DTE. After a brief time delay to ensure all data has been received that was transmitted, the DCE turns CTS off.

Transmit Data Line (TD)

The signals on this circuit are transmitted serially from DTE to DCE. When no data is being transmitted the signal line is held in the Mark state. For data to be transmitted, DSR, DTR, RTS and CTS must all be in the on state.

Clear to Send (CTS)

This signal is turned on by the DCE to indicate to the DTE that it is ready to receive data. CTS is turned on in response to simultaneous on condition of the RTS, DSR and DTR signals.

Data terminal Ready (DTR)

This in conjunction with DSR indicate equipment readiness. DTR is turned on by the DTE to indicate to the DCE it is ready to receive or transmit data. DTE must be in the on condition before the DCE can turn on DSR. When DTR is turned off by the DTE, the DCE is removed from the communication channel following the completion of transmission.

Ring Indicator (RI)

The ring indicator is turned on by the DCE while ringing is being received and is a term left over from the use of the standard in telephone line modem applications. Primarily used in auto-answer systems.

Signal Ground (pin 5)

This is the ground which provides the common ground reference for all the interchange circuits and is separate from the protective ground. The protective ground is electrically bonded to the equipment frame and is usually directly connected to the external ground. Any static discharges are then routed directly to ground without affecting the signal lines.

While all these pins are assigned, once again not all equipment uses every pin. Consider the mouse which can use as few as 4 lines, Signal ground, RI, TD and RD. Most equipment does however utilise a minimum of RTS, DTR, TD, RD, CTS and DSR.

Also of note is the usage of the DTE interface. The majority of equipment uses this interface and makes use of the null modem as a means of communication between DTEs. The null modem makes use of feeding back the RTS signal to the CTS line on each interface, Figure 4.17.1 details the connections for implementing a full null modem for the DB9S connector.

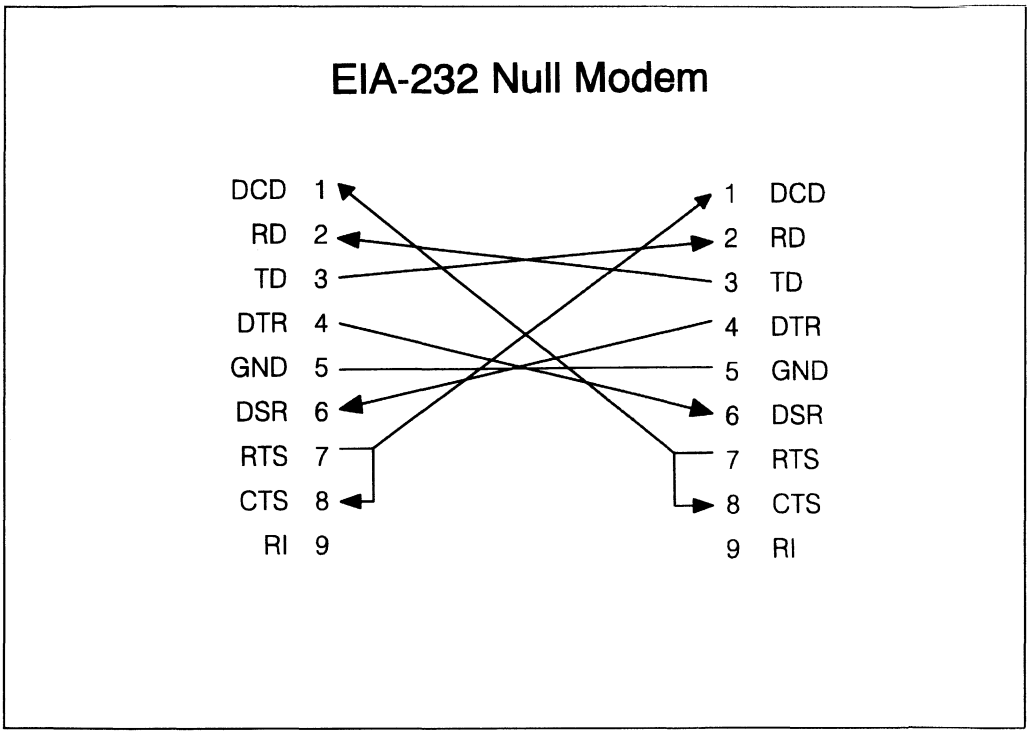


Figure 4.17.1 - EIA-232 Null Modem

2.4.SN75C185: Optimised PC Interface

If we study the DB9S DTE interface further we see there are 3 transmit lines and 5 receive lines. This is an awkward combination for the standard EIA-232 IC configurations in use today. Consider the ubiquitous SN75188 and SN75189 quad drivers and receivers. To implement this interface would require 3 ICs, one '188 and two '189s. Equal combinations of drivers such as the triple driver/receiver of the SN75C1406 still requires two chips to implement the interface.

For this reason TI has developed the SN75C185. By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be provided – the SN75C185 is just that. The SN75C185 integrates three drivers and five receivers and

includes the necessary capacitors for driver slew-rate limit (30 V/μs) and receiver filter implementation, all in a single 20-pin package

The designer's dilemma is eased further by the use of a flow-through pin out architecture, see figure 4.18. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs or UARTs, printed circuit board (PCB) layout can be greatly simplified.

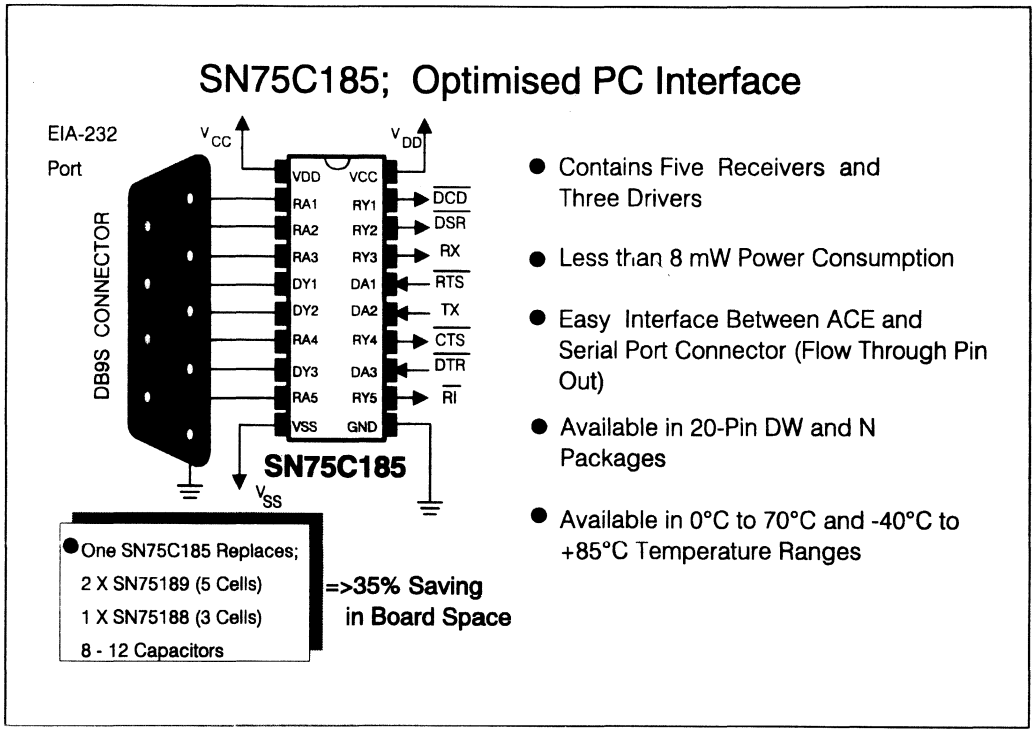


Figure 4.18 - SN75C185; Optimised PC Interface

2.4.1. Low Power as Well

In common with all of Texas Instruments BiMOS products, these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving, when compared to the alternatives is calculated in the following pages and is illustrated graphically in figure 4.19.

Available in either a single 20-pin, wide-bodied SO pack or DIP pack, the SN75C185 offers designers greater than 25% saving in board space, compared to alternate solutions.

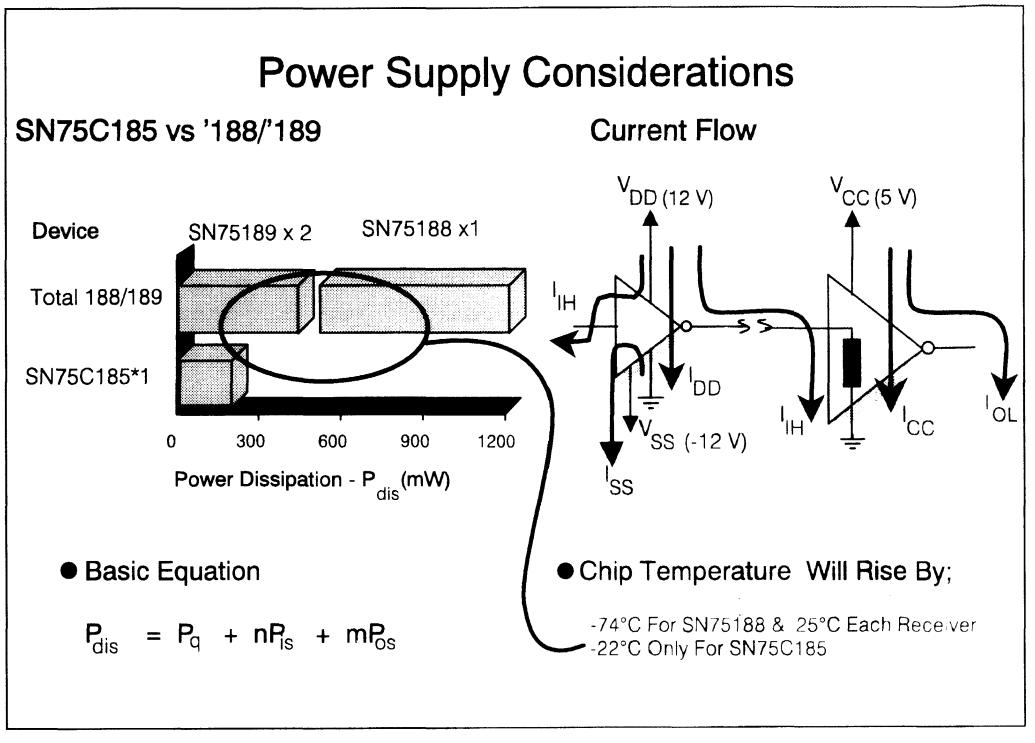


Figure 4.19 - Power Supply Considerations

2.4.2. SN75C185; Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially when using devices in confined spaces. These areas will normally have very poor air circulation, causing the ambient temperature of the whole system to increase.

These types of problems are particularly difficult to diagnose as failure can often be intermittent as devices pass into and out of thermal shutdown.

For these reasons, low quiescent-power devices are becoming a necessity for modern applications. As digital technologies advance, their power consumption decreases, making the interface circuits the limiting factor as far as system power consumption is concerned.

2.4.3. Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad-driver package and two quad-receiver packages; in the driver chip, one device is redundant while in the

receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations below demonstrate this difference.

When comparing the 'C185 solution to that provided by the SN75188 and SN75189 devices, the power saving is enormous.

Both implementations require three supply voltages; a 5 V and ±12 V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576 mW. In addition to this the power dissipated in the input stage, P_{isd}:-

$$P_{isd} = V_{CC} * I_{IL}$$

$$= 12 * 1.6 \text{ mW}$$

$$= 19.2 \text{ mW}.$$

This is multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{osd}, is:

$$P_{osd} = (V_{CC} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 9) * \frac{9}{3} \text{ mW}$$

$$= 9 \text{ mW}.$$

This figure will be multiplied by three to take into account the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$P_{dis} = 576 + 4 \times 19.2 + 3 \times 9 \text{ mW}$$

$$= 680 \text{ mW}.$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver.

$$P_{osr} = V_{OL} * I_{OL}$$
$$= 0.45 \times 10 \text{ mW}$$
$$= 4.5 \text{ mW}$$

This power dissipated is multiplied by five to take into account the five receivers being used. The input stage can also dissipate some power, but this power is not supplied by this part of the interface system. The power dissipated within the IC will however cause the junction temperature to rise.

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$
$$= \frac{9^2}{3} \text{ mW}$$
$$= 27 \text{ mW}$$

This power dissipation is then multiplied by five. The remaining receivers will require tying to a state where they will not be susceptible to noise. Tying them to the 5 V supply increases the power dissipation by a further 8.3 mW per receiver.

Assuming three receivers in one SN75189 are being used and two receivers in the other, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 4 \times 27 + 3 \times 4.5 \text{ mW}$$
$$= 233 \text{ mW}.$$

The power dissipated in the second receiver is:-

$$P_{dis} = 130 + 4 \times 27 + 2 \times 4.5 \text{ mW}$$
$$= 210 \text{ mW}.$$

This raises the temperature of the first and second receiver by 25°C and 23°C, respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling **1.12 W.**

Using the SN75C185

The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent- power consumption of the SN75C185 is equal to:-

$$P_q = V_{DD} * I_{DD} + V_{SS} * I_{SS} + V_{CC} \times I_{CC}$$
$$= 12 * 200 + -12 \times -200 + 5 \times 750 \quad \mu W$$
$$= 8.55 \text{ mW}$$

The power dissipated in the input stage of the driver is:-

$$P_{isd} = V_{DD} \times I_{IL}$$
$$= 12 \times 1 \ \mu W$$
$$= 12 \ \mu W.$$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output stage of the driver, P_{osd}, is:

$$P_{osd} = (V_{DD} - V_{OH}) \times \frac{V_{OH}}{R_L}$$

$$= (12 - 10) \times \frac{10}{3} \text{ mW}$$

$$= 6.67 \text{ mW}.$$

This is multiplied by three to take into account the three drivers driving the interface line, giving a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:

$$\text{Posr} = V_{OL} \times I_{OL}$$

$$= 0.4 \times 3.2 \text{ mW}$$

$$= 1.28 \text{ mW}$$

This value is multiplied by five giving a total of 6.4 mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

The power dissipated in the input stage, P_{isr}, equals:

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{10^2}{3} \text{ mW}$$

$$= 33.3 \text{ mW}$$

This power dissipation will also require multiplying by five. Giving a total input power dissipation of 167 mW.

Summing all the power contributors the total power dissipation is given by;

$$P_{dis} = P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr}$$

$$= 8.55 + 3 \times 12 \times 10\text{-}3 + 3 \times 6.67 + 5 \times 33.3 + 5 \times 1.28 \text{ mW}$$

$$= 201 \text{ mW}.$$

The total power dissipated by the SN75C185 is **201 mW**

This is represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.

2.4.4. On Chip Slew Rate Limiting

The EIA-232-E standard specifies a maximum slew rate through the transition region of **30 V/μs**. Relating this to capacitance and current only 100 μA of output current into 30 pF load capacitance is needed to exceed the slew-rate limit. All devices are capable of supplying more than 5 mA. Therefore if the slew rate limit is not to be exceeded, the switching speed of the driver's output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of the loading capacitor required will depend upon the line length, but it is generally in the order of 330 pF. The effect of this capacitor is to cause the output transistors to saturate, causing it to short circuit current limit, thus preventing fast switching edges.

There are some major problems with this established process; one being the variance in current at which the output short-circuit current limit operates, especially when taking temperature changes into consideration. Again the value of capacitance placed on the line will depend upon the driver's output short-circuit capability as well as line length. For example a device capable of sourcing 10 mA will need a total capacitance of 330 pF placed on its output to meet the 30 V/μs slew rate limit, while placing this value across a device capable of sourcing 4 mA will have its slew rate limited to less than 12 V/μs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver will normally be close to one supply rail, so when it tries to switch to the other, the active transistor will have almost all of the supply voltages across it. The extra external capacitor will clamp the driver's voltage close to the supply voltage causing the output transistor to source large amounts of current. The combination of a large source current and large voltage cause it to dissipate large amounts of power. Operating at these prolonged bursts of high current will ultimately increase the chip temperature which in turn can affect the long-term life of the device. Bipolar technologies are normally much better able to withstand such effects

A better solution, and that employed by the drivers in the SN75C185, is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew-rate-limited operational amplifiers, the slew rate of line drivers can also be limited. Using the Miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The on-chip capacitors are normally in the order of 5 pF, while the currents driving the on-chip capacitor are the order of micro amperes, thus reducing power consumption within the device. The biasing current to the output transistors is unaffected by this technique and will be more than sufficient to drive the 3 kΩ load as offered by the receiver.

2.4.5. Internal Noise Filtering

The standard states a maximum line cable capacitance of 2500 pF, which corresponds to an approximate line length of 20 metres. As the interface line gets longer, it becomes more susceptible to noise pick-up from the surrounding environment. This pick-up is due in part to the inductive nature of the line. As the signal switches, a rapidly changing magnetic field induces noise currents into the line, thereby corrupting signal data. The level and cause of this noise will dictate the nature of solutions or precautions that should be taken.

For operation at high data rates, the use of a differential line might be the best solution. If however, a low cost and simple single-ended solution is required then standard EIA-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input stage,

making them too slow to respond to fast switching noise pulses. Even small levels of input noise can falsely trigger the receiver. The maximum data rate specified in the standard is 20 kbps, corresponding to a minimum pulse period of 100 µs. Therefore in normal applications, most devices are far faster than the specification requires.

To slow down older bipolar receivers such as SN75189s, a capacitor, C_C, needed to be placed on each of its response control pins. This means an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low-pass filter on the receiver's input. In order to provide large pulse rejection, the capacitor needs to be quite large. Furthermore, the filter response is asymmetric, affording protection against positive noise voltage spikes only, negative spikes are unaffected, and will tend to attenuate rather than reject short noise pulses.

Receivers in the SN75C185 integrate on-chip filtering which reject fast transient noise pulses. The on-chip filters are more precise than filters implemented using external passives. Consequently the receiver response is unaffected. These filters are totally symmetrical, offering protection against both positive and negative noise pulses and with the ability to reject rather than attenuate short noise pulses. To approach the level of filtering offered by the 'C185 receivers the standard '188 type receivers require much larger capacitors and even then fall well short of filtering requirements.

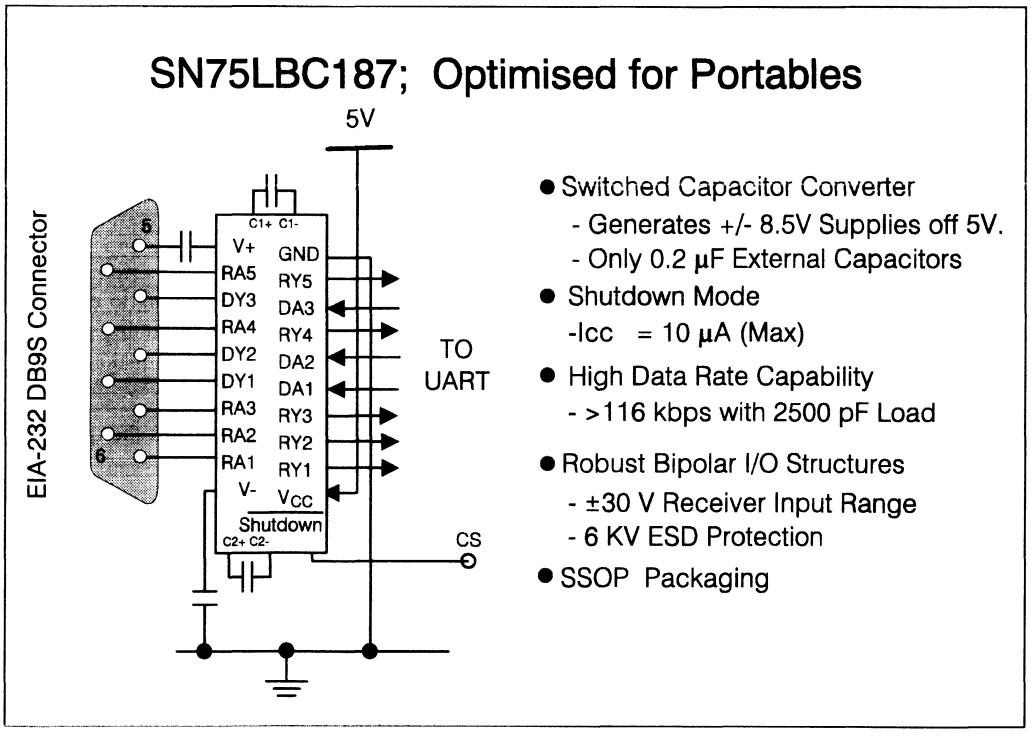


Figure 4.20 - SN75LBC187; Optimised for portables

2.4.6. SN75LBC187; Optimised for Portables

The SN75C185 is the ideal choice for computer applications where the bipolar supplies required by EIA-232 are available within a computer system. Most desk top computers generate ±12 volt supplies for powering the internal disk drive. However for portable equipment, e.g. laptops, notebooks, hand held measuring equipment, the EIA-232 interface may be the sole user of a negative supply. The cost of implementing a switch mode supply, using inductive switching regulators, to generate the negative supply can make this option unattractive. Switch mode supplies also have the draw back of increasing the EMI emissions, a factor becoming an increasingly important design constraint. Integrating a switch mode power supply on silicon would reduce the emissions, and has been the dream of semiconductor manufacturers, but thus far no one has yet managed to integrate the inductor.

An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is transferred into a holding reservoir capacitor that is then used to supply the output voltages. Furthermore such a scheme can be integrated into silicon. Using a network of capacitors both voltage doublers and invertors can be made.

The SN75LBC187 integrates the charge pump on the same IC as the EIA-232 drivers and receivers. It is fabricated in TI's proprietary LinBiCMOS technology and contains three independent drivers and 5 independent receivers together with the switched-capacitor voltage converter. The SN75LBC187 provides a single 5 V supply interface between the asynchronous communications element (ACE or UART) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards EIA/TIA-232-E-1986 and EIA/TIA-562 and CCITT recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small (0.2 µF) external capacitors to generate the positive and negative voltages required by EIA-232 line drivers from a single 5 V logic supply input. Like the SN75C185 the drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without sustaining damage. Furthermore the 'LBC187 is guaranteed to withstand up to 6KV ESD on any of its pins making it TI's most rugged EIA-232 product.

The device also features a reduced power or shutdown mode that virtually eliminates the quiescent power supply when the IC is not active.

The primary application for the 'LBC187 is for battery operated, portable equipment where power consumption is a key factor. A separate consideration, and one that usually goes hand in hand with these factors, is that of shear physical size. With the 'LBC187, TI has used the latest SSOP packaging to reduce board area to an absolute minimum. The new SSOP package reduces board space to 43% of the standard 28-pin SOIC package Couple this with the small 0.2 µF and you have the ideal single supply solution for space restricted applications.

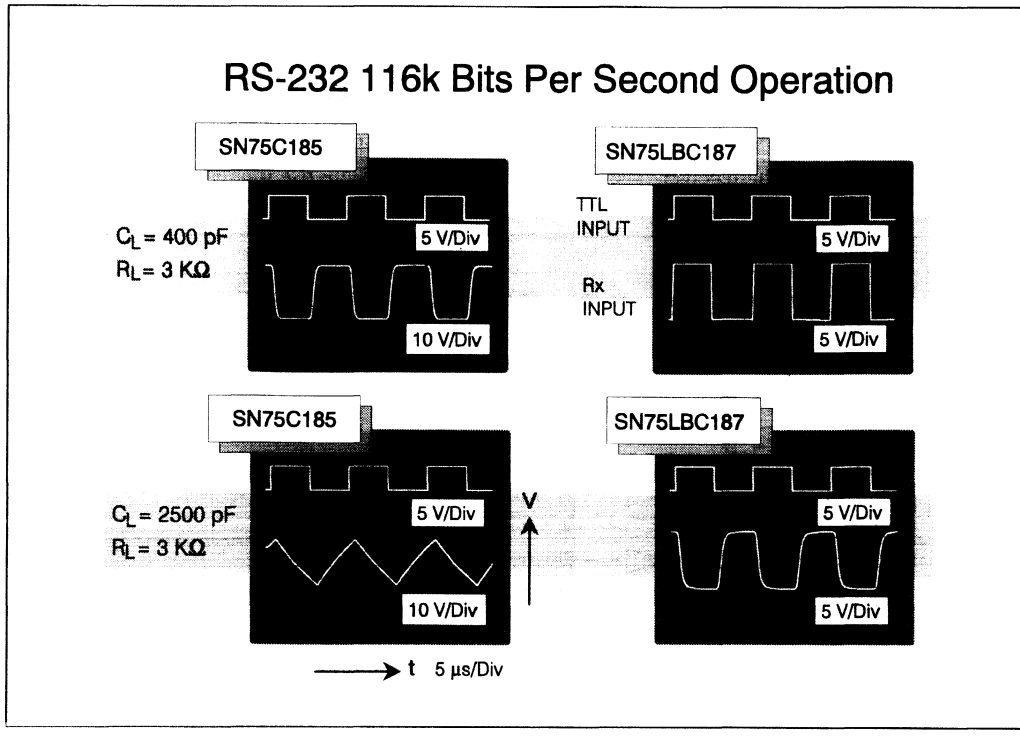


Figure 4.21 - RS-232 116k Bits Per Second Operation

2.4.7. SN75LBC187; 116 kbps operation

As discussed in section 2.3.1 the limitation on data rate is one of short circuit output current and the actual load capacitance. With the 'LBC187 the driver short circuit current, I_{OS}, is higher than say the SN75C185 and is therefore able to drive longer line lengths at higher data rates. Figure 4.21 illustrates this. The 400 pF load in the top half of the figure represents a cable approximately 3 metres long. As the 'scope traces show, the 'C185 produces a perfectly acceptable output trace at 116 kbps. Similarly with the 'LBC187 trace.

If the line length is now upped to 20 metres or 2500 pF load, we can see how the short circuit current limit now limits the slew rate. With the 'LBC187 the trace is still acceptable and will provide reliable data transmission. With the 'C185, the data will still be transmitted but the probability of error is now increased. Most software programs that operate 116 kbps, e.g. Laplink™ (Laplink is a trademark of Travelling Software Inc.) provide the interconnect cable as part of the system. In most cases this cable is less than 3 metres in line length so either the 'C185 or 'LBC187 would be able to transmit data reliably. It is interesting to note that both devices would meet EIA-232-D if the rise time to unit interval relationship was extrapolated, however both would fail EIA-232-E. Of course conformance to EIA-232 is not relevant above 20 kbps.

2.4.8. Conformance to EIA-562

A new standard has recently been introduced in an attempt to provide a low power standard for 5 volt systems and also to increase the data rate over EIA-232. Known as EIA-562, the standard increase the maximum data rate from 20 kbps to 64 kbps and facilitates lower driver voltages. The downside is the reduced noise margin at the receiver. The specification also details the rise time and ripple conditions of the driver. The SN75LBC187 is fully conformant to this standard.

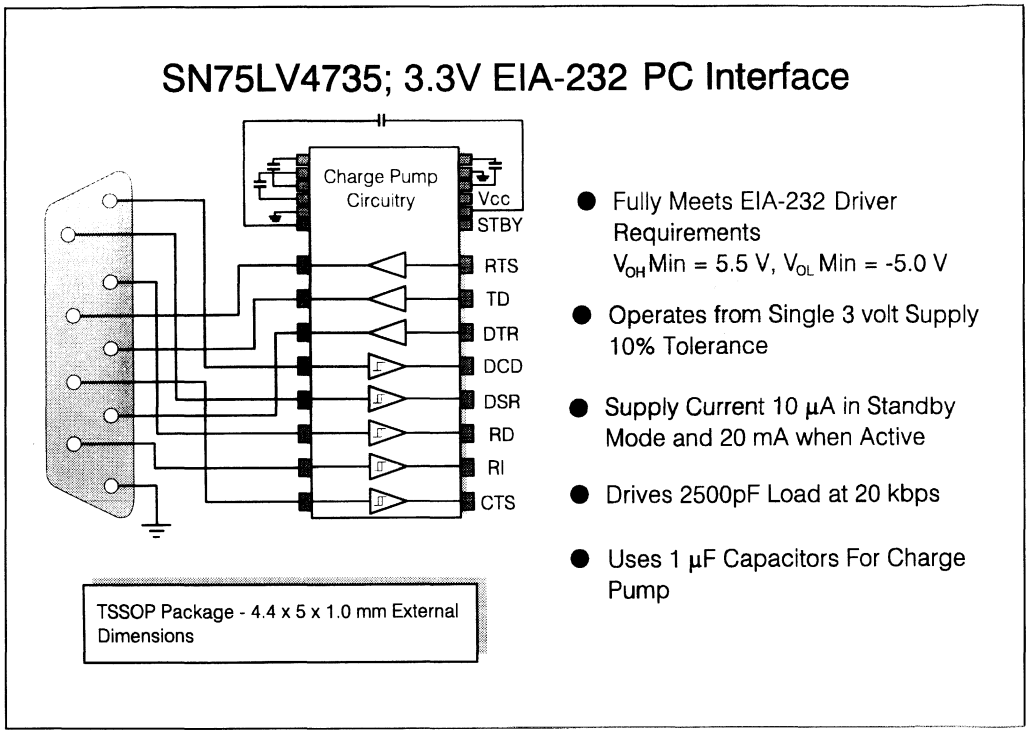


Figure 4.22 - SN75LV4735; 3.3V EIA-232-E PC Interface

2.5.SN75LV4735; 3 Volt EIA-232 PC Interface

Continuing the move to lower power systems the obvious choice is to reduce the supply voltage of the system. Assuming supply current remains constant power dissipation is instantly reduced. The driving force behind this reduction is once again the notebook type PC equipment. To facilitate the move to 3 Volts, TI has introduced the SN75LV4735. From 3 volts the device is still capable of producing the required V_{OH} and V_{OL} for conformance with EIA-232.

Once again the device is designed specifically for the DB9S PC DTE interface containing 3 drivers and 5 receivers for a single package solution.

The device is packaged in the TSSOP package with a board area of only 22 mm^2 and a maximum package height of 1 mm.

2.6. ACEs (UARTs) From Texas Instruments

Most EIA-232 systems use dedicated communication controllers. Termed ACEs (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter), these devices are responsible for controlling the exchange of information over the EIA-232 interface.

The ACE

The ACE is a dedicated asynchronous communications controller designed to off load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add or delete start and stop bits and provide odd/even parity code generation and detection. Industry standard devices such as the **TL16C450** family contain many extra features as listed below:

- **Programmable bps-rate generator**
- **Adds and deletes standard asynchronous communication bit**
- **Fully programmable serial interface characteristics**
- **Data communication diagnostic capability**
- **Modem-control functions**
- **Simple interface to microprocessors**
- **Maximum data rate of 256 k bits per second**

All devices are designed using Texas instruments EPIC™ CMOS process and operate from a single 5 V supply. The **TL16C450** is the most common choice for standard PC applications as well as many other asynchronous serial applications. The TL16C450, housed in a 40-pin package, contains all the necessary facilities for implementing a single asynchronous serial port. The CPU within the system can read and report on the status of the ACE at any point in the ACEs operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered, parity, overrun etc.

The TL16C450 ACE includes a programmable, on-board, bps-rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to $(2^{16} - 1)$ and producing a 16 x clock for dividing the internal transmitter logic. Provisions are included to use this 16 x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimise the computing required to handle the communications link. The **TL16C451** is similar to TL16C450 with the single serial port, but also contains a Centronix parallel printer port. The IBM PC AT/XT sets the standard for this parallel printer interface that all "compatible" manufactures have to follow. TTL-level signals are presented on a 25-pin D-type socket. Apart from the choice of connector, this parallel printer port is directly compatible with the "Centronix" standard printer interface. The **TL16C452** has two serial ports plus a parallel Centronix printer port. Using this ACE together with two SN75C185s provides a simple three chip complete solution for the two EIA-232 ports plus a printer port that is common on basic PC configurations.

EPIC is a trademark of Texas Instruments Incorporated

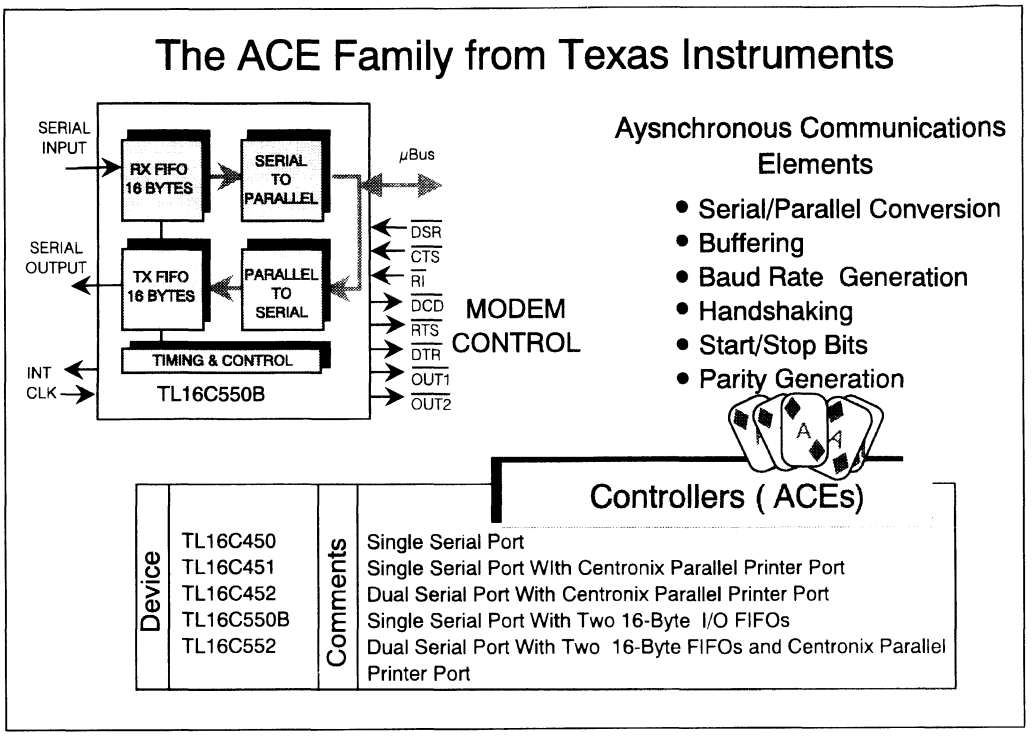


Figure 4.22.1 - The ACE Family from Texas Instruments

2.6.1. The FIFO (First-In-First Out)

The CPU can send data at much faster rates than a normal ACE can handle. This is particularly true for today's multitasking applications that demand high performance microprocessors. This can be expensive in CPU overheads as the CPU will be tied to the speed of the serial interface, i.e., data will be transferred over the interface through the ACE and onto the CPU bus. This is true also when the data is exchanged from the CPU to interface via the ACE.

Devices like the **TL16C550B** and **TL16C552** alleviate this problem by including buffer registers and FIFOs in series with the ACE's transmitter and receiver. These are quick access registers that hold data until the CPU can be freed. The CPU can then execute a block read or write.

The ACE is, in effect, isolated from the slow communications channel.

The TL16C550B is similar to the TL16C450, but two 16-byte FIFOs are included to buffer the transceiver and receiver data stream, further reducing the number of interrupts from the microprocessor.

2.6.2. Forward-Looking Performance With Backward Compatibility

By allowing two modes of operation, the TL16C550B allows users to maintain software compatibility with earlier industry standard ACEs such as the TL16C450. In addition to the TL16C450 mode, the TL16C550B can operate in the FIFO mode. In FIFO mode, two 16-byte FIFOs (First-In-First-Out) are enabled to relieve the CPU of excessive software overheads. The independent receive and transmit FIFOs act as buffers, vastly reducing the number of interrupts required. Furthermore two dedicated pins serve as handshaking lines to a DMA (Direct Memory Access) controller, thus allowing the FIFOs to load and unload data without direct intervention from the CPU.

The flagship of the range is the TL16C552, which is similar to the TL16C452 in structure but with the added advantage of input/output FIFOs as in the TL16C550B

This device serves two serial input/output interfaces simultaneously in either microcomputer or microprocessor-based systems. In addition to its dual asynchronous serial communication capabilities, the TL16C552 provides a fully bi-directional parallel data port that fully supports the parallel Centronix-type printer. The parallel port and the two serial ports provide IBM PC/AT compatible computers with a single low-power device to serve the three-port system. Like the TL16C550B, the TL16C552 contains 16-byte receive and transmit FIFOs that act as buffers to reduce the number of interrupts on the CPU. Also in common with the TL16C550B, the device contains two pins for each ACE that serve as handshaking lines for DMA control. The TL16C552 is housed in a 68-pin plastic-leaded chip carrier, PLCC.

Integration of FIFO and DMA signalling circuitry onto a single chip makes the TL16C550B and TL16C552 one of the most efficient solutions for higher performance multitasking systems.

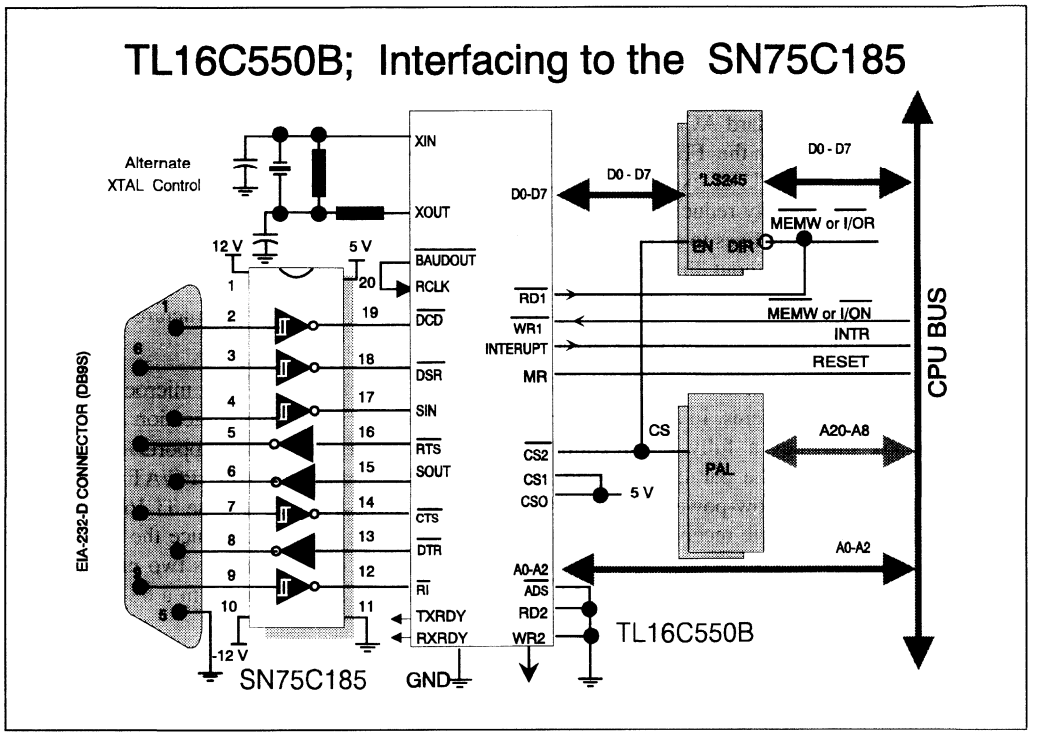


Figure 4.22.2 - TL16C550B; Interfacing to the SN75C185

2.7. Interfacing Between the TL16C550B and the SN75C185

The circuit shown demonstrates the simplicity, in hardware terms, in implementing an asynchronous serial interface with the SN75C185 driver/receiver and the communications controller TL16C550B.

When interfacing between the TL16C550B ACE and the Intel CPU bus, minimal glue logic is required. Namely an 'LS245 Octal bus transceiver is used to provide drive current to an 'off-card' CPU, and programmable array logic (PAL) to decode address lines and generate a chip select signal. While an exhaustive description of this interface is beyond the scope of this section, a discussion of key interface lines can be useful.

Xin/Xout:
External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$,RCLK:

The transmitter reference clock is available externally via the $\overline{\text{baudout}}$ pin. In this application bpsout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock rate is

established by the reference oscillator clock frequency (xin) and divided by a driver specified by the bps generator divisor latches.

$\overline{\text{TXRDY}}$:

Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$:

Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7:
Databus. Eight 3-state data lines provide the bi-directional path for data, control, and status information between the ACE and CPU bus.

$\overline{\text{RD1}}$, RD2:

Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from the selected ACE register. Since only one of these inputs is required for the transfer of data during the read operation, RD2 is tied to its inactive state, i.e., low.

$\overline{\text{DCD}}$, $\overline{\text{DSR}}$, SIN, $\overline{\text{RTS}}$, SOUT, $\overline{\text{CTS}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$:

These signals are the EIA-232 compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between ±5 V to ±15 V. The signal can then be transmitted over distances of up to 15 m.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example, driving/receiving combinations precisely match the interface requirement, plus the pin-out is aligned directly to the DB9S connector.

$\overline{\text{WR1}}$, WR2:

Write inputs. A logic applied to $\overline{\text{WRI}}$, during ACE selection allows the CPU to write either control words or data into a selected ACE registers. WR2 is tied in active, i.e.: logic low.

INTERRUPT:
When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

- **Receiver error**
- **Received data available or time-out (FIFO mode only)**
- **Transmitter holding register empty**
- **Enable modem status interrupt**

The interrupt is reset (deactivated) either when the interrupt has been serviced or by a master reset (MR).

MR:
Master reset. When active (high), MR clears most ACE registers and sets the states of various outputs (i.e. interrupt).

CS0, CS1, $\overline{CS2}$:

Chip Select. An active low on the $\overline{CS2}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{CS2}$ chip select. A logic high on $\overline{CS2}$ will de-select the ACE.

A0 to A2:
Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example, providing the correct write/read operation had taken place at logic 0 at A2, A1, and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{ADS}$:

Address strobe. An active low on $\overline{ADS}$, the register select signals (A0 TO A2) and chip-select signal ($\overline{CS2}$) drive the internal logic directly.

2.8. EIA-232 Products Summary

In this section we have discussed devices which are concerned primarily with the DB9S connector. TI also has a wide range of other EIA-232 ICs which offer differing combinations of drivers and receivers which can offer the optimum solution for your system. The reader is advised to consult the current edition of Interface Circuits Data Book (Reference SLYD006) which contains a complete selection guide of EIA-232 products.

2.9. EIA-232 Selection Guide

Data Transmission Circuits

Function	Per Package	Type	Features
	2	SN75150	Industry Standard
		UA9636AC	Industry Standard
Line Driver	4	LT1030	Robust bipolar design, with 3-state driver outputs
		SN55188	–55°C to 125°C temperature range
		SN75188	Industry standard
		SN65C188	–40°C to 85°C temperature range
		SN75C188	Low-power BiMOS
		SN65C198	–40°C to 85°C temperature range
		SN75C198	Low-power BiMOS with sleep-mode

Line Receiver	4	SN75154	Industry standard
		SN55189	-55°C to 125°C temperature range
		SN75189	Industry standard
		SN55189A	-55°C to 125°C temperature range
		SN75189A	-55°C to 125°C temperature range
		SN65C189	-40°C to 85°C temperature range
		SN65C189A	-40°C to 85°C temperature range
		SN75C189	Low-power BiMOS
		SN75C189A	Low-power BiMOS

Continued Over.....

Data Transmission Circuits (Continued)

Function	Per Package	Type	Features
Line Driver / Receiver	1/1	SN75155	On-chip 5-v regulator
	2/2	MAX232	On-chip charge pump
	2/2	LT1080	On-chip charge pump and 3-state outputs
	2/2	LT1080	On-chip charge pump
	3/3	LT1039	Robust bipolar design, with 3-state outputs
	3/3	SN65C1406	–40°C to 85°C temperature range
	3/3	SN75C1406	Low-power BiMOS
	4/4	SN75186	Robust bipolar design, with loopback
	4/4	SN65C1154	–40°C to 85°C temperature range
	4/4	SN75C1154	Low-power BiMOS
	3/5	SN65C185	–40°C to 85°C temperature range
	3/5	SN75C185	Optimised for DB9S (9-pin) connector
	3/5	SN75LV4735	3 volt operation
	3/5	SN75LBC187	Optimised for Laptop Applications¥

Control Circuits

Function	Type	Features
ACE+	TL16C450	Single ACE
	TL16C451	Single ACE with parallel port
	TL16C452	Dual ACE with parallel port
	TL16C550B	Single ACE with FIFO§
	TL16C552	Dual ACE with parallel port and FIFO

Notes

+ ACE: Asynchronous Communications Element.

§ FIFO: First In First Out.

¥ Product currently under development, contact TI representative for further details.

3. Interface Circuits for RS-485

3.1. The Need for Balanced Transmission Line Standards

This section focuses on industry's most widely used balanced transmission line standard, the EIA RS-485. After reviewing key aspects of the standard, the reader will be introduced to the practicalities of implementing a differential transmission scheme based on a factory automation example. Finally, new additions to Texas Instruments EIA product range will be discussed along with their application, where appropriate.

Data transmission between computer system components and peripherals over long distances and under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-485 is a balanced (differential) digital transmission line interface developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to l0 Mbps and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

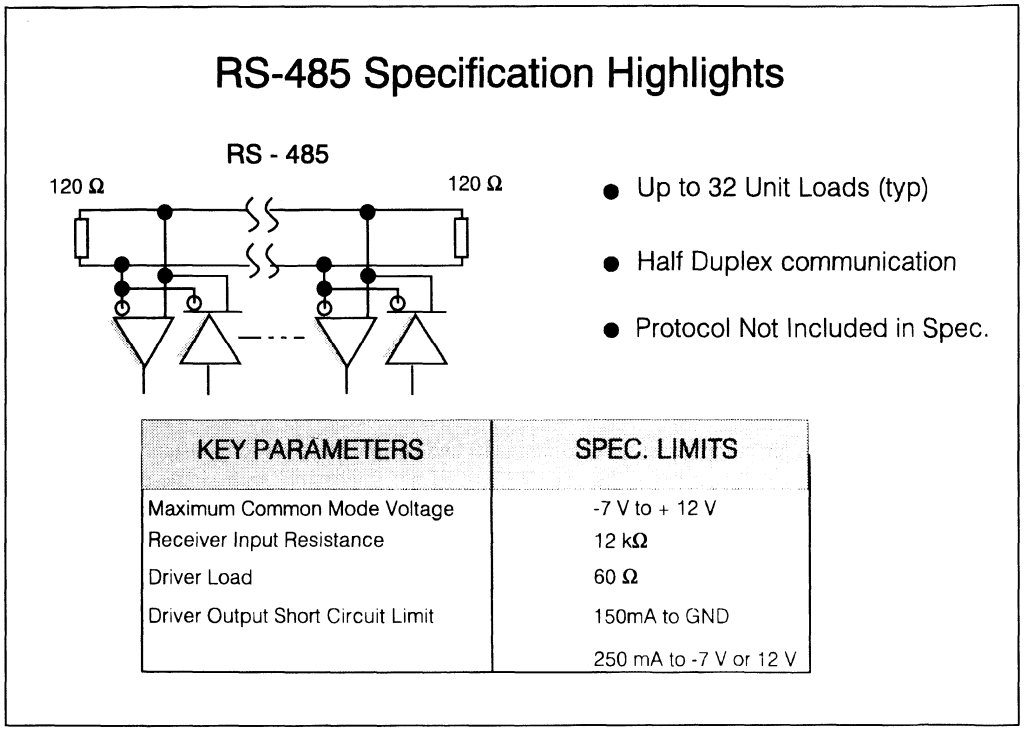
3.1.1. Application Areas

RS-485 is an upgraded version of RS-422-A extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bi-directional multi-point party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the physical layer specification of their standard. Examples include the ANSI (American Nationals Standards Institute) Small Computer Systems Interface (SCSI) which we will discuss in section 4, the Profibus standard, the DIN Measurement Bus.

3.1.2. EIA RS-485

The balanced transmission line standard EIA RS-485 was developed in 1983 to interface a host computer's data, timing or control lines to its peripherals. The standard specifies the physical layer only. Protocols, timing, serial or parallel data, connector choice are all left to be defined by the user



KEY PARAMETERS	SPEC. LIMITS
Maximum Common Mode Voltage	-7 V to + 12 V
Receiver Input Resistance	12 kΩ
Driver Load	60 Ω
Driver Output Short Circuit Limit	150mA to GND
	250 mA to -7 V or 12 V

Figure 4.23 - RS-485 Specification Highlights

RS-485 was originally defined as an upgrade and more flexible version of RS-422-A. Where RS-422 facilitates simplex communication only, RS-485 allows for multiple drivers and receivers on a single line facilitating half-duplex communication. Like RS-422 the maximum line length is not specified but, based on 24 AWG cable, is nominally around 1.2 km. Maximum data rate is unlimited and is set by the ratio of rise time to bit time, similar to EIA-232. In many cases it is the line length of the cable which limits the data rate more than the drivers due to transmission line effects, see section 1.

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multi-point communications.

3.1.3. RS-485 Driver features

i. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

ii. The driver output, off-state, leakage current should be 100 μA or less with any line voltage from -7 V to +12 V.

iii. The driver should be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from -7 V to 12 V.

iv. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

3.1.4. RS-485 Receiver features

i. High receiver input resistance, 12 kΩ minimum.

ii. A receiver input common-mode range of -7 V to 12 V.

iii. Differential input sensitivity of ±200 mV over a common-mode range of -7 V to 12 V.

3.2. Process Control Design Example

To fully understand the considerations of designing an RS-485 system it is advantageous to take a specific design example. In this case we will consider a factory automation system with a host controller and several out-stations. Each out-station is capable of transmitting as well as receiving data.

The general system specification is shown in figure 4.24 and comprises:

i. Furthest out-station is 500 m from the host controller.

ii. We require up to 31 out-stations on the line. With the host controller this totals 32 stations in total.

iii. System data rate will be 500 kilobits per second.

iv. Only one cable will be used for data transmission operating in half duplex mode.

With this system specification the main design consideration are:

i. Line Loading including termination.

ii. Cable choice

iii. Signal Attenuation and distortion

iv. Fault Protection including fail safe operation

Consider each one of these points:

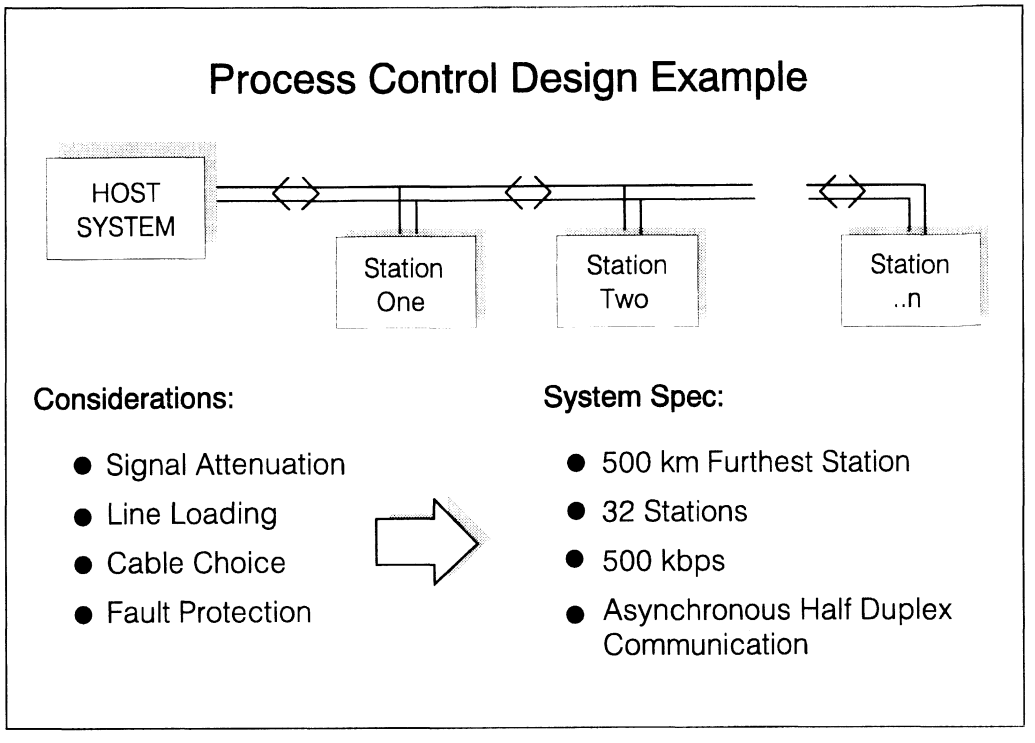


Figure 4.24 - Process Control Design Example

3.3. Line Loading

The RS-485 standard takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether to terminate or not will be system dependent and will be affected by the choice of line driver and the maximum line length.

Line Termination

As we discussed in section 1 the test for whether a transmission line is to be considered as a distributed parameter model or a lumped parameter model is dependent upon the relationship of signal rise time, t_T, at the receiving end and the propagation time of the signal down the cable. The threshold between the two types of transmission line is given by the following equation:

$$2t_{pd} = t_T$$

If we build a margin of error into this equation a better test is to determine the relationship of twice the rise time to 5 times the propagation delay:

If the relationship $2t_{pd} \geq 5t_T$ is true then the transmission line must be treated as a distributed parameter model and terminated accordingly. If the converse i.e. $2t_{pd} \geq \frac{t_T}{5}$ is true. the transmission line can be treated as a lumped parameter model and termination is not necessary.

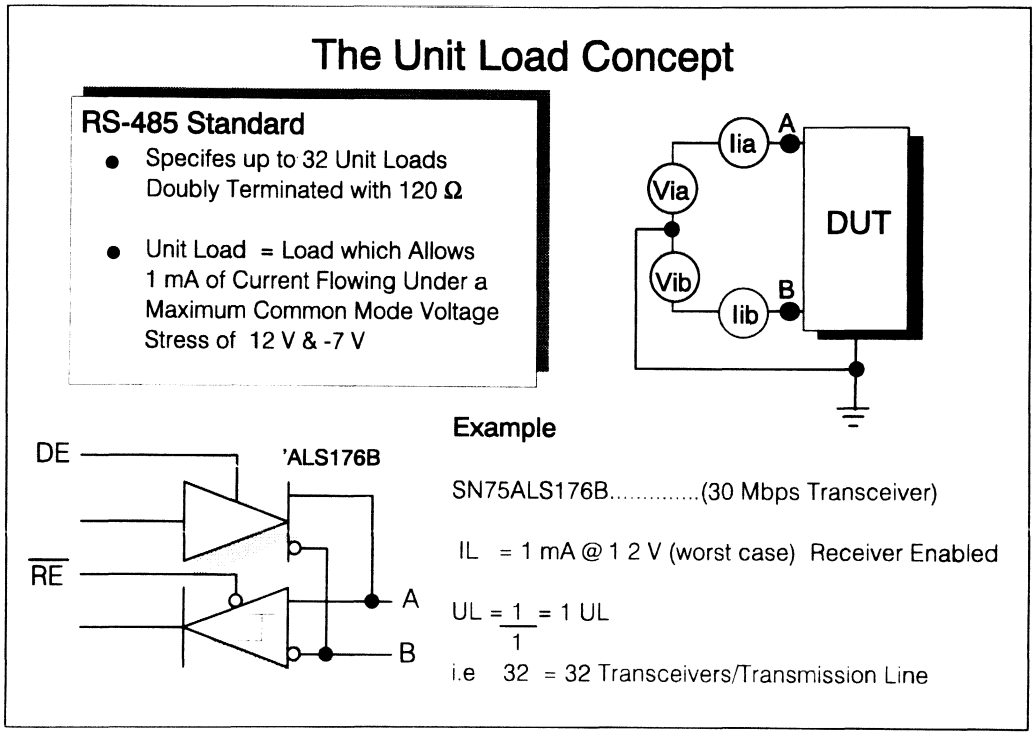


Figure 4.25 - The Unit Load Concept

To determine t_T tests must be carried out on the transmission cable. For the purposes of this example we chose a low cost non shielded, twisted pair cable - 500 m of a Belden type 8205 cable as supplied by RS Components Ltd of the UK, reference number 360-964. On the driving and receiving ends we connected a SN75ALS176 single channel transceiver. The rise time at the receiver end measured :

t_T = 0.9 µs to the 10% and 90% points.

Assuming a propagation delay down the line of 5 ns/m, the time tpd = 500 x 5 = 2500 ns or 2.5 µs.

so in this case:

5 t_T = 4.5 µs and $2t_{pd}$ = 5 µs, so 2 tpd > 5 t_T and therefore the transmission line should be considered as having a distributed parameter model and consequently must be terminated in its

characteristic impedance. In this case as we are using half duplex transmission the line must be terminated at the furthest ends.

To determine the characteristic impedance of the cable we used the technique described in section 1.5.4. Z_O in this case measured at 100 Ω.

The Unit Load Concept

The maximum number of drivers and receivers that can be placed on a single RS-485 communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

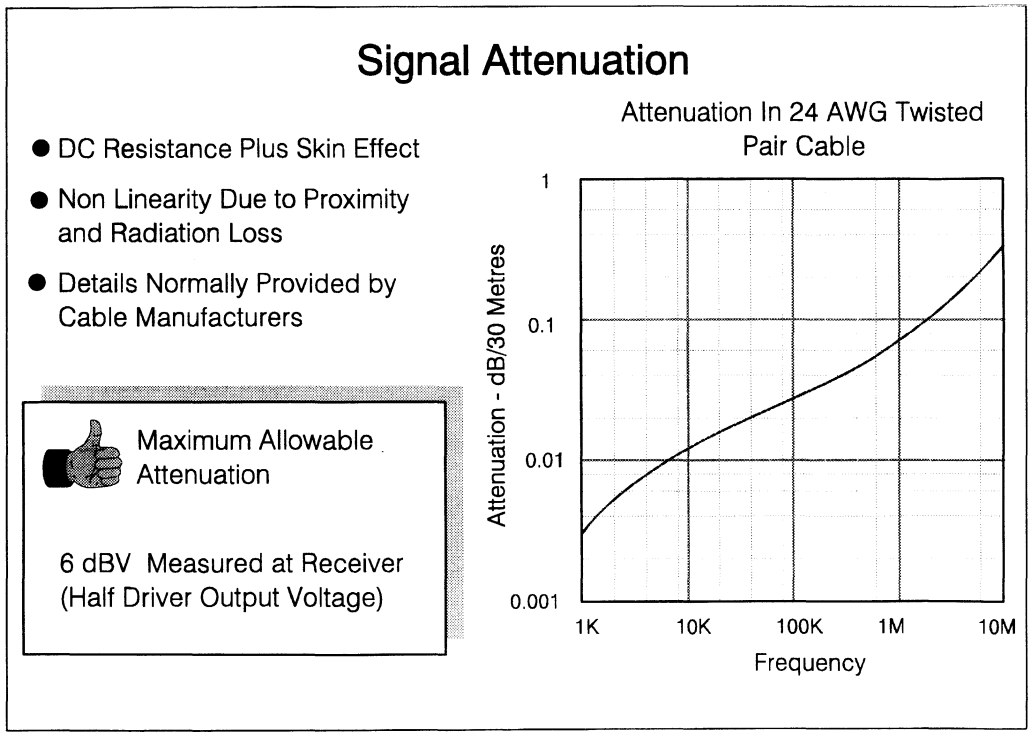


Figure 4.26 - Signal Attenuation

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V. The loads may consist of drivers and/or receivers but does not include the termination resistors, which may present additional loads as low as 50Ω total for doubly terminated lines.

The example in figure 4.25 shows a unit load calculation for the SN75ALS176B. Since this device is internally connected as a transceiver, i.e. driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is

made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 U.L. which will allow up to 32 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designer's risk.

3.3.1. Signal Attenuation

Section 1.3 discusses attenuation in more detail but a sufficient rule of thumb is where the attenuation of the line reduces the driven signal by no more than 6 dBV. Attenuation figures are usually supplied by cable manufacturers. The curve in figure 4.26 shows the attenuation curve versus frequency for 24 AWG cable. For 500 metres of cable and using the 6 dBV figure, the maximum attenuation we can tolerate is 0.35 dBV/30 metres. In this case the 500 kbps data rate attenuation is well within this limit. The attenuation of the fundamental frequency and higher frequency components of the signal up to 10 Mbps will still be detectable at the receiver. This effect coupled with the the variation of signal velocity with frequency (termed dispersion) results in distortion of the pulse at the receiving end of the line.

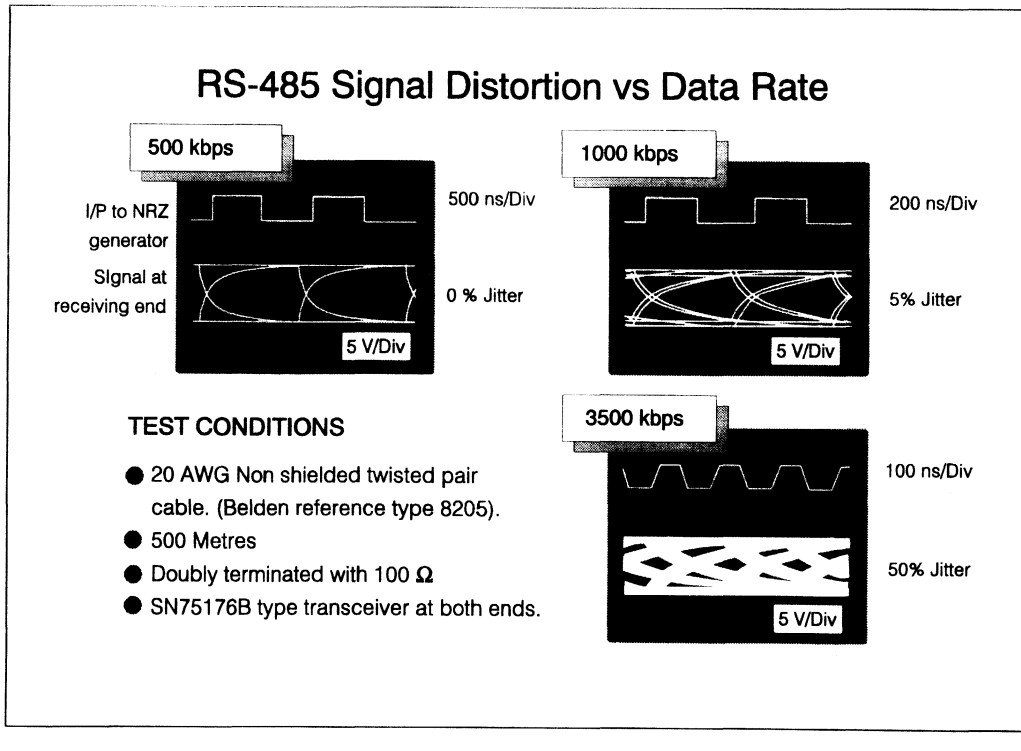


Figure 4.27 - RS-485 Signal Distortion vs Data Rate

3.3.2. Signal Distortion Vs Data Rate

The simplest way to determine the effects of random noise, jitter, attenuation, dispersion, on the inter symbol interference is by the use of eye patterns. For information on how to set up eye patterns, refer to section 1.4 of this Section. Figure 4.27 shows the distortion of the signal at the receiving end of 500 metres of 20 AWG twisted pair cable at different data rates. Using the system constraint of 500 kbps, we see the distortion is limited to the rounding of the signal pulse. If the data rate is increased further, the effects of jitter then become noticeable. In this case at 1 Mbps we begin to observe 5% jitter. At 3.5 Mbps we start to loose the signal completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system should be limited to 5%. The causes of jitter are discussed in more detail in section 1.4.2.

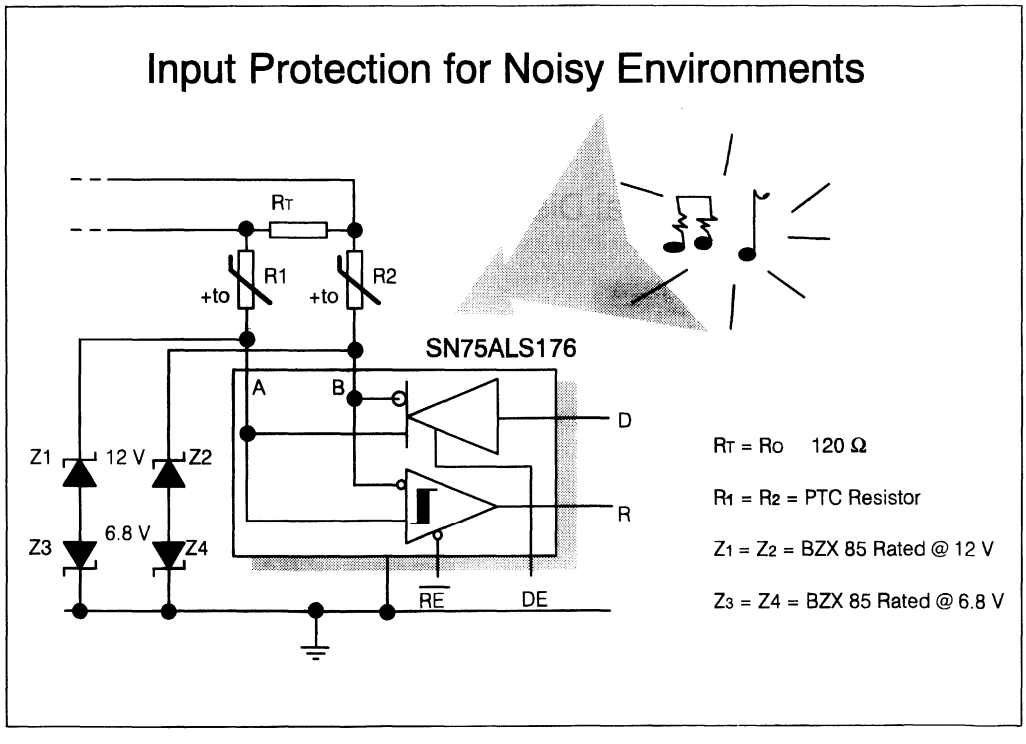


Figure 4.28 - Input Protection for Noisy Environments

3.3.3. Fault Protection and Fail Safe Operation

Fault Protection

Factory control applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 can be insufficient. Protection can be accomplished in a number of ways, the

most effective being through galvanic isolation which we will discuss later. Galvanic isolation provides system level protection but does not necessarily limit the voltages indcued on the transmission lines with respect to the RS-485 driver/receiver grounds. This can be accomplished by the use of protection diodes.

Figure 4.28 shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

Fail Safe Operation

The feature of fail safe protection is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

The Need For Fail Safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle and occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or logic low state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe**. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input regardless of whether the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination if present when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of open line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved of little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting input of the receiver. These resistors are normally in the range of 100 kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few millivolts are generated. As a result

this voltage (receiver threshold voltage) is insufficient to switch the receiver. To use these internal resistors effectively means no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

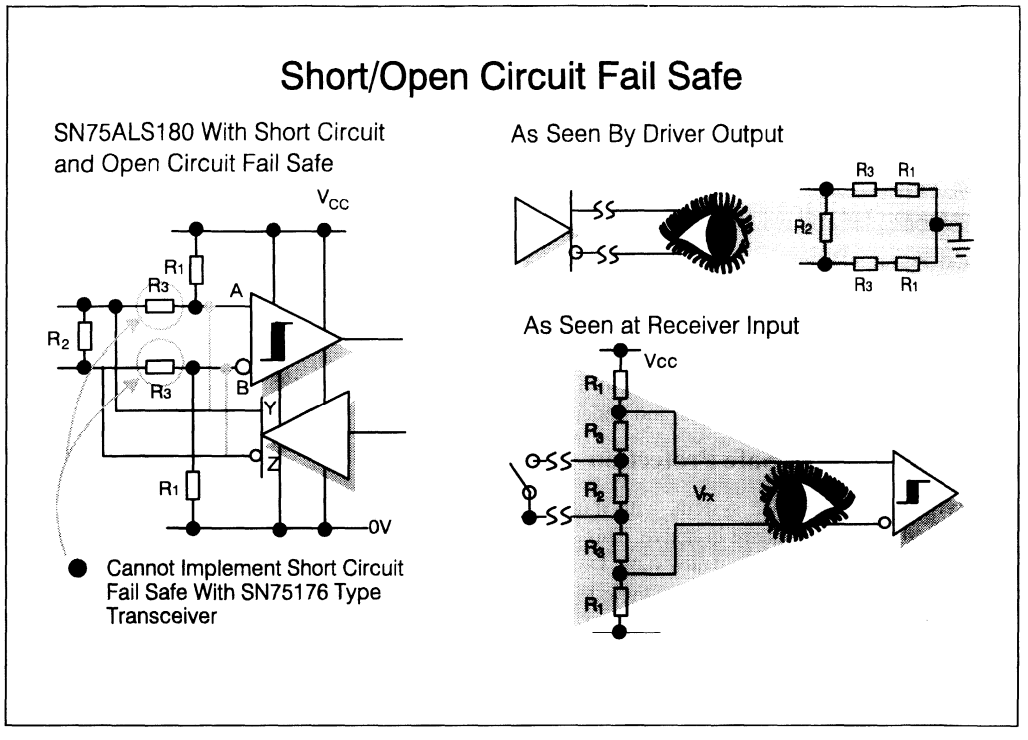


Figure 4.29 - Short/Open Circuit Fail Safe

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an ac. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedance's. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance, Z_O, produces a potential divider between $2R_1$ and Z_O. The voltage formed across the line, V_{OC}, equals

$$V_{oc} = V_{cc} \times \frac{Z_o}{2R_1 + Z_o}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{OC} to be greater than 200 mV. From this the relationship of R_1 to Z_O can be derived:-

$$R_1 = Z_o \times \frac{1}{2} \times \frac{V_{cc} - V_{oc}}{V_{oc}}$$

With V_{CC} = 5V, V_{OC} = 200 mV and Z_O = 100 Ω, yields R_1 = 1.2 kΩ.

Biasing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers, like the SN75ALS176, it is not possible to provide shorted line fail safe configurations, since the driver and receiver share the same IC. pins. Hence for devices like the SN75ALS176 this open line configuration is the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in figure 4.29, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The 'ALS180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{cc} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 applications the standard specifies V_{rx} to be greater than 200 mV. So

$$V_{rx} = V_{th} = 200 \text{ mV}.$$

Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \quad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = \tfrac{1}{2} R_2 \times [\{(V_{cc} - \alpha V_{th})(V_{cc} - V_{th})\}/\{(\alpha - 1) V_{th} V_{cc}\}]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_o, therefore

$$Z_o = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \quad \textbf{(c)}$$

Combining equations **(a), (b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = \tfrac{1}{2} Z_o \times \frac{(V_{cc} - V_{th})^2}{(\alpha - 1) V_{th} V_{cc}}$$

$$R_2 = Z_o \times \frac{V_{cc} - V_{th}}{V_{cc} - \alpha V_{th}}$$

$$R_3 = \tfrac{1}{2} Z_o \times \frac{V_{cc} - V_{th}}{\alpha - 1 V_{th}}$$

In this application assuming the supply voltage is 4.5 V and V_{th} = 200 mV with an a value α of 1.5 and driving a line with characteristic impedance of 120 Ω yields the following values:-

R_1 = 2.2k Ω

R_2 = 120 Ω

R_3 = 110 Ω

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R_1 resistors are the same, and that all R_3 resistors are the same Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 12 kΩ.

3.3.4. Galvanic Isolation

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in figure 4.30.

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

For example consider the case in a process control system where the interface node, shown in figure 4.30, connects between a data logger and host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a process control type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit.

capability. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability.

Transceiver protection circuitry is formed by Z_1, Z_2, Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

The bus driver used is the **SN75LBC176**, chosen for its low power consumption and high data rate Using a cable with a characteristic impedance of Z_O = 120 Ω and a desired V_{TH} of 200 mV, requires $R_1 = R_2$ to be around 1.6 kΩ in value. The terminating resistor, R_T would be in the order of 124 Ω.

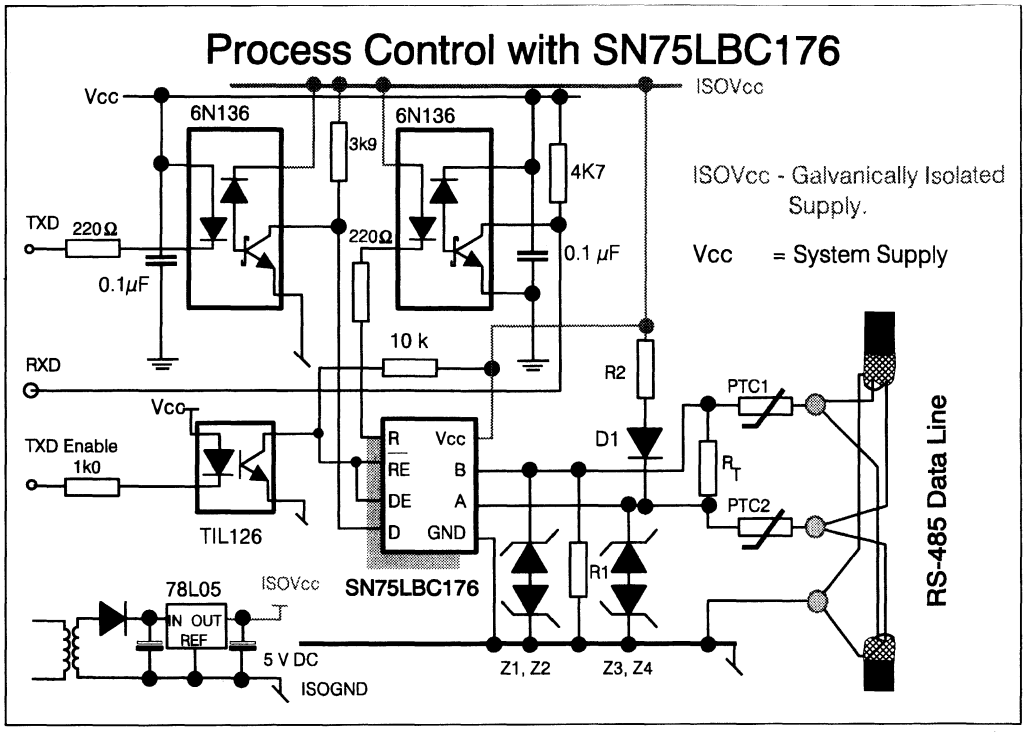


Figure 4.30 Process Control SN75LBC176

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions. The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/opto isolators. The 6N136 is chosen for its high data rate capability, t_p = 75 ns (max), and its high voltage isolation.

The 6N136 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The 6N136 consists of a GaAsP light emitting diode and integrated light detector, composed of a photo diode, a high gain amplifier and a Shottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of

13 mA (eight 1.6 mA TTL loads). A TTL input is provided for applications that require output transistor gating.

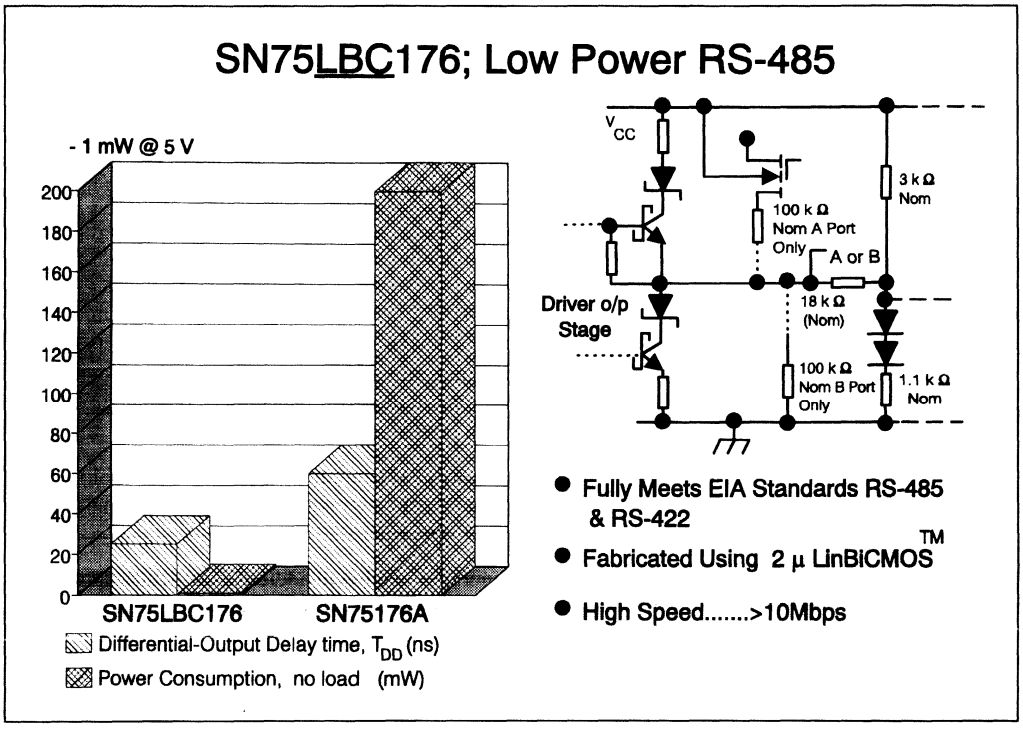


Figure 4.31 - SN7LBC176; Ultra Low Power

Housed in a single 8-pin dual-in-line plastic package the 6N136 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000 Vµs.

A 0.1 µF capacitor has been connected between V_{CC} and ground to improve switching performance.

3.4.SN75LBC176; Ultra Low Power

The key feature of the SN75LBC176 is the very low power consumption, 1 mW. Compare this to the consumption of the older generation SN75176A, where the quiescent power is as high as 200 mW. Normally low power consumption signifies a reduction in ac performance. In the case of the 'LBC176 the ac performance is improved over the SN75176A. Data rates of greater than 10 Mbps are achievable while still being conformant to RS-485. The low power consumption has further benefits than simply reducing supply current:

3.4.1. Improve MTBF

Although not representing the most glamorous end of the semiconductor design spectrum, reliable line interface circuits are crucial if the overall system mean time between failure (MTBF) is to be minimised. System designers have long been aware that often the weak link in ensuing system reliability has been line interface circuits. This vulnerability is due in part to the circuits close proximity to the outside world via the edge connector. Consequently interface circuits are particularly susceptible to failure from high external voltages caused by noise, ESD or incorrect insertion of cables. For this reason the technology of choice for many Texas Instruments emerging interface products is LinBiCMOS.

LinBiCMOS, the Technology of Choice

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3 µm pure CMOS technology with 16 V capability, making it ideal for the design of low power analog products such as op-amps and analog-to-digital converters (many examples of which are discussed elsewhere in this book). By shrinking the geometry to 2 µm and adding a high performance 30 V bipolar structure, a new analog merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost , as many "nice to have" features can make a process too expensive to address a wide range of opportunities.

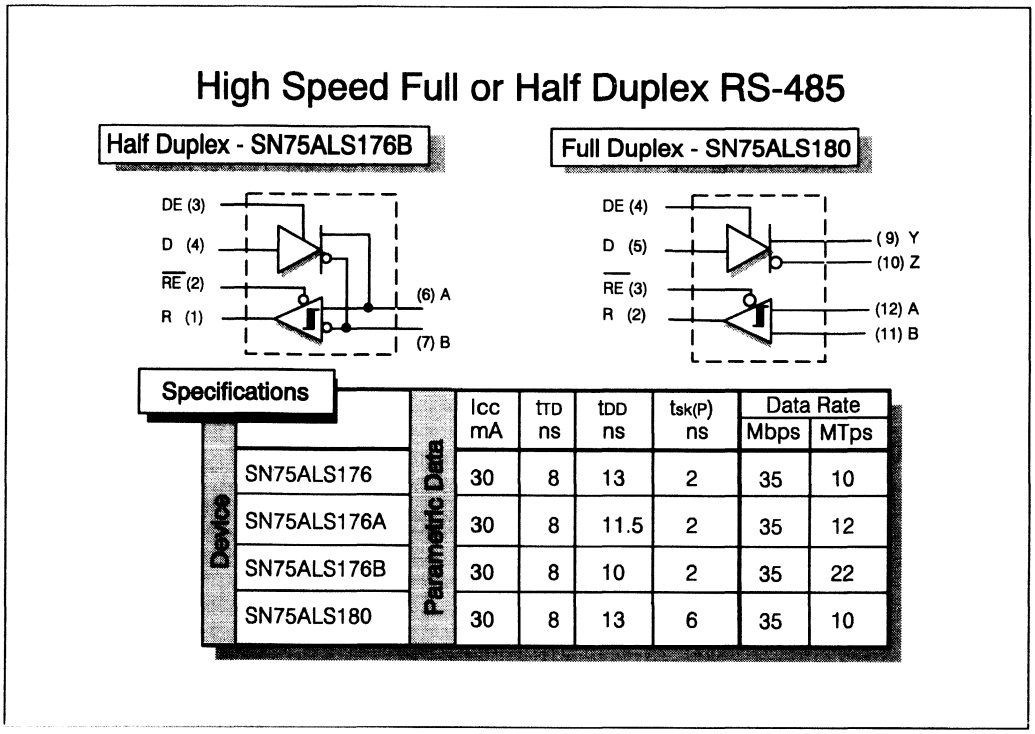
By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective. Modules available for LinBiCMOS

include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and shottky diodes for clamping.

The Applications

With its high voltage capability and excellent switching speed LinBiCMOS is ideal to address standards such as EIA-232 and RS-485. For example the RS-485 standard, demands that driver outputs can be shorted to +12V and -7V without damage. This is particularly difficult to implement as RS-485 devices are designed to operate from a single 5 V supply, meaning that parts of the chip must be designed to operate well outside its supply rails. Further more the "party line" nature of the standard requires devices that must be able to withstand contention (multiple drivers accessing the bus simultaneous) without failure. For this reason short circuit protection and thermal shutdown are built into the chip.

The standard SN75LBC176 is charaterised for commercial temperature range applications. For more extreme conditions the SN65LBC176 extends the operating range to -40°C to +85°C.



Device	Icc mA	tTD ns	tDD ns	tsk(P) ns	Data Rate Mbps	Data Rate MTps
SN75ALS176	30	8	13	2	35	10
SN75ALS176A	30	8	11.5	2	35	12
SN75ALS176B	30	8	10	2	35	22
SN75ALS180	30	8	13	6	35	10

Figure 4.32 - High Speed Full or Half Duplex RS-485

3.4.2. Full Duplex and High Speed RS-485

In the process control example we discussed earlier, the key requirement has been for reliable data transmission over 500 metres of cable. The data rate under consideration was limited to 500 kbps however in many systems the data rate requirements are in excess of 10 Mbps. Cable length must be reduced accordingly as transmissions at this rate are only possible over short line lengths, <50 metres. We have discussed the SN75LBC176, however for speeds above 10 Mbps we must look towards a technology which is more well suited for high speed applications.

Advanced Low Power Shottky technology provides the key to the quest for speed. The SN75ALS176 utilises the true benefits of ALS pushing the data rate to over 35 Mbps. For synchronous systems where skew limits are critical, the SN75ALS176B facilitates 22 MTps (Million Transfers per second). This is the highest speed RS-485 transceiver on the market today.

The SN75ALS176, like the SN75176, DS3695, TL3695, is of a transceiver configuration. As shown in figure. 4.32, the transmit and receive pins are accessible through pins 6 and 7 only. With this configuration communication is limited to half duplex only. For quasi-full duplex operation, using two separate RS-485 lines, one must use a device like the SN75ALS180. this device allows separate lines to

be connected to both the receiver and driver. The 'ALS180 has similar performance to the 'ALS176 facilitating up to 35 Mbps.

3.4.3. RS-485 Selection Guide

In this section we have concentrated on the single transceiver type function. TI does however support a wide range of parts compliant with the RS-485 standard in various configurations and multiples. The below selection guide is provided for convenience. The reader is advised to consult the Interface Circuits Data Book (Reference SLYD006) for the latest technical specifications.

RS-485 Data Transmission Circuits

Device	Devices	Device	Key
Line Drivers	4	SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
Line Receivers	4	SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS173	High Speed
		SN75ALS175	High Speed
Line Transceivers (Drivers / Receivers)	1	SN75176A	Reduced Slew-rate
		SN75176B	Industry Standard
		SN75177B	Industry Standard Repeater
		SN75178B	Industry Standard Repeater
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
	1/1	SN75179B	Industry Standard
		SN75ALS180	Full Duplex Communication
		SN75ALS181	Full Duplex Communication
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
	3	SN75ALS170	High Speed
		SN75ALS171	High Speed
		SN75ALS1711	High Speed
	9	SN75LBC976	Low Power

Notes

¥ Product currently under development, contact TI representative for further details.

4. Interface Circuits for SCSI

4.1. SCSI Overview

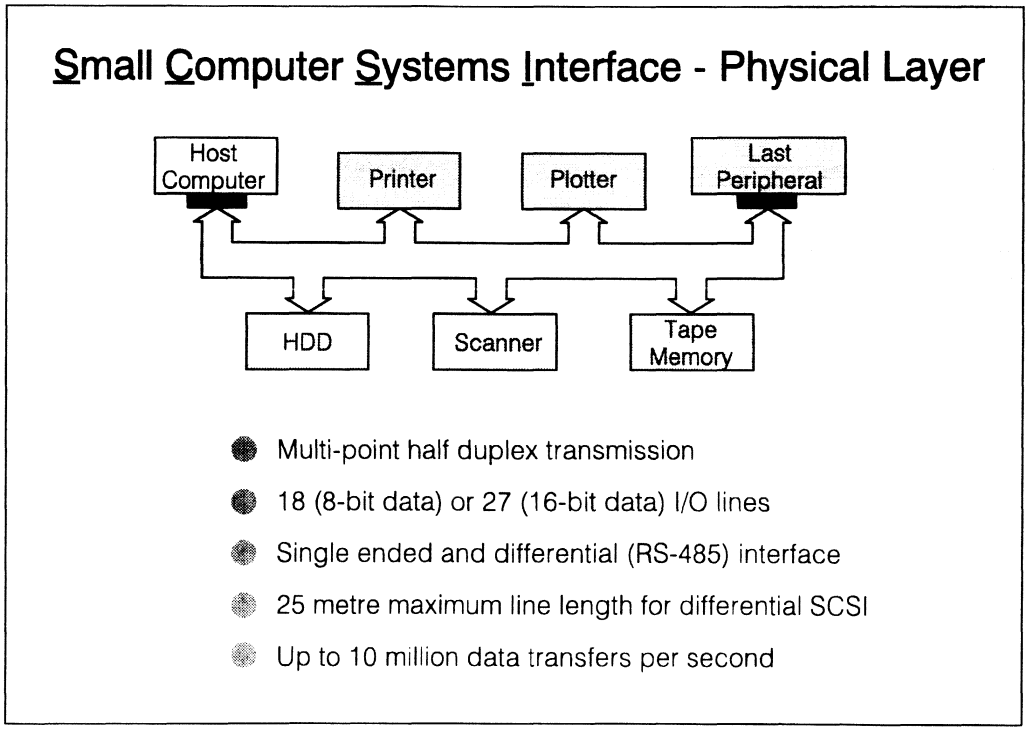


Figure 4.33

SCSI is the acronym for Small Computer Systems Interface and details the ANSI specification for a peripheral bus and command set. The specification defines a high performance peripheral interface that distributes data independently of its host, helping to free up the host for more user oriented commands. The objective of the interface is to provide high speed data transfer between computer peripherals

independently of the host. Already there are a large number of disk drives, notebook PCs, and CD ROM drives incorporating a SCSI port.

Basic SCSI is an eight bit parallel I/O bus, with parity, and nine control/handshaking lines, making . 18 lines in total. More recently, to increase the data throughput, the data bus has been increased to 16 bits with two parity bits while maintaining the nine control lines, making for 27 lines in total. This is referred to as wide SCSI.

4.1.1. SCSI Physical Layer

There are two electrical specifications referred to in the SCSI standard, single ended and differential:

It is beyond the scope of this seminar hand book to discuss the complete SCSI standard, we shall concern ourselves with the physical layer only. For more information on the standard the reader is encouraged to refer to the numerous publications on SCSI.

Single Ended Interface

The single-ended driver and receiver configuration utilises TTL logic levels and is primarily intended for applications with a cabinet, the maximum line length being limited to 6 metres and the data rate is normally limited to 5 Million Transfers per second (MTps), although innovative termination techniques enable the maximum trasnfer rate to approach 10 MTps.

Differential Interface

The differential driver and receiver configuration uses the EIA RS-485 standard and is primarily concerned with transmitting data between cabinets. Maximum line length is 25 metres with the maximum data rate currently 10 MTps.

4.2.Single Ended SCSI

4.2.1. Termination of Single Ended Bus

Termination of the single ended SCSI bus is becoming increasingly important as designers strive for faster system speeds. If error-free data rates of 10 Mbps over the 6 metre bus are to be achieved then signal integrity must be preserved. Termination will reduce unfavourable transmission line effects such as reflections and distortion which can degrade system performance as signal speeds increase. Proper termination of a bi-directional bus such as SCSI requires terminators at each end of the cable.

4.2.2. Signal Transitions

The potential for high data rates depends upon quick and clean transitions between low and high signal levels. The range of SCSI signals is shown below in fig 4.33.1. A low to high transition, or de-assertion, of a signal is initiated by an open collector driver switching off and causing an instantaneous voltage step to travel down the line.

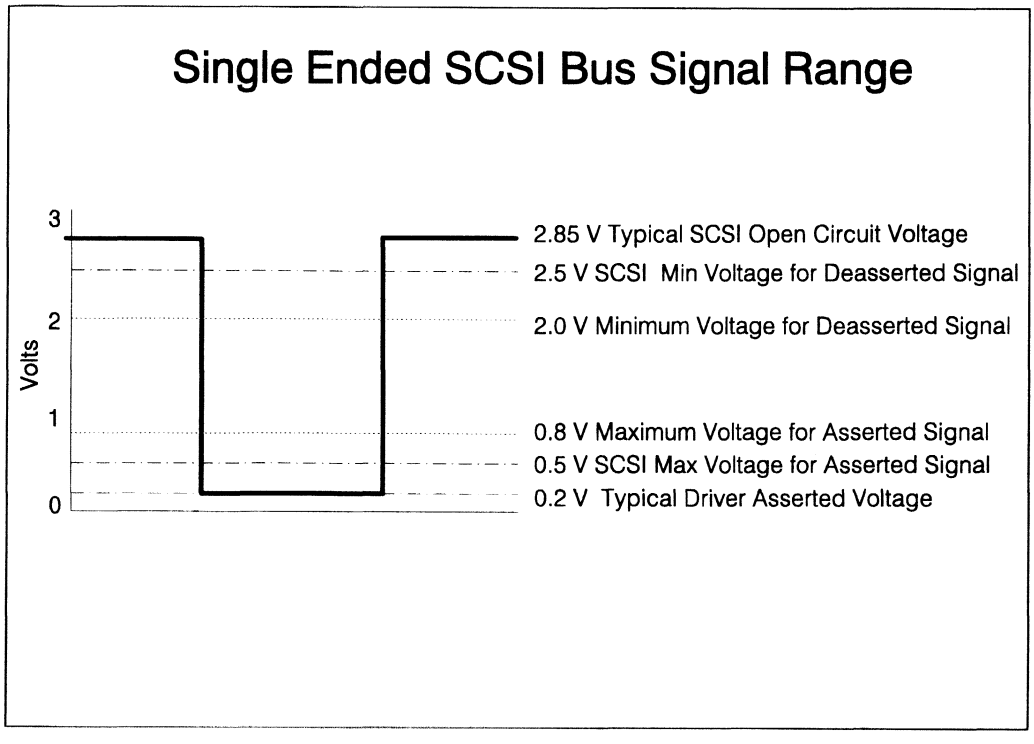


Figure 4.33.1 - SCSI Bus Signal Range

The size of the first step on de-assertion depends upon the amount of current in the line, I_L, the characteristic line impedance seen by the signal, Z_O, and the driver output-low voltage (V_{OL}), and can be calculated as follows ;

$$V_S = V_{OL} + Z_O I_L$$

To achieve the maximum data rate the first step needs to exceed the receiver threshold voltage in a single transition. Although the 110 Ω impedance of a typical SCSI ribbon cable suggests that this will require only limited line current capability, the impedance seen by a signal is always less than the specified cable value. Extra capacitance due to peripheral connections to the bus, transmission line effects, and the position of the signal source, can all combine to reduce the effective impedance by 50% or more.

To make up for this lack of 'real' impedance, it is the terminators job to source as much current as possible during de-assertion. This role is restricted by the SCSI specification, however, which limits each terminator to supplying a maximum of 24 mA to prevent the line current from exceeding the 48 mA current sink limit of the open collector drivers.

The role of the SCSI terminator is not confined to low-to-high signal transitions. Once a signal has been de-asserted the terminator is required to bias the bus lines to the correct open circuit voltage level and thereby provide maximum noise margins.

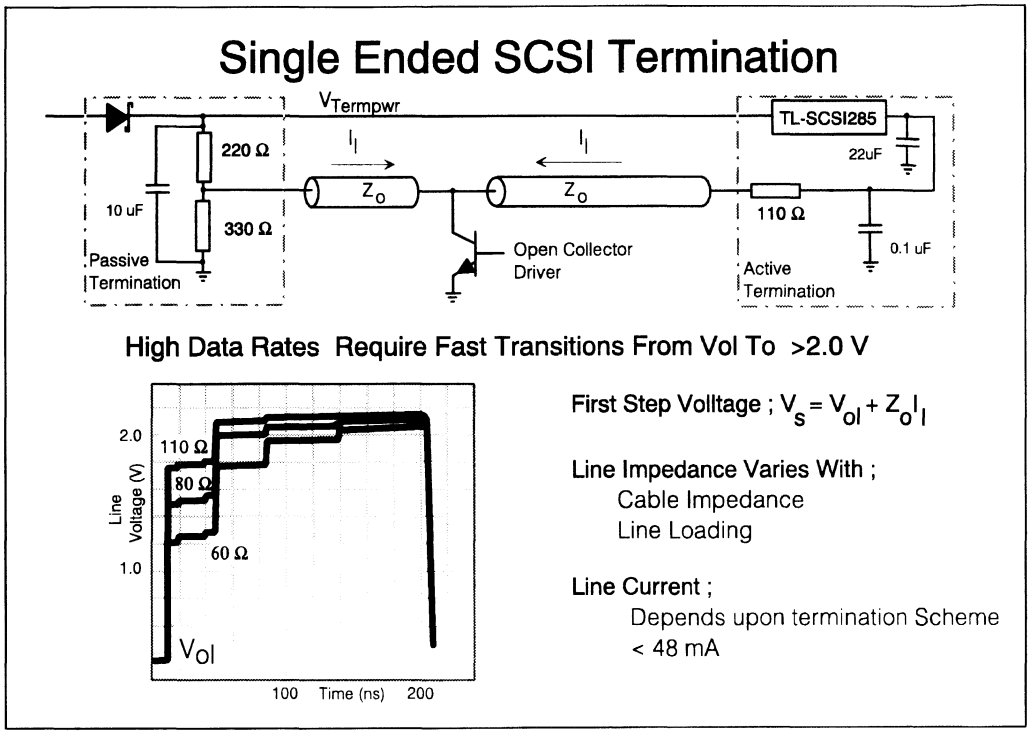


Figure 4.34 - Single Ended SCSI Termination

4.2.3. Passive and Active SCSI Termination

SCSI termination has traditionally been carried out using passive termination networks. As illustrated in figure 4.34 these consist of 2 resistors per signal line ; a 220 Ω pull up resistor connected to the termination power source (Termpwr), and a 330 Ω pull down resistor connected to ground. The Shottky diode is needed by all termination schemes to protect the power source from reverse currents.

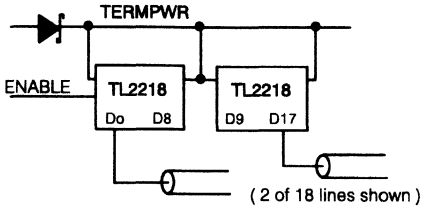
This type of termination typically results in a maximum line current of around 17 mA. Assuming the terminator is on a heavily loaded bus, signified by an impedance of approximately 75 Ω, then the above equation gives a first step value of 1.76 V - well short of the desired 2.0 V level.

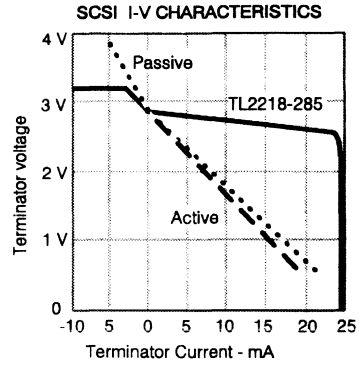
In addition to this limited current capability and the power consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result the line voltage will fluctuate with variations in the load current and Termpwr, leading to smaller noise margins, lower line currents, and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110 Ω resistor per line (fig 4.34). This method, known as Active, Boulay, or Alternative 2 termination, was developed to overcome two of the main shortcomings of passive termination.

TL2218-285 - Current Source Terminator

TL2218-285 Enables Single Ended Data Rates of 10 MHz





- 23 mA Applied at First High-Level Step
- Very Low Output Capacitance, Typically 6 pF
- No External Components Required
- Compatible with Active Negation
- Thin Shrink Small Outline Package (TSSOP)

4.35 TL2218-285 Current Source Termination

The 110 Ω resistors increase the typical line current available on de-assertion to 21 mA, which, from a transmission line viewpoint, is equivalent to a 35% increase in line impedance. The line current and the high-level noise margins are also more stable since Termpwr is no longer used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage.

The TL-SCSI285 and TL2217-285 low dropout regulators from Texas Instruments are specifically designed for active SCSI termination. With an overall accuracy of 2 % and a maximum dropout voltage of 0.6V the TL-SCSI285 is the highest performance dropout regulator available for SCSI active termination.

4.2.4. Current Source Termination Using the TL2218

Although active termination brings a number of advantages to SCSI termination these can be further improved upon. The TL2218-285 from Texas Instruments is a completely new type of SCSI terminator which does just that.

During de-assertion the TL2218-285 operates as a 23.5 mA current source which is able to maintain this current level until the signal reaches the correct SCSI open circuit voltage. At this point the TL2218-285 becomes a voltage source of 2.85 V.

The additional current supplied by the TL2218-285 reduces the low-to-high transition time by ensuring that each voltage step is consistently the largest possible. The effect of this can be seen in figure 4.36, which shows the signal wave forms obtained after using a TL2218-285, a commercially available active terminator, and a passive termination network to terminate a 50 Ω cable (the equivalent of a heavily loaded bus). Even at 10 MHz the first step voltage of the TL2218-285 terminated system still exceeds the desired 2.0 V level.

Another feature of the TL2218-285 is the inclusion of a disable function which allows the terminator output to be shut down. This is particularly useful for a peripheral which finds itself somewhere other than the physical end of the bus, and needs some way of easily 'removing' its terminator. If disabled the TL2218-285 consumes just 500 µA of current, and maintains an output capacitance of 6 pF. Allowing for the 15 - 16 pF typical output capacitance of a peripherals transceivers, this will give a total node capacitance well within the 25 pF SCSI limit. An active terminator, on the other hand, will normally maintain a disabled output capacitance of 10 pF, often leaving the system to operate outside of the SCSI specification.

Use of the TL2218-285 also removes two possible causes of system failure or driver damage associated with active termination.. Firstly the 2% output tolerance of the TL2218-285 ensures it does not supply more current than allowed by the driver protecting SCSI limit. The tolerances of the voltage regulator and the 110 Ω resistors used in active termination, however, can result in the terminator supplying in excess of the maximum 24 mA.

The other potentially damaging situation arises when active negation drivers are being used. These devices sense bus voltages and source sufficient additional current to ensure that first step voltages reaches the minimum SCSI level. Despite this attractive feature their relatively high cost has limited their use to ultra fast changing control lines such as ACK and REQ. To be compatible with active negation drivers it is clear that any terminator connected to the bus must be able to sink current. Again this is a problem with active termination but not with either the TL2218-285 or a passive terminator. The voltage regulator of an active terminator will shutdown when any driver voltage exceeds 2.85 V. This allows the line voltage to rise and any driver which then pulls low may sink more than their 48 mA limit.

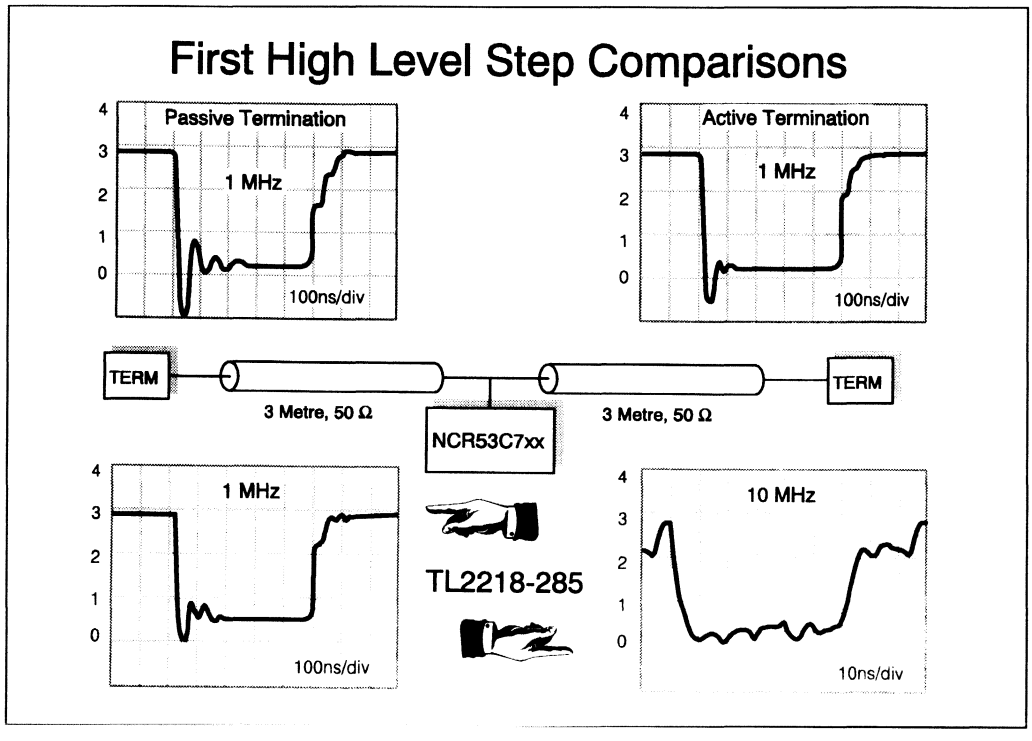


Figure 4.36 - First High Level Step Comparisons

4.2.5. Power Considerations

As well as enabling increased data rates, termination will also increase the power consumption of a SCSI system. As SCSI has found increased usage in portable or battery powered systems this has become more important. Exactly how much depends upon the method of termination, but not quite as obviously as might at first be thought.

During data on periods, the power dissipation of each of the SCSI termination methods is very similar. For an 8 bit bus with all the data lines asserted the power dissipation in each case will be around 1 W.

During data off periods the position is significantly changed. The resistor dividers of a passive terminator will still draw around 750 mW of power. Both the TL2218-285 and active terminators, however, require a total quiescent current of less than 10 mA, providing a 30x saving in power consumption.

For a single TL2218-285 it is possible to calculate a worst case dynamic power dissipation of 493 mW. This assumes that all nine lines in the package are asserted simultaneously and experience a 50% duty cycle. In some systems it may be desirable to avoid any single device dissipating this much power. This can be achieved by partitioning the SCSI bus lines in an appropriate manner. One such method is

to split the data lines between the two devices (for an 8 bit system) and also assign the REQ and ACK lines to separate packages.

Battery powered systems will also benefit from the extended Termpwr range of the TL2218-285. Compared to competing solutions which require a minimum Termpwr of 4 volts, the 3.5 V to 5.5 V range of the TL2218-285 greatly increases the potential for prolonged operation.

4.3. Differential SCSI

4.3.1. SN75LBC976DL; Two Chip Differential SCSI

Much debate has taken place on differential versus single ended SCSI for data rates above 5 million transfers per second (MTps). It is clear however, that for data rates approaching 10 MTps and at line lengths in excess of 6 metres, differential SCSI is essential.

As we discussed earlier, the standard 8-bit interface is made up of 8 data lines, one parity bit, and 9 control lines, making 18 channels in total. The only differential transceivers capable of transmitting at 10 MTps data rate have utilised the LS and ALS technologies. Using these technologies and considering the 18 transceivers per interface the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

From a designers viewpoint, 2.4 watts is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where shear equipment size is the limiting element. A further factor is board area, using one discrete transceiver per channel, i.e. 18 8-pin SO packages, is unacceptable for many applications.

From a semiconductor designers viewpoint integrating a number of transceivers is of course possible however the limiting factor once again is power dissipation. The SN75LBC976 is designed to overcome both the problems of power dissipation and integration. The device incorporates on a single IC, nine RS-485 configurable transceivers each capable of transmitting at 10 MTps. This is made possible using LinBiCMOS technology. With all drivers disabled the quiescent power consumption of the 'LBC976 is a mere 1.5 mW, with all drivers enabled the quiescent consumption rises to 45 mW, a considerable saving over LS and ALS parts. The package size has also been reduced to a minimum using the 0.635 mm pitch 56 pin SSOP package which reduces board area significantly compared with alternate packages such as PLCC. The reader should note that irrespective of the device power, there is still the relatively high line current. The SSOP package has been thermally enhanced to handle this level of power dissipation. We will cover this point later as we look at the thermal characteristics of the package.

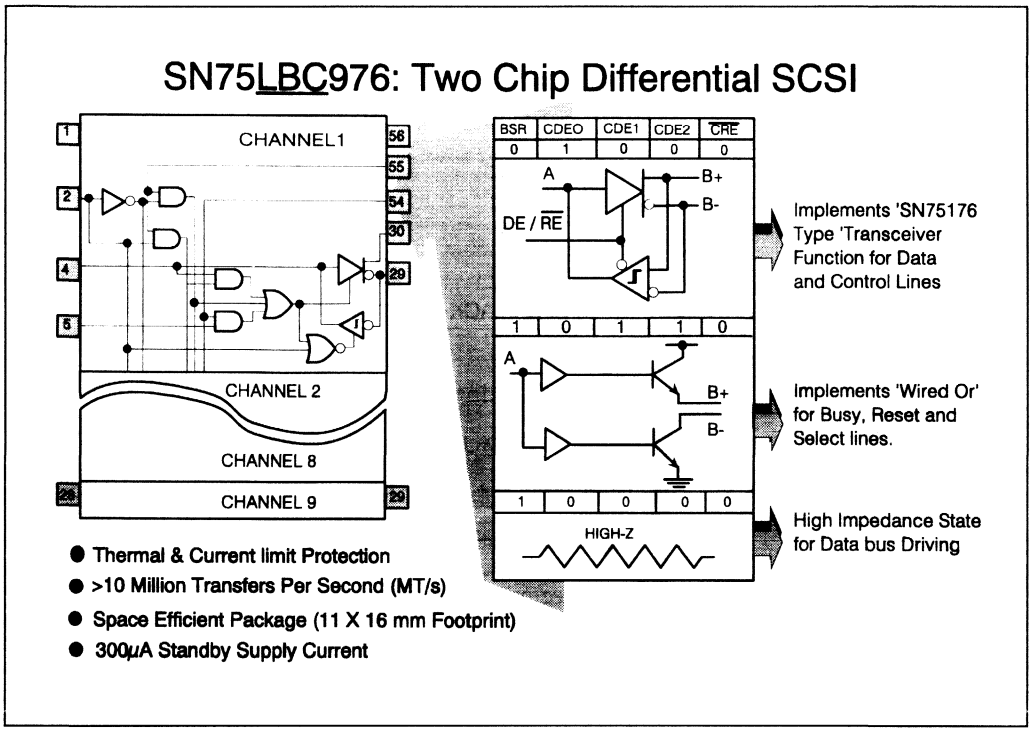


Figure 4.37 - SN75LBC976: Two Chip Differential SCSI

The SN75LBC976 is fully configurable to facilitate connection to any type of SCSI system arrangement. The 9 channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, CRE control pins.

The 7 channel configurations are:

1. Transparent, permanently enabled Receiver.
2. Transparent, permanently enabled Driver.
3. Bi-directional transceiver with direction control.
4. Driver with enable control.
5. Open ended driver for Wired OR control lines.
6. Driver with ORed data and enable lines.
7. Permanent high impedance state.

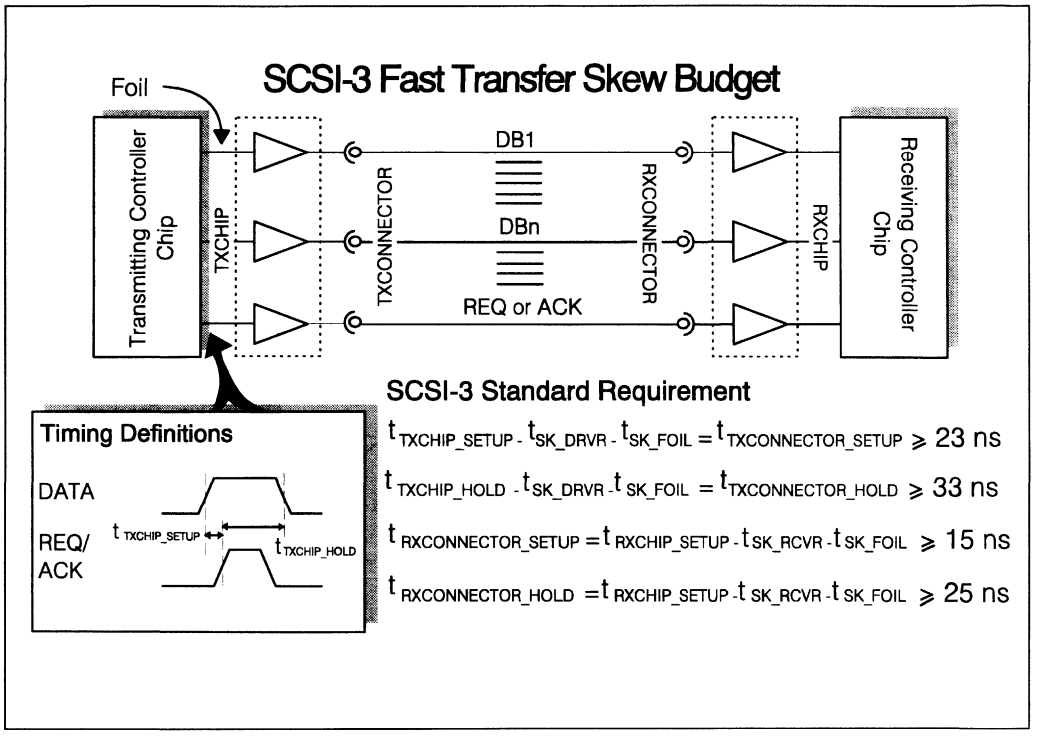


Figure 4.38 - SCSI-3 Fast Transfer Skew Budget

4.3.2. SCSI and IPI Skew Considerations

SCSI as we have discussed is a parallel data bus. This is also the case with IPI. IPI, an acronym for Intelligent Peripheral Interface, is similar to SCSI in that it is a high speed peripheral bus with the same high speed differential interface requirements. By the parallel nature of the interface, both standards transfer data over the cable more than one bit at a time. SCSI and IPI allow 8-bit (one Byte) or a 16-bit (one word) data width and transfers as often as once every 100 ns or 10 million transfers per second.

Since the logical state of any one bit can change every 100 ns, this defines a period during which the logical state should be valid across the bus. This is the unit Interval (UI). The voltage transitions which define the start and end of the UI can propagate along the bus at different velocities due to the physical differences along each electrical path. So the original UI at the start will be different at the destination.

Time variation of the defining voltage transitions is typically called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest minus the slowest propagation delays along any part of the bus. This, in effect, will reduce the UI by $t_{sk(lim)}$ establishing a minimum unit interval, UI_{min}, that can be transmitted with a particular data bus.

The proposed SCSI-3 standard for fast transfers (10 MTps), defines UI_{min} in terms of set-up and hold times at the SCSI connector for inter-operability with any other SCSI device. At the time this document is being written the requirements are as shown in figure 4.38.

The budget behind the connector is left to the designer and depends upon the SCSI controller, transceivers, and layout being used. The table shows some skew budget examples with various controller chips that would comply with the requirements at the SCSI connector. The column under 'Rec' (for recommended) is data for the worst case number for SCSI controllers surveyed by the SCSI SPI Working Group and budgets 8 ns for the external driver and 9 ns for the external receiver. This is the origin of the $t_{sk(lim)}$ specifications in the SN75LBC976 data sheet.

Parameter	Rec	Vendor A	Vendor B	Vendor C	Units
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hold =	15	20	15	10	ns
t_{sk_etch} =	1	1	1	1	ns
max t_{sk_dvr} =	8	6	11	11	ns
max t_{sk_rvc} =	9	4	9	14	ns

Transceiver Skew Budgets for Various SCSI Controllers

The time it takes one transceiver of the 'LBC976 to change logic states is called the propagation delay time. For a driver this is designated as t_{dD} and for a receiver t_{pd} and does not differentiate whether the logical transition is from high-to-low or low-to-high level. The $t_{sk(lim)}$ parameter for the transceiver is nothing more than the maximum difference of the propagation delay times between any two drivers or any two receivers on any two devices. Compliance to the $t_{sk(lim)}$ specifications of the data sheet and the recommendation of the SCSI standard is assured by measuring the propagation delay time of each channel of each 'LBC976 and accepting only those devices within the $t_{sk(lim)}$ band. To keep the production costs of the 'LBC976 reasonable, this testing is done at 25°C and at 70°C ambient temperatures at a V_{CC} of 5 volts.

Admittedly, the die temperatures and supply voltage are all the same (or nearly the same) during TI's production testing and not necessarily the same would be seen in actual use. However the sensitivity of the propagation delay times to these factors is the same and repeatable from device to device. In other words, as long as the operating environment of all of the channels of the SCSI interface is similar, the change in propagation delay times from the data sheet conditions will be the same. This will maintain the $t_{sk(lim)}$ even though the actual propagation delay times may change.

It is nearly impossible to predict the instantaneous die temperatures of these devices in actual use. Due to the non-deterministic nature of the state of any one channel and the averaging affect of nine channels and of the package thermal time constant, the die temperature must be considered using the mean power dissipation. It is also reasonable to assume the mean power dissipation of separate devices on the

same printed circuit board to be close to each other and the temperature of the air around them will not have a large (<5°C) gradient between the two. Even if there was an air temperature gradient of 45°C, there would be only about a 2 ns difference in the driver propagation delay times and, from recent data, little or no difference in the receiver propagation delay times. If such a temperature gradient actually existed across a board, it' is likely that skew budgets are not going to be the problem with the equipment!

In summary:

1. The designer should determine the transceiver skew requirements based upon his controller and board design.
2. The current specification and testing of $t_{sk(lim)}$ of the 'LBC976 is, the best compromise for a cost effective solution.
3. We have application information from our experience gained through numerous users with no inter-operability problems detected at the time of writing.

4.3.3. SN75LBC976 Channel Power Dissipation Considerations

Channel Power Dissipation

To understand the SN75LBC976 power dissipation when connected to a SCSI bus and the subsequent heat sinking requirements, we must develop a realistic model for the power consumption under working conditions. We must consider the power dissipation within the silicon. There are three primary sources, the dc quiescent power, the ac or switching power, and the dc or resistive losses in the output drivers.

The current necessary to bias the circuits of a single enabled 'LBC976 differential driver is typically 0.53 mA and a maximum of 1.1 mA. A single enabled receiver circuit requires 3.22 mA typically and 5.00 mA maximum. The typical values have been measured on 94 SN75LBC976DLs from three different wafer lots. The maximums have been verified over temperature on the same samples.

It follows the driver quiescent power consumption, P_{DCC} is:

$$P_{DCC} = I_{CC} \times V_{CC}$$
$$= 0.53 \text{ mA} \times 5.00 \text{ V} = 2.65 \text{ mW/Channel average}$$
$$= 1.11 \text{ mA} \times 5.25 \text{ V} = 5.83 \text{ mW/Channel maximum}$$

And the receiver quiescent power, P_{RCC} is:

$$P_{RCC} = I_{CC} \times V_{CC}$$
$$= 3.22 \text{ mA} \times 5.00 \text{ V} = 16.10 \text{ mW/Channel average}$$
$$= 5.00 \text{ mA} \times 5.25 \text{ V} = 26.25 \text{ mW/Channel maximum}$$

The average I_{CC} of a representative sampling of the SN75LBC976 has been measured to be 9.77 mA for nine unloaded drivers switching at 5 MHz (10 Mbps), a 50% duty cycle, and at a V_{CC} of 5 V. Nine receivers at the same frequency and duty cycle and unloaded outputs consumed 36.0 mA average. Since both measurements include P_{DCC} or P_{RCC}, they are subtracted below:

Driver switching losses, P_{DAC}, at 5 MHz:

$$P_{DAC} + P_{DCC(average)} = (I_{CC(average)}/9) \times V_{CC}$$

$$P_{DAC} = (I_{CC(average)}/9) \times V_{CC} - P_{DCC(average)}$$

$$= (97.7/9) \times 5.0 - 2.65$$

$$= 51.6 \text{ mW/Channel}$$

Receiver switching losses, P_{RAC}, at 5 MHz:

$$P_{RAC} + P_{RCC(average)} = (I_{CC(average)}/9) \times V_{CC}$$

$$P_{RAC} = (I_{CC\ (average)}/9) \times V_{CC} - P_{RCC(average)}$$

$$= (36.0 \text{ mA}/9) \times 5.0 \text{ V} - 16.10$$

$$= 3.9 \text{ mW/Channel}$$

The output stage losses vary with the magnitude of the output voltages or the output transistor saturation voltages and with the load conditions. The following is based upon the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

For the differential driver, the worst case condition is with a driver asserting the line with SCSI bus termination and a differential output voltage of about 2 V. Under these conditions there would be 144 mW dissipated in the output transistors when asserted and 71 mW when negated. The average output voltage of the SN75LBC976 driver is 2 V. As such, the average power dissipated in the output transistors is also a worst case condition.

Driver output dc losses, P_{DOH} is given by:

$$P_{DOH} = 144.0 \text{ mW/Channel}$$

The same circuit but with the line negated:

$$P_{DOL} = 71.0 \text{ mW/Channel}$$

The receiver output stage is rated for sinking 8.0 mA at a maximum low-level output voltage of 0.8 V.

Receiver output dc losses, P_{RO}, is given by:

$$P_{RO} = 8.0 \text{ mA} \times 0.8 \text{ V} = 6.4 \text{ mW/Channel maximum}$$

Since $P_{DCC} + P_{DAC} = P_{DO} >> P_{RCC} + P_{RAC} + P_{RO}$, the worst case power dissipation in a data channel occurs when the driver is enabled and transmitting data. This case will be used to analyse the device power dissipation.

Device Power Dissipation

Assuming the probability that any one bit on the bus is asserted is equal to the probability of being negated, the state of the output is non-deterministic, and the thermal time constant of the device is long with respect to the data transfer period, the mean die temperature will be determined by the mean power dissipation. In the driver output this is the mean of the asserted and negated values:

Mean device output dc losses:

$$P_{DO(DEV)} = (P_{DOH} + P_{DOL})/2 \times 9 \text{ Channels}$$

$$= (144 \text{ mW/Ch} + 71 \text{ mW/Ch})/2 \times 9 \text{ Channels}$$

$$= 967.5 \text{ mW}$$

From the assumptions above and the probability that the driver output will change state on the next cycle is equal to the probability that it will not, the mean power dissipated due to driver switching is one-half P_{DAC} which was measured with the switching loss occurring every cycle.

Mean device switching losses:

$$P_{DAC(DEV)} = P_{DAC}/2 \times 9 \text{ Channels}$$

$$= (51.6 \text{ mW/Ch})/2 \times 9 \text{ Channels}$$

$$= 232.2 \text{ mW}$$

Total Device quiescent power:

$$P_{DCC(DEV)} = P_{DCC(average)} \times 9 \text{ Channels}$$

$$= 2.65 \text{ mW/Ch} \times 9 \text{ Channels}$$

$$= 23.85 \text{ mW}$$

The total mean power dissipated in 9 enabled drivers transmitting over a SCSI bus for several package thermal time constants is then

$$P_{D(DEV)} = P_{DO(DEV)} + P_{DAC(DEV)} + P_{DCC(DEV)}$$

$$= 967.5 \text{ mW} + 232.2 \text{ mW} + 23.85 \text{ mW}$$

$$= 1223.6 \text{ mW}$$

4.3.4. Junction Temperature and Layout Considerations

Measurements of the thermally enhanced 56-pin SSOP package and lead frame used on the SN75LBC976DL were performed on a 130 mm by 98 mm six layer printed circuit board with the ground and heat sinking pins soldered to a common solder pad and connected to a second layer ground plane through one via interconnect, see figure 4.39. The ground plane was 0.254 mm below the surface of the board and was a 1 oz copper layer. The results of two tests resulted in θ_{JA}s of 52.9 and 46.6°C/W with zero air flow.

The mean junction temperature rise above ambient when all drivers are enabled and transmitting data over the SCSI bus for several package thermal time constants can then be calculated.

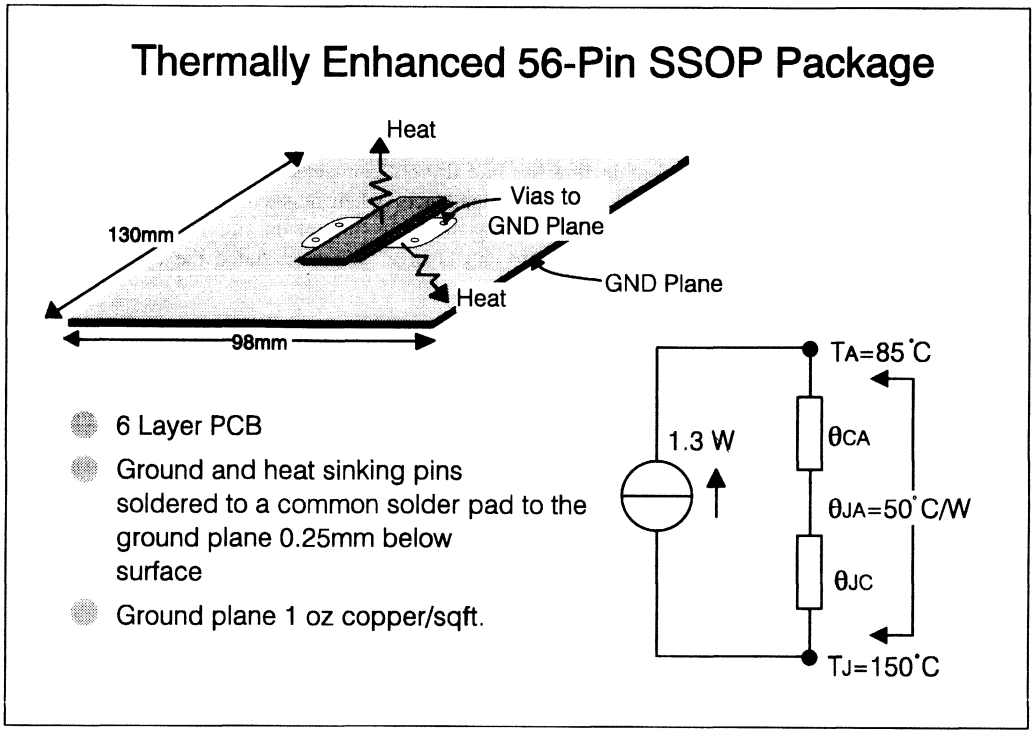


Figure 4.39 - Thermally Enhanced 56-pin SSOP Package

Junction temperature rise above ambient:

$$T_J - T_A = \theta_{JA} \times P_{D(DEV)}$$

$$= (52.9°C/W + 46.6²C/W)/2 \times 1233.6°mW \times 1\ W/1000\ mW$$

$$= 60.8°C$$

Most designs require two junction temperature conditions to be met. The junction operating temperature should not exceed 150°C under worst case operating conditions and the average operating junction temperature should be no more than 110°C.

Since the worst case condition of all nine channels transmitting data was used for analysis, the maximum ambient air temperature, T_A, with no air flow should be:

$$T_{A(maximum)} = 150°C - 60.8°C$$

$$= 89.2°C$$

When evaluating the average operating junction temperature the effects of transmit/receive duty cycle communication port activity must be taken into account.

4.4. Driving the 'Wired-Or' SCSI Lines with the SN75LBC976

The control lines of the SCSI bus have three 'Wired-Or' lines, these are BSY (busy), RST (reset), and SEL (select). These lines are wired-or in that the line drivers connected to these lines drive in one direction (assertion) only and are tri-stated (high impedance) when negated. This allows numerous drivers to be active at the same time without affecting the logic state of the line and requires that all drivers be released or off before the logical state can change. When tri-stated the bus termination network passively negates the signal.

The technique used for wired-or operation with differential transceivers is to input the signal into the driver enable pin and connect the driver input to a fixed logic level input. When the input signal to the driver enable is active (high), the driver becomes enabled and the outputs drive the SCSI bus to the state of the driver input. When the input signal at the driver enable pin goes low, the driver turns off and allows the bus termination to negate the signal on the bus after all other drivers on the bus are also shut off.

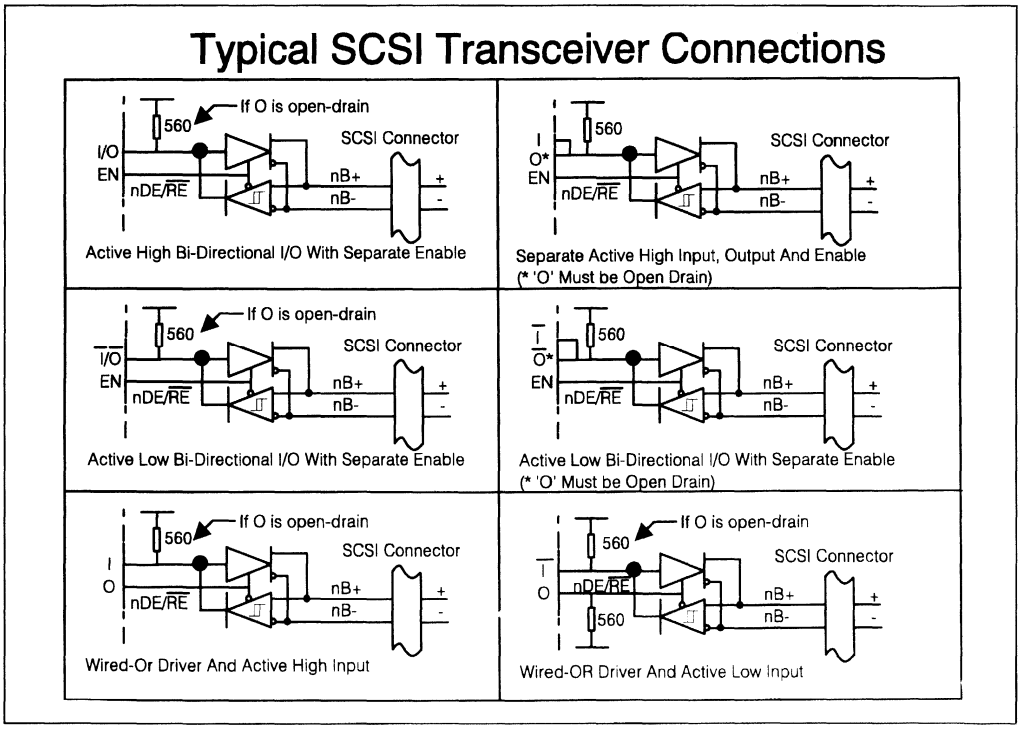


Figure 4.40 - Typical SCSI Transceiver Connections

Many communications controllers used for differential SCSI have separate inputs and outputs for these signals. When used with the SN75176 type RS-485 transceiver, these controller I/Os can be directly connected to separate driver enable inputs or receiver outputs. The SN75LBC976 device does not have a separate driver input and receiver input, these are tied together internally to save pins.

Controllers with separate I/Os can still be used with the 'LBC976 using the connections shown in figure 4.40. The controller output will go high and enable the driver and disable the receiver. Upon disabling the receiver, the external pull-up or pull-down resistor will drive pin A of the 'LBC976 to the proper level for bus assertion and the driver will assert the SCSI signal line. When the controller output goes low, the driver disables and allows the termination to negate the bus signal. After a short delay, the receiver outputs are enabled and will reflect the logical state of the bus signal.

5. Summary and Further Information

5.1. EIA Standards

For copies of the EIA standards please contact the Electronic Industries Association. For details and a copy of the Catalog of EIA & Jedec Standards & Engineering Publications contact the EIA Standard Sales office at the following address and telephone number:

EIA Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
United States
Telephone Number + 1 (202) 457-4966

5.2. References

The following books were invaluable in producing the Section on data transmission:

1. **Digital, Analog, and Data Communication** - William Sinnema & Tom McGovern - Prentice-Hall International - ISBN 0-835-91313-9.

2. **Data Transmission** - D. Tugal and O. Tugal - McGraw Hill - 1980

5.3. Texas Instruments - Completing the Picture

The range of products discussed throughout this section demonstrate the commitment made by Texas Instruments to the field of peripheral interfacing. Use of leadership technologies has enabled the production of high performance, reliable line drive/receive functions and highly integrated controllers.

Obviously in a seminar this short it is impossible to cover all TI's data transmission products. The reader is encouraged to contact a TI representative to obtain the latest data books on transmission ICs. As a minimum the designer should posses a copy of the Interface Circuits Data Book.

Finally, although we have discussed the older standards such as EIA-232 and RS-485 TI is continuing to work and participate in the various standard definition committees to ensure new and emerging

standards gain the full support of TI's semiconductor experience. Testimony to this fact has been the SN75LBC976 RS-485 transceiver, the specifications for which were closely aligned with the outcome of the work done by the SCSI-3 standards group.

Over the next 12 months TI will be releasing products in support of Futurebus+, and is actively supporting the P1394 high speed serial bus Working Group among others.

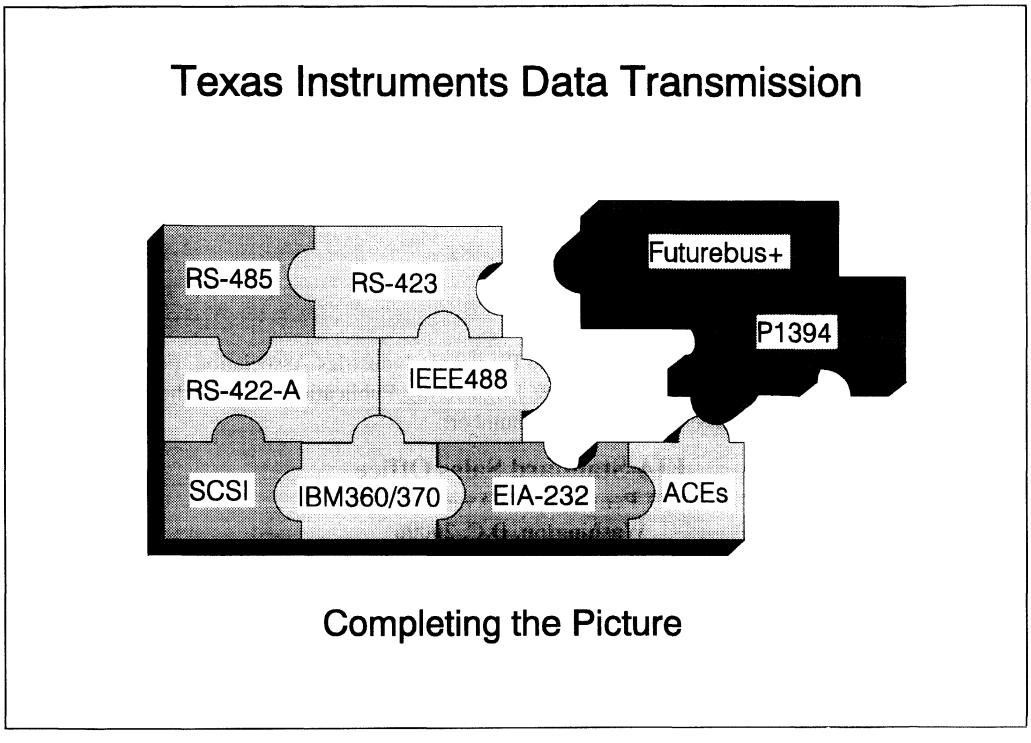


Figure 4.41 - Texas Instruments Data Transmission - Completing the Picture

Section 5
Power Drive Circuits

Section Contributions by:

Julie Holland
Charles Wray
Mick Maytum
Ross Hugo
David Cotton

Section 5
Contents

1. Introduction

1.1. Output Circuits

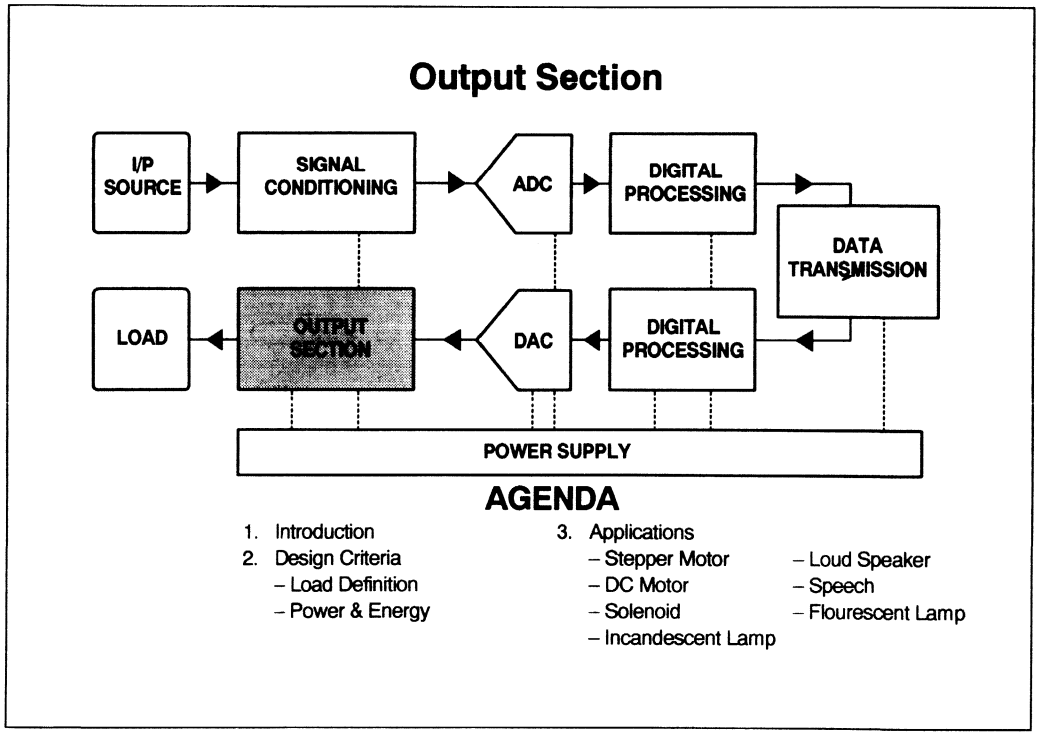


Figure 5.1.1 - Output Section

The output section of a control system serves as the interface between electrical control signals and the "real world". The end product of the output section is the control of a "real world" function such as motion, light, sound or any number of other physical actions. Control systems vary greatly in their complexity from controlling a simple single action to complex interactive systems with multiple feedback signals, fault isolation and adaptive software. Regardless of the system complexity an output system is normally employed to complete the interface between control system and the "real world" .

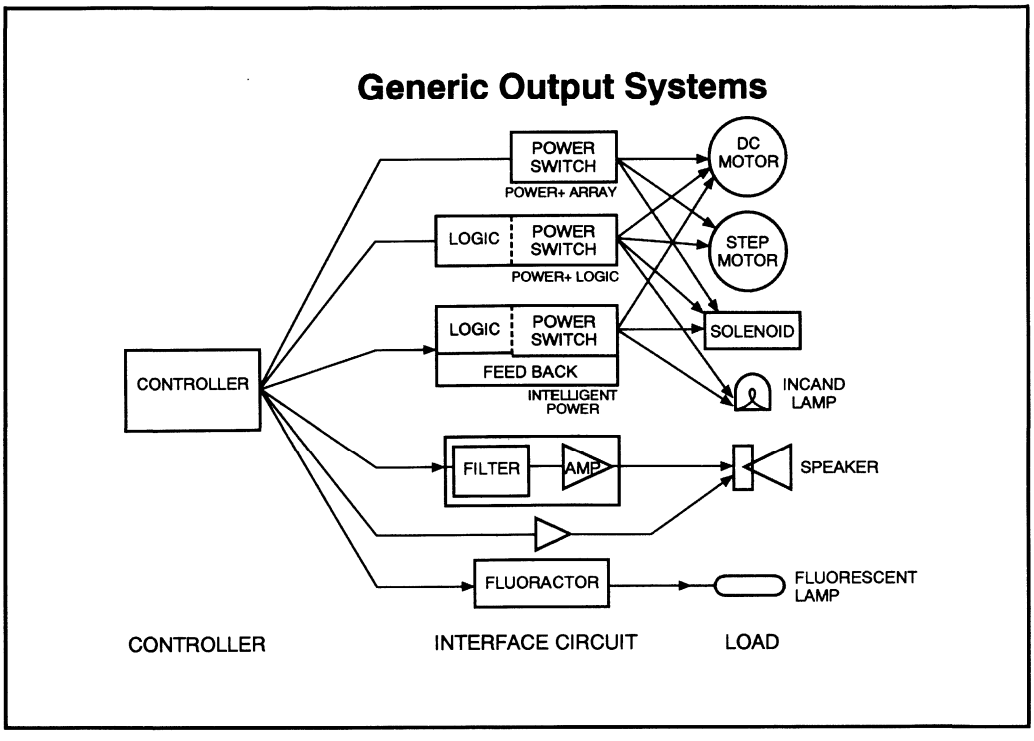


Figure 5.1.2 - Generic Output Systems

Figure 5.1.2 represents a generalized output system consisting of a controller, an interface circuit and a load. The design problem we are addressing is controlling the operation of a load with a small signal. Several typical loads such as motors, solenoids, speakers and lamps are shown. Notice that for most of the loads several signal paths exist from the controller through the interface circuits. Each path represents a solution to one specific design problem. Although multiple solutions exist they may not all be the best solution. The next section will discuss the methodology for designing an output system that is well suited for a particular application.

2. Output System Design

2.1. Selecting a load device

Selecting a Load

Energy Output	Load	Load Output Specifications
Rotating Motion		
Continuous	D.C. Motor	HP - Torque - RP
Incremental	Stepper Motor	Torque - Step Speed
Linear Motion	Solenoid	Ft-LBs - Inches
Light	Incandescent Lamp	Watts - Lumens
	Fluorescent Lamp	Watts - Lumens
Sound	Loudspeaker	Watts - Hertz

Figure 5.2.1 Selecting a Load

The first step is to select a load device. Selecting the load involves, defining the type of output energy needed, selecting the proper class of load, and selecting the correct size load. Figure 5.2.1 depicts some energy types with the corresponding load and output parameters. A dc motor for example will usually have an output specification that is in terms of torque at a given speed. Matching the mechanical requirements for a particular application is outside the scope of this discussion. We will assume that a suitable load can be selected.

The second step is evaluation of the input requirements for a particular load. Load input specifications address the voltage and current requirements during normal operation. Normal operation includes load switching (turn on, turn off and accompanying transients). Often the behavior of a load during switching is not adequately specified and must be characterized for the specific application. Understanding load input requirements will lead to the interface circuit requirements.

2.1.1. Interface Circuit Requirements

If we assume that the interface circuit is a switch then what do we need to know in order to select the right switch?

Motors, solenoids, lamps and other assorted loads are generally specified by operating voltage and current with a specified power output. The information provided is sufficient for operating at continuous duty, however in most applications the load is being switched on and off. When switching loads the operating requirements as well as transient conditions must be considered. The power requirements are often further influenced by dynamic operating conditions.

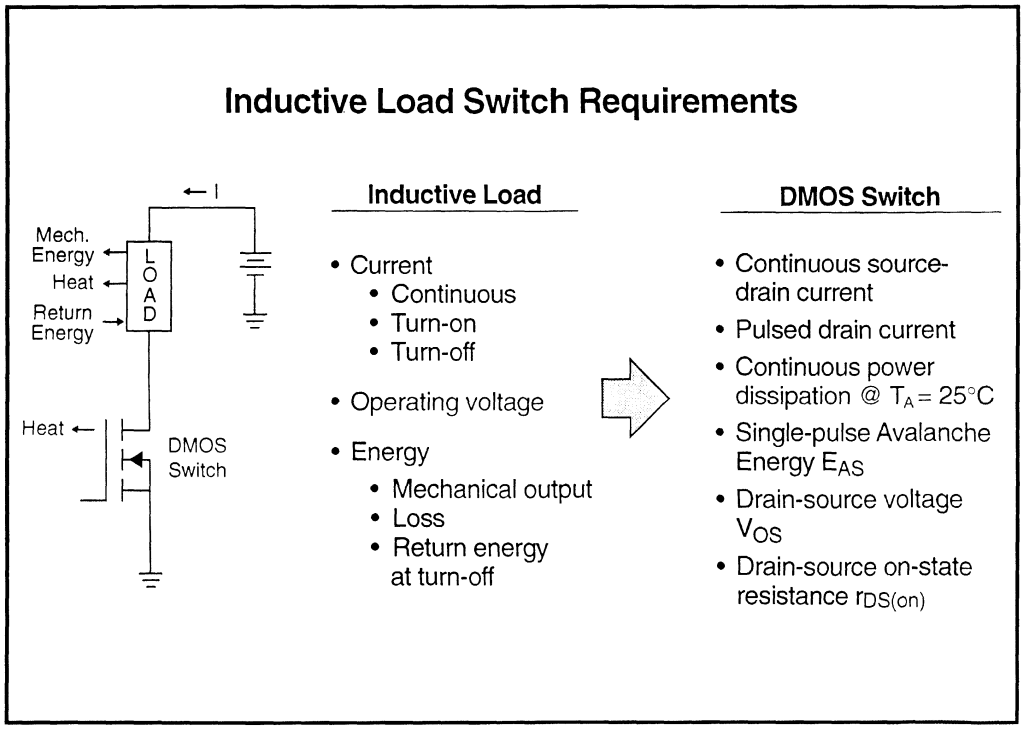


Figure 5.2.2 Inductive Load Switch Requirements

The easiest way to look at load requirements is to consider the example in Figure 5.2.2, of a load operating from a battery and controlled by a low-side switch. What is needed to design the switch and evaluate the system?

The system power supply and load choice will determine:

Current drawn from the battery, including transients when the switch is turned on and off

Battery terminal voltage. (V)

Energy output from the load (motion, sound, etc.)

Energy dissipated from the load in the form of heat. (IR loss, magnetic loss, friction)

Energy returned to system (inductive, regeneration, cross coupling)

These system load requirements must then be used to determine the switch requirements:

Continuous source-drain current

Pulsed drain current

Continuous power dissipation @ $T_A = 25°C$

Single-pulse avalanche energy (energy returned to the device from back e.m.f.)

Drain-source voltage (V_{DS})

Drain-source on-state resistance ($R_{DS(on)}$)

Selecting or designing a switch is a three step process, determine the total energy, current and voltage required, select a switching device which will accommodate the energy, evaluate the system power dissipation to determine any heat sinking requirements.

2.1.2. Determine Total Energy

Determining the total energy begins with evaluating load current during operation and switching.

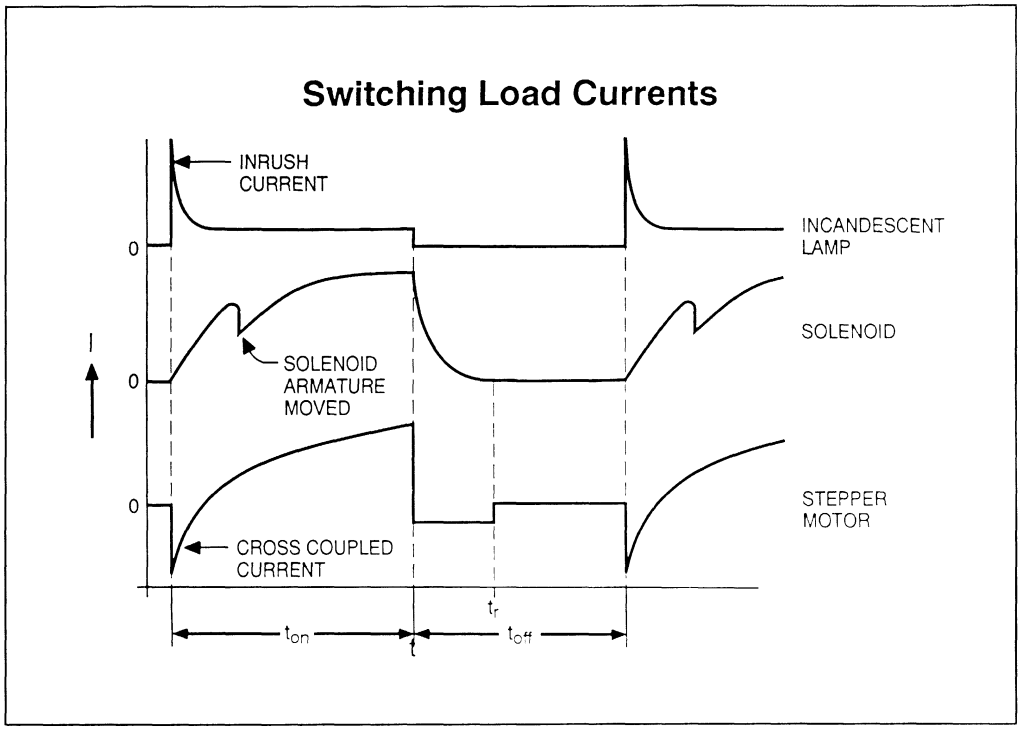


Figure 5.2.3 - Switching Load Currents

Figure 5.2.3 shows the current waveforms for an incandescent lamp, a solenoid and a stepper motor. This diagram depicts steady state and switching conditions which must be considered in controlling a load.

The incandescent lamp current shows, a high in rush at turn on (t_{on}) decreasing to a steady current value until turn off (t_{off}), and then a clean turn off with no current flowing after t_{off}. The high inrush is due to the difference in filament resistance when cold and hot. A lamp control switch will need to withstand high peak currents or limit the current until the lamp filament warms up.

The solenoid current increases starting at t_{on}, increases until t_{off}, and continues to flow until t_R. The change in current slope between t_{on} and t_{off} is caused by the solenoid armature moving closer to the coil and increasing the coil inductance. The current flow between t_{off} and t_R is a result of the magnetic field in the solenoid collapsing and returning energy to the system. A solenoid switch must be capable of conducting the coil operating current and the system must provide a method for accommodating the energy returned to the system at turn off. Several methods are employed to deal with the returned energy, which when it is dissipated in the switch is referred to as avalanche energy.

The stepper motor exhibits a exponential current increase characteristic of an inductive load. Return energy is a factor in stepper motor control. Additionally stepper motor windings can produce currents as a result of cross coupling from adjacent motor windings. A control circuit for a stepper motor such

as depicted in Figure 5.2.3 must accommodate the transient energy at turn on and the returned energy at turn off.

Once the load characteristics are determined energy calculations can proceed.

Energy and Power Calculations for an Inductive Load

- Power-on time MOSFET dissipation

$$P_{on} = \frac{1}{3} (I_p^2)\, r_{DS(on)}\, d$$

$$\text{For } \frac{L}{R_L} > t_{on}$$

- Back e.m.F energy

$$E_T = \frac{3\, L\, I_p^2 V_{CL}}{6\,(V_{CL} - V_{SS}) + 4 R_L I_{DM}}$$

- Power off dissipation

$$P_{off} = E_T f$$

- Total average switch power dissipation

$$P_T = (P_{on} + P_{off})n + P_{(quies)}$$

L = Load Inductance
I_p = Peak Drain Current
V_{CL} = Max Output Clamp Voltage
V_{SS} = Load Supply Voltage
R_L = Inductor Resistance
F = Switching Frequency
d = Duty Cycle (Ratio)
$r_{DS(on)}$ = Drain to Source on Resistance
n = Total Number of Switches Operating
$P_{(quies)}$ = Quiescent Power Dissipation of Switch Circuit
t_{on} = Switch On Time

Figure 5.2.4 - Energy and Power Calculations for Inductive Loads

The energy calculations for an inductive load are presented in Figure 5.2.4. The intent is to calculate the total power dissipated in the transistor switch.

Power dissipated during switch "on" time is calculated as follows:

During the power-on time the inductor's current approximates to a linear ramp, assuming the inductors L/R_L time constant is greater than the turn on time (t_{on}). This results in a mean square drain current of 1/3 I_P^2 with I_P equal to the peak drain current. Therefore the average power dissipated in the output MOSFET, P_{on}, is equal to:

$$P_{on(av)} = 1/3\,(I_P^2) * r_{DS(on)} * d$$

This assumption would be applicable to the stepper motor wave form in Figure 5.2.3, but would not work for the solenoid. The solenoid time constant L/R_L is less than t_{on}, therefore P_{on} will be greater than that calculated above.

Power dissipated during switch off time is calculated as follows:

When the output MOSFET is turned off, the back e.m.f. generated by the inductor raises the drain voltage, which must be clamped either externally or internally. External clamping is normally accomplished with a snubber diode. Internal clamping is also accomplished with a zener diode the clamp voltage V_{CL} is also called avalanche voltage.

The equation to define avalanche energy is:

$$E_T = \frac{\left(3 * L_H * I_P^{\,2} * V_{CL}\right)}{\left(6 * \left(V_{CL} - V_{SS}\right) + 4 * R_L * I_P\right)} \qquad \text{JEDEC Standard No. 10}$$

This equation assumes a linear decay of the current in the inductor. A more accurate calculation of E_T can be made by integrating the inductor current and clamp voltage in the load from turn off until the inductor current decays to zero as follows:

$$E_T = \int_0^{t_1} V_{CL} * I_L * dt$$

$$I_L = \left(I_P + \frac{\left(V_{CL} - V_{SS}\right)}{R_L}\right) * e^{-\frac{R_L}{L}t} - \frac{\left(V_{CL} - V_{SS}\right)}{R_L}$$

$$I_P = \frac{V_{SS}}{R_L} * \left(1 - e^{-\left(\frac{R_L}{L} * \frac{d}{f}\right)}\right)$$

$$t_1 = \frac{L}{R_L} * \ln\left[1 + \left(\frac{I_P * R_L}{\left(V_{CL} - V_{SS}\right)}\right)\right]$$

$$E_T = V_{CL} * \frac{L}{R_L} * \left(I_P - \frac{\left(V_{CL} - V_{SS}\right)}{R_L} * \ln\left[1 + \frac{I_P * R_L}{\left(V_{CL} - V_{SS}\right)}\right]\right)$$

The power dissipated during the turn-off period, P_{off}, can be equated to the product of E_T and the frequency of switching

$$P_{off} = E_T * f$$

Hence the total power, P_T, dissipated in an integrated switch with multiple output sections is:

$$P_{T(av)} = (P_{off} + P_{on}) * n + P_{(quies)}$$

This is the average power dissipation for multiple sections whose duty cycles have a fixed time relationship to each other. For multiple outputs with variable duty cycles the power calculation becomes more difficult.

Where, E_T = Total turn-off transient energy absorbed

f = Switching frequency

d = Duty cycle

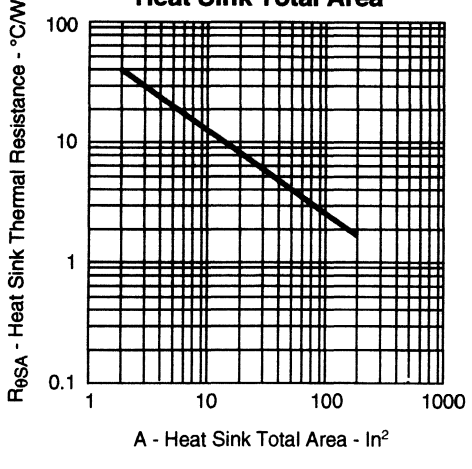
L	=	Load Inductance
I_P	=	Peak output load current
n	=	Number of output switches operating
P_{off}	=	Turn-off power dissipation in each switch
P_{on}	=	On-state power dissipation each switch
$P_{(quies)}$	=	Interface device bias power dissipation
$P_{T(av)}$	=	Average total power dissipation
R_L	=	Resistance of inductor
V_{CL}	=	Clamp voltage
V_{SS}	=	Load supply voltage

2.1.3. Thermal Considerations

With the device total power dissipation calculated now a thermal evaluation can proceed. The objective is to determine if external heat sinking will be required.

Thermal Consideration for Power Switches

Typical Heat Sink Thermal Resistance vs. Heat Sink Total Area



Max Power Dissipation

$$P_{MAX} = (T_{J(MAX)} - T_A)\, R_{\theta JA}$$

Thermal Resistance

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - \left| R_{\theta JC} + R_{\theta CS} \right|$$

Where:

$R_{\theta SA}$ = Heat sink-to-ambient thermal resistance, °C/W

$R_{\theta JC}$ = Device junction-to-case thermal resistance = 3.0°C/W

$R_{\theta CS}$ = Case-to-heat sink thermal resistance, °C/W = 0.5°C/W typical with thermal joint compound

$P_{T(AV)}$ = Total average power dissipation, W

T_J = Junction operating temperature, °C

T_A = Operating ambient temperature, °C-

Figure 5.2.5 - Thermal Considerations For Power Switches

The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature. The maximum power which can be dissipated in a device (P_D) can be determined as follows:

$$P_D = (T_J - T_A) / (R_{\theta JA})$$

Where,

T_J = Maximum device junction operating temp.

T_A = Maximum ambient operating temp.

$R_{\theta JA}$ = Junction to ambient thermal resistance, °C/W

T_J and $R_{\theta JA}$ are taken from the device specification and TA is determined by the application environment.

Is a heat sink required?

If the total power dissipated in the device PT exceeds the maximum power dissipation P_D then either a heat sink must be used or a different device must be selected.

A heat sink size can be determined by first calculating the required heat sink to ambient thermal resistance $R_{\theta SA}$ as follows:

$$R_{\theta SA} = [(T_J - T_A)/P_{T(AV)}] - [R_{\theta JC} + R_{\theta CS}]$$

Where,

$R_{\theta JC}$ = device junction to case thermal resistance

$R_{\theta CS}$ = case to heat sink thermal resistance, °C/W

= 0.5 /W typical with thermal joint compound

$P_{T (AV)}$ = total average power dissipation, W

T_J = junction operating temperature, °C (from data sheet)

T_A = operating ambient temperature, °C

The $R_{\theta SA}$ required can now be compared to heat sink design specifications to determine the design type and size required.

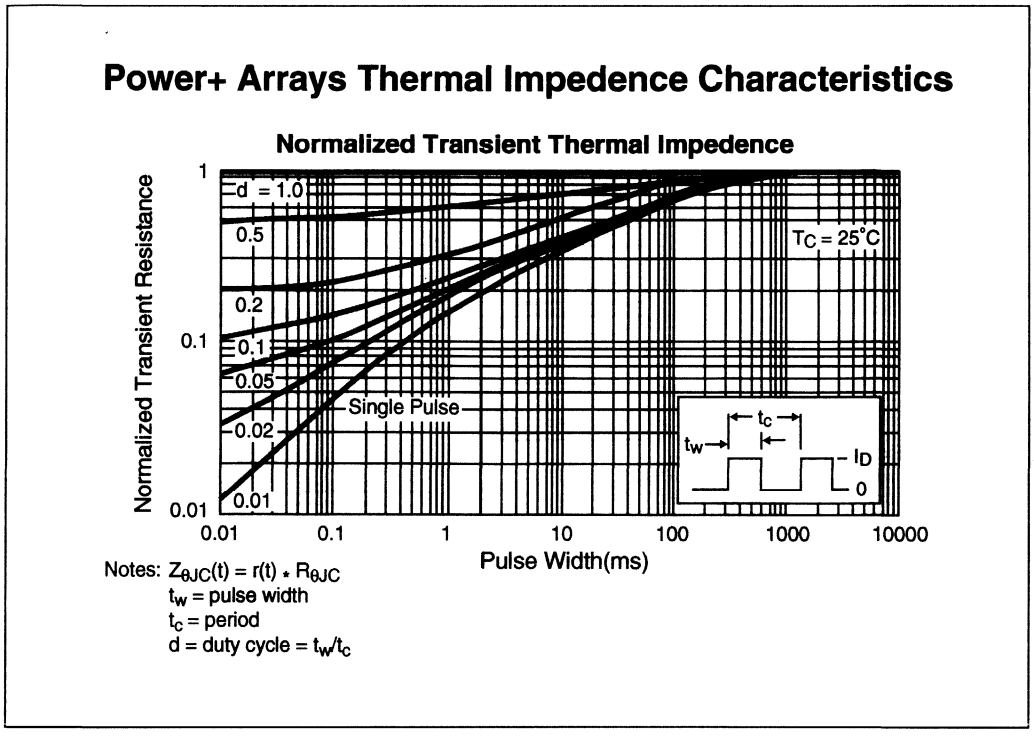


Figure 5.2.6 - Power+ Arrays Thermal Impedance Characteristics

The preceding thermal calculations were based on the assumption that the device average power was duty cycle dependent. This is true if the pulse widths are short in relation to the device thermal time constant. An example would be a switch that is "on" for one hour in every twenty four hours. the actual duty cycle is low but your system must be designed to accommodate 100% on time for the switch. The graph in Figure 5.2.6 gives the times associated with the Power+ Arrays.

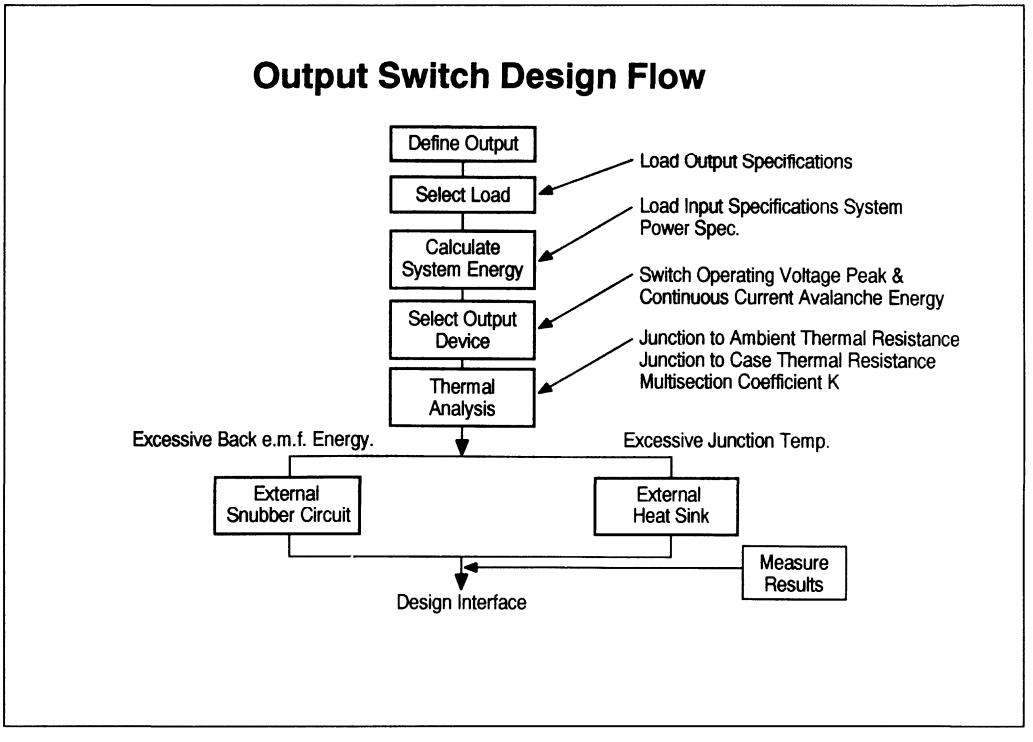


Figure 5.2.7 - Output Switch Design Flow

2.1.4. Conclusion

Summarizing the process, defining the requirements leads to selection of a load based on the load output specifications. System energy can then be calculated based on the load characteristics, and load input specifications along with some switch assumptions. A switch device can then be selected on peak and average power and energy calculations. A thermal analysis based on the selected device thermal specifications will determine if additional heat sinking and external circuitry for back e.m.f. energy dissipation will be required.

The design of the switch section will be completed when actual measurements from the system are used to verify the design.

3. Stepper Motor Application

3.1. Introduction

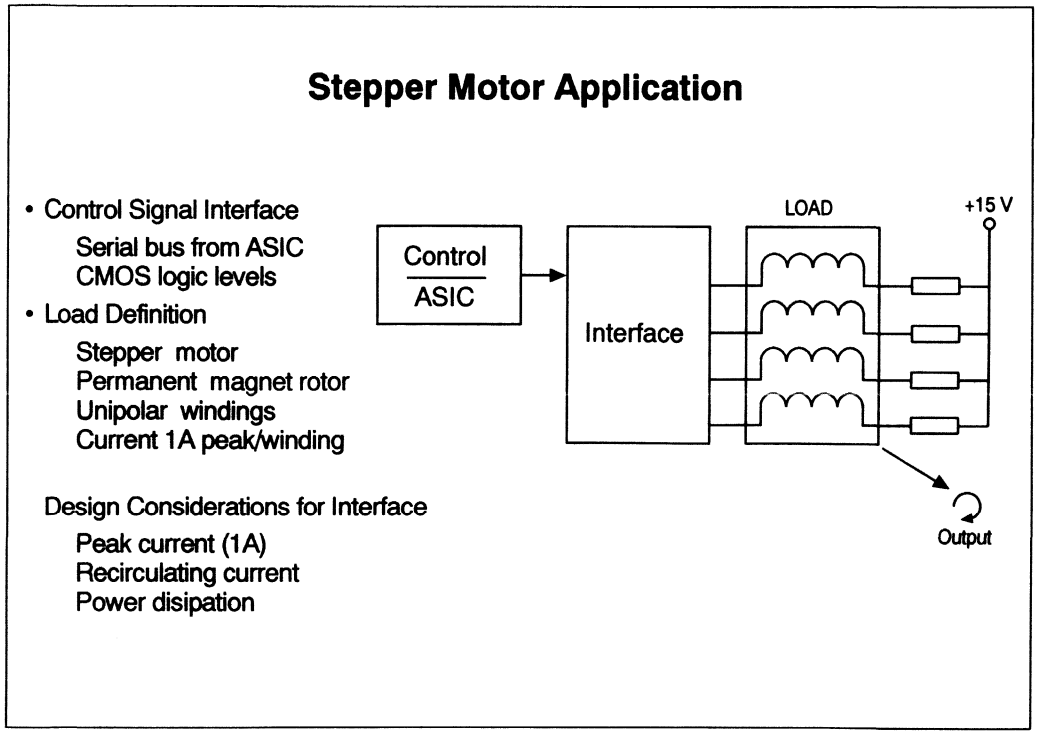


Figure 5.3.1 - Stepper Motor Application

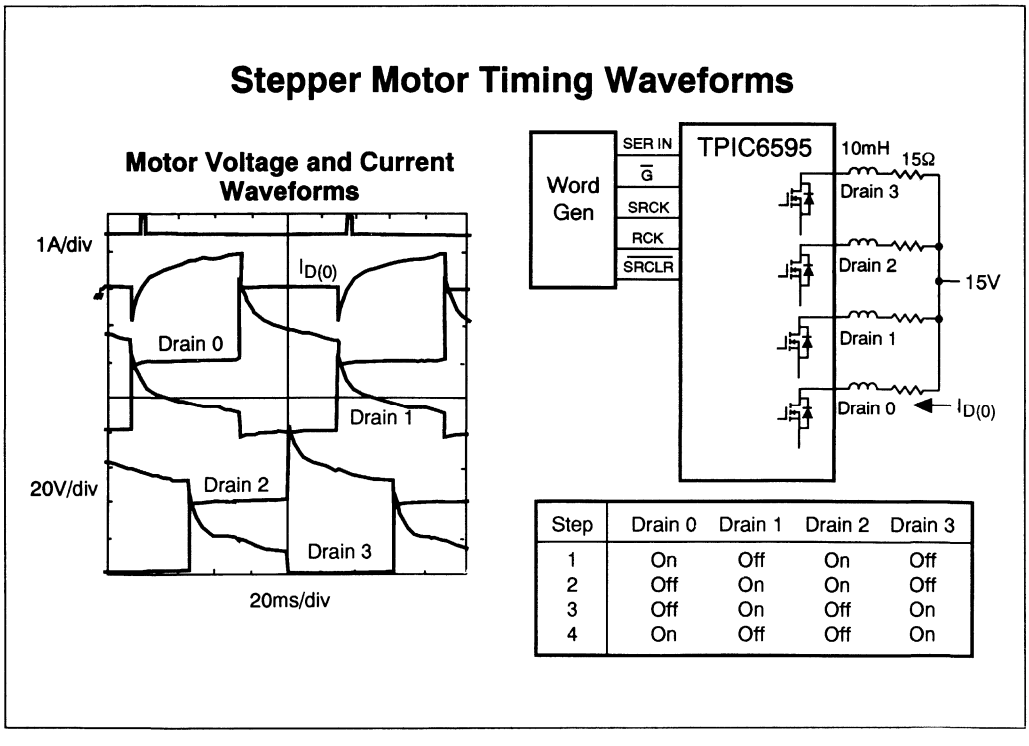
Stepper motors are often chosen to provide incremental rotating motion. Some typical applications are printers, copiers, and industrial robots. Stepper motors present a multiple phase inductive load to the output circuit.

Figure 5.3.1 shows a block diagram of the application. The motor chosen has unipolar windings which require a peak current of 1 A.

3.2. Load Description:

The first consideration in designing this application is to consider the load which in this case is a Superior Electric stepper motor. The permanent magnet rotor stepping motor has two forms of stator winding: bipolar and unipolar.

The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by interface devices with open-drain outputs. The motor chosen for this application has unipolar windings. Due to the manner in which the windings are constructed when one winding is turned off a back e.m.f. voltage will be induced both in the winding that was turned off and in the other bifilar winding.



Step	Drain 0	Drain 1	Drain 2	Drain 3
1	On	Off	On	Off
2	Off	On	On	Off
3	Off	On	Off	On
4	On	Off	Off	On

Figure 5.3.2 - Stepper Motor Timing Waveforms

3.3. Energy Calculations

Figure 5.3.2 shows a timing wave form of the stepping motor. The table in the lower right section shows the winding switching sequence. Additionally we can see that at any step two windings will be energized. With the knowledge that the windings are driven two at a time and by observation of the current wave form we can begin energy calculations. The value of back e.m.f. energy will remain the same as if it were all returned to one winding.

Observation of the timing diagram indicates t_{on} = 5 ms and that the winding current approximates a linear ramp ($L/R > t_{on}$). This indicates that the simplified formula will be a good approximation.

Therefore:

$$P_{on} = 1/3 (I_P^2) * r_{DS(on)} * d$$

Where, $d = 0.5$ (each winding conducts twice in the four step cycle)

Note that in this example if the motor is stopped the current through each winding will be a steady 1 A. This brings up an important point. The power calculations are based on an assumed operating frequency. If the motor is stopped the individual drive currents may exceed the maximum continuous current rating of the switches. When calculating energy and power worst-case assumptions must be considered.

3.4. Choosing an Interface Circuit

Figure 5.3.2 shows a TPIC6595 has been chosen for this application. This device was chosen because it can meet the power requirements, can drive all four windings from a single integrated circuit, and includes interface logic.

Figure 5.3.2 shows the TPIC6595 driving the stepper motor. The motor is driven at its rated 1 A by operating two output DMOS transistors in parallel. In Figure 5.3.2, drain 0 is representative of output transistors 1 and 5 in parallel. Similarly, drain 1 is representative of output transistors 2 and 6, etc. Anti-parallel source-drain diodes are omitted for clarity. In this example, the input logic which would normally be provided by the system's microprocessor is provided by a Hewlett Packard HP8180A data generator.

The antiparallel diodes are used to recirculate the current that is induced in the winding when the current through the previously activated winding on the pole is terminated. Hence, during each motor revolution both positive and negative current flows through the power switches which control the winding.

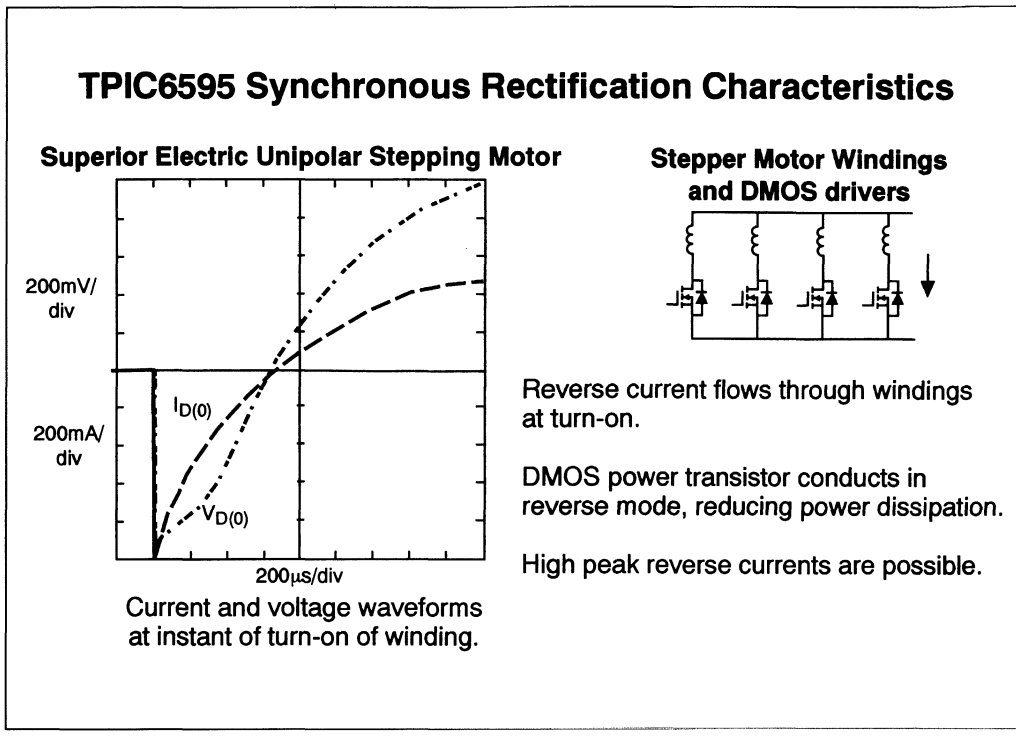


Figure 5.3.3 - TPIC6595 Synchronous Rectification Characteristics

Two features of the Power+ Logic DMOS output structure enhance the performance of the outputs when switching inductive loads as in the previous stepper motor example. Figure 5.3.3 shows an expansion of the wave forms of the negative current region of the winding pulse from the stepper motor application.

As previously mentioned, the anti-parallel diodes of the DMOS output allow the recirculation of current at winding turn-on. It is the anti-parallel diode which allows the DMOS output to withstand high peak reverse currents. In contrast, a power bipolar structure does not benefit from an inherent anti-parallel diode; one must be physically added, either to the integrated circuit design, or externally at the board level. If negative currents are required of a bipolar power switch which does not include such as diode, parasitic isolation diodes in the bipolar structure will conduct which may cause system malfunction. It is for this reason that a DMOS solution is often the most practical and economical for motor drive applications.

Returning to the stepper motor example, as the winding turns on, the voltage drop across the output decreases. Once the voltage drop across the output ceases to be at least 0.7 V, the body drain diode no longer conducts. At this point, the DMOS power transistor turns on in the reverse direction, allowing continued negative current flow to the inductor.

Once reverse conduction through the DMOS becomes the vehicle for negative current flow to the inductor, the power dissipation is given by the product of $r_{DS(on)}$ and the square of the drain current. Reverse conduction continues through the DMOS transistor until the current reaches zero.

3.5. Why choose a Power+ Logic device for an application

The DMOS output structure is power efficient..

The output structure can withstand high avalanche energy.

System design is simpler than with discrete DMOS or bipolar transistors.

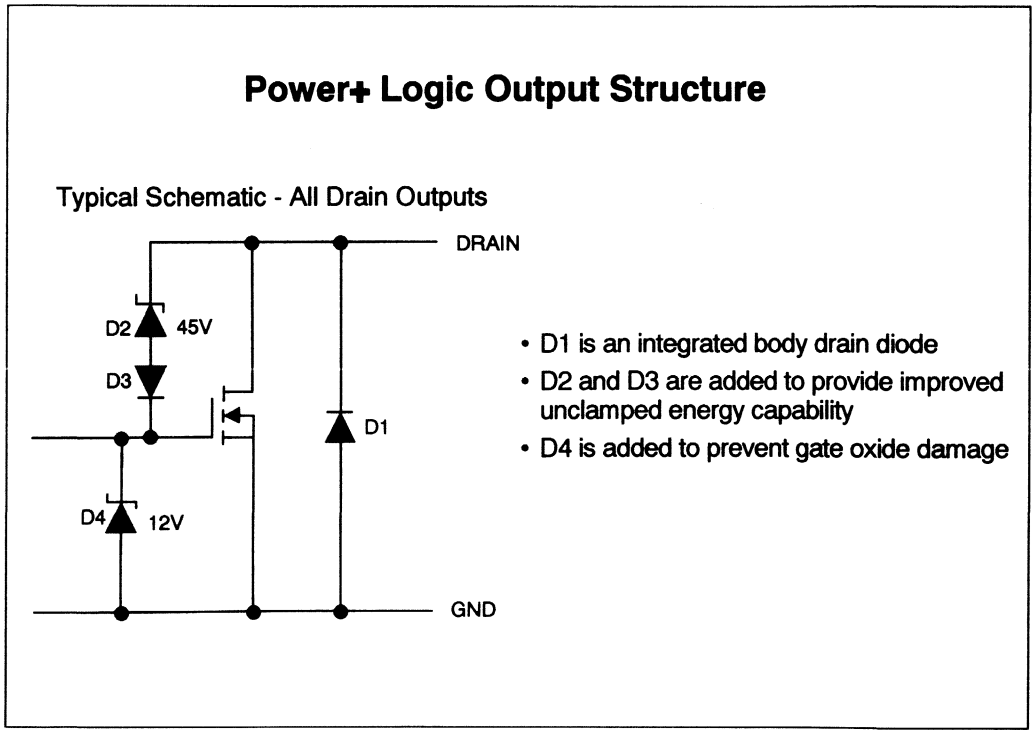


Figure 5.3.4 - Power+ Logic Output Structure

The TPIC6595 device has 8 power DMOS outputs with built-in 45-V voltage clamps for enhanced inductive energy switching capability. When switching inductive loads, high voltage transients are seen at the device output when the output is placed in a high impedance state. The voltage generated by the inductive transient is limited by the breakdown mechanism of the output structure.

For the Power+ Logic devices, the internal dynamic 45-V clamp circuit will eventually conduct during switching of an unclamped inductive load, allowing current to charge up the gate of the DMOS. Once

the DMOS gate voltage exceeds the threshold voltage of the device, the DMOS turns back on, completely dissipating the energy from the inductor. Thus, the entire active area of the DMOS transistor is used in the forward bias mode to absorb energy from the inductive load. Without the internal clamp circuitry, the device output would be driven into avalanche breakdown, and would operate in the much lower energy capability reverse bias mode. The built-in voltage clamps of the Power+ Logic devices allow the user to switch up to 75 mJ of avalanche energy without the use of external snubber circuitry.

Each DMOS output of the TPIC6595 can provide 250 mA of continuous current with all outputs turned on. Individually, the outputs can be pulsed to provide up to 1.5 A of current. Or, multiple outputs can be paralleled for increased current drive of up to 6 A of pulsed total load current. This rating is sufficient to drive the stepper motor when operating at the described duty cycle.

3.5.1. Avalanche Energy Capability

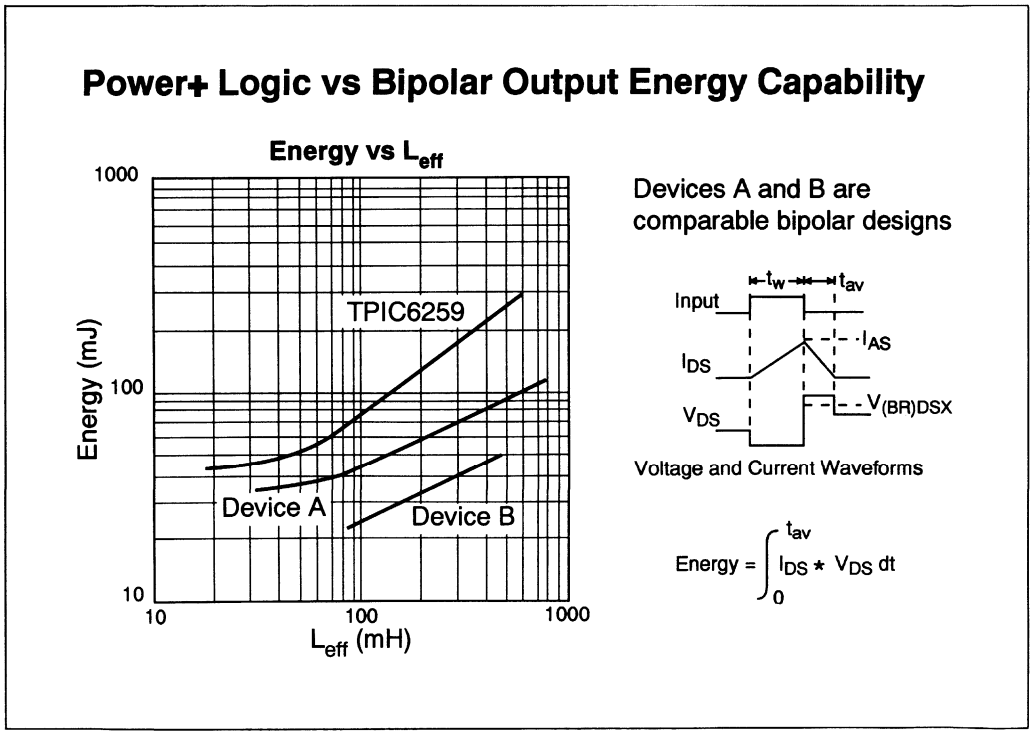


Figure 5.3.5 - Power Logic vs. Bipolar Output Energy

In describing the ruggedness of any power output, a key parameter is the avalanche energy capability. When the maximum energy capability is determined by thermal limitations of the silicon, the energy that can be dissipated during avalanche is not a constant, but varies with peak switching current and load inductance. Some power structures, however, may be prematurely limited by secondary breakdown and will have a constant energy rating. For an inductive switching pulse within the energy

capability of the device, the energy dissipated in the output is proportional to the product of the current and voltage wave forms.

Figure 5.3.5 benchmarks the ruggedness of the Power+ Logic devices against two low side bipolar devices having comparable voltage capability. Device A has a breakdown voltage of 37 V, while device B has a breakdown voltage of 50 V. Each bipolar device has approximately twice the output active area as the Power+ Logic devices. The data in the figure reflects the last point of output survival just prior to its destruction.

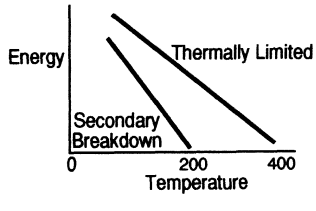
It is evident that the Power+ Logic DMOS device is much more rugged that either of the bipolar structures. While switching a 350 mH inductor, the TPIC6259 dissipates 200 mJ prior to destruction, more than twice the energy of the bipolar devices. Note that while the energy capability of the Power+ Logic devices decrease to 45 mJ while switching a 30 mH load, this is still significantly more than comparable bipolar devices.

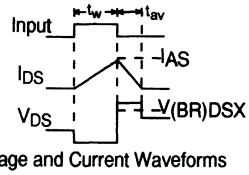
3.5.2. Power+ Logic Energy Capabilities

Unclamped Inductive Switching Test Data

Maximum Energy Capability Prior to Device Destruction
T_j = Starting Junction Temperature = 25 °C

Device Type	I_{AS} (A)	t_{av} (ms)	V_{DSX} (V)	V_{DD} (V)	L_{eff} (mH)	L (mH)	E (mJ)	P_o (W)	K	T_m (°C)	T_{jpk} (°C)
DMOS	2.1	0.8	50	15.1	19	13.2	42.2	105.5	269.0	378	403
TPIC6259	1.7	1.4	50	15.1	42	29.4	58.1	83.0	269.0	394	419
Bipolar	1.3	1.5	37	9.0	41	30.7	35.4	48.8	139.5	122	147
Device A	0.9	2.6	37	12.8	101	66.3	43.9	34.4	139.5	114	139
	0.8	5.0	37	19.0	247	120.0	69.4	27.8	139.5	129	154
Bipolar	0.8	1.3	50	11.6	80	61.4	25.6	40.0	139.5	94	119
Device B	0.7	1.8	50	9.5	125	101.0	30.6	35.0	139.5	96	121
	0.5	3.4	50	15.0	335	335.0	41.9	25.0	139.5	95	120





Voltage and Current Waveforms

$$\text{Energy} = \int_0^{t_{av}} I_{DS} * V_{DS}\, dt$$

Figure 5.3.6 - Unclamped Inductive Switching Test Data

In addition to peak switching current and load inductance, the energy capability of a power device varies with temperature. As the junction temperature of the device increases, energy capability decreases. This temperature-energy relationship was exploited to further understand the avalanche energy capabilities of the Power+ Logic devices.

Unclamped inductive switching tests were performed on the Power+ Logic devices in which the junction temperature of the DMOS output was gradually raised by forcing the device to dissipate increasingly large amounts of energy. The virtual junction temperature of the device immediately prior to destruction was calculated. Note that for the purposes of these tests, the 150°C maximum junction temperature specification of the Power+ Logic devices was violated; these tests do not reflect recommended operation of the Power+ Logic devices.

Assuming mechanical limitations of the package are disregarded, the maximum avalanche energy capability of a power device operating in the forward bias mode is limited by the thermal capabilities of silicon. However, the actual avalanche energy dissipated by a given power structure may be prematurely limited by a secondary breakdown mechanism. In the case of the Power+ Logic outputs, the absence of forward secondary breakdown can be shown. The calculated virtual junction temperature of the Power+ Logic output structure at the point of device destruction was greater than 400°C. Since silicon is thermally limited at approximately 400°C, silicon thermal limitations were the probable cause of device destruction.

For comparison, similar tests were performed on the bipolar devices A and B. Bipolar device B (50 V clamp) had a calculated maximum virtual temperature of approximately 120°C immediately prior to destruction, clearly illustrating a secondary breakdown limitation. Bipolar device A (37 V clamp) had improved characteristics, but still clearly experienced secondary breakdown limitations with destruction temperatures ranging from approximately 140°C to 150°C.

The following terms and definitions apply to Figure 5.3.6:

I_{as} = Peak current reached during device avalanche

t_{av} = Time duration of device in avalanche

L = Load inductance

L_{eff} = Effective load inductance; accounts for supply voltage

E = Energy absorbed by device under test $L_{eff} \times I_{as}^{2}/2$

V_{dd} = Output supply voltage

V_{dsx} = Effective device avalanche voltage

T_c = Case temperature

T_M = Maximum junction rise which occurs in inductive switching

P_o = Power = $I_{as} \times V_{dsx}$

K = 139.5 = A thermal constant where the area of active silicon = 1k mils square.

= $2/(A(p\ kc)^{1/2})$

Where, A = Area of power generation silicon

p = density of silicon

k = thermal conductivity of silicon

c = thermal capacity of silicon

T_M = $(2^{0.5})/3\ Po\ k(tav)^{0.5}$

T_{JPK} = Peak junction temperature at point of destruction
= $T_M + T_C$

3.5.3. Low Quiescent Currents

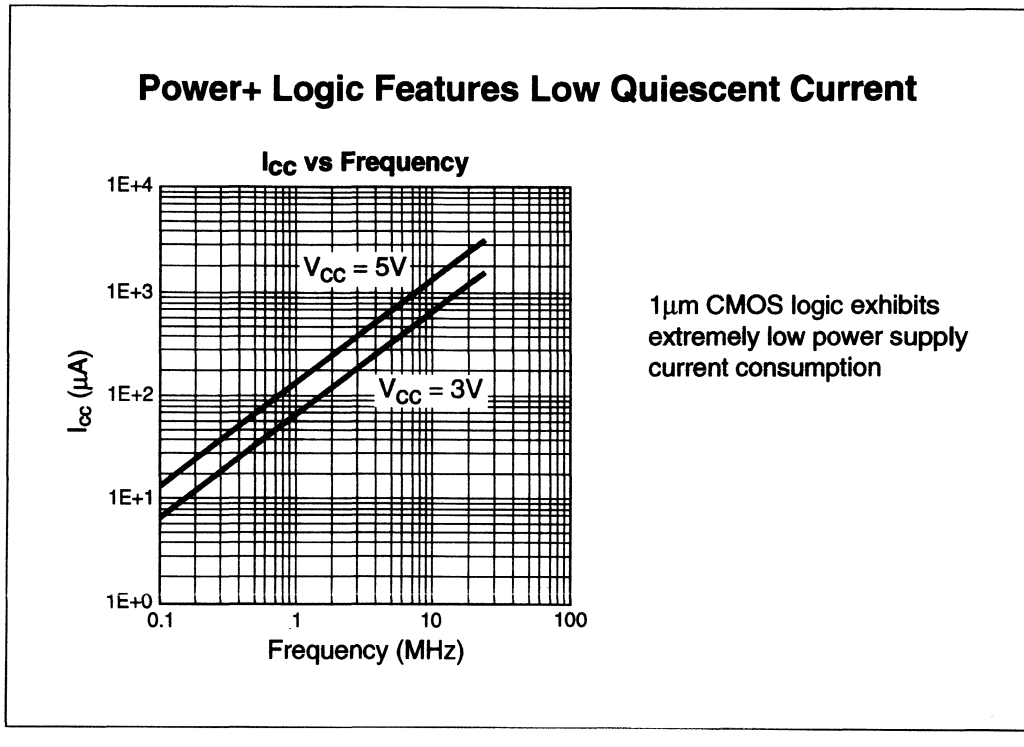


Figure 5.3.7 - Power+ Logic Features Low Quiescent Current

The Power+ Logic devices integrate performance power output structures with high-density sub micron CMOS logic. Figure 5.3.7 shows I_{CC} versus SRCK frequency for the TPIC6595 with the outputs static and an alternating bit pattern on the SER IN pin. This example demonstrates the high logic frequency capability of the Power+ Logic devices, as well as the low V_{CC} power consumption. A high logic speed capability allows the information to be transferred from the microprocessor interface very quickly even though the switch and load operation occurs at a much slower repetition rate. This would especially be important when cascading several devices for a large number of outputs all controlled be a single serial interface.

The power described in this graph is the term P_{quies} used in calculating the total average power dissipated in a device.

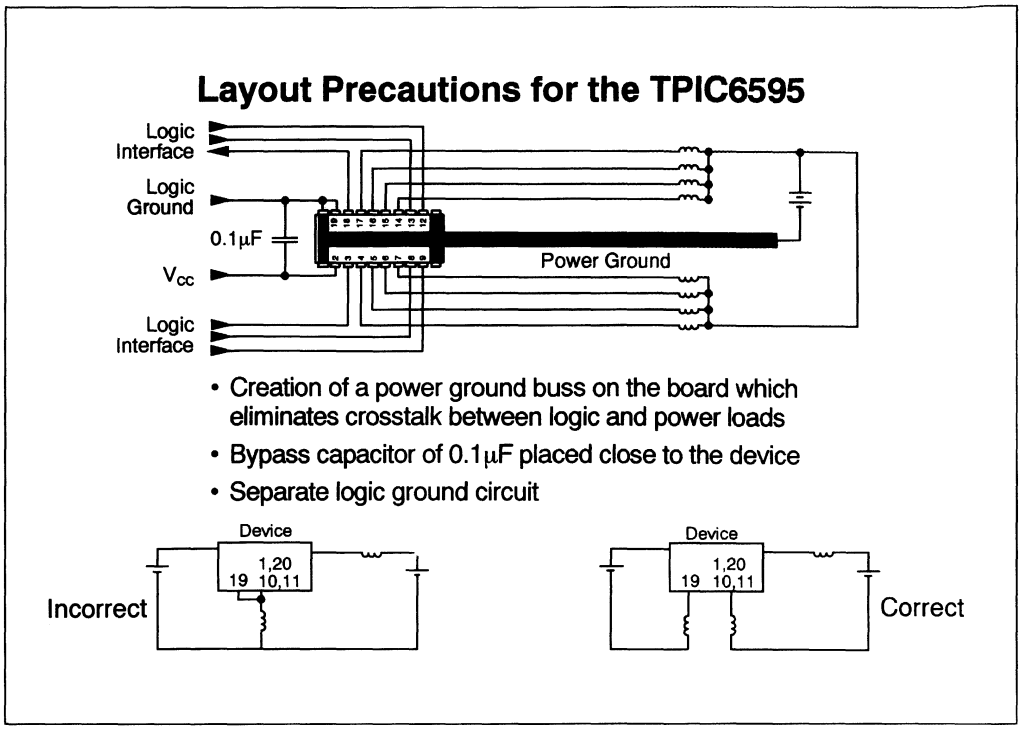


Figure 5.3.8 - Layout Precautions for the TPIC6595

When using the TPIC6595, or any of the Power+ Logic devices, there are several PCB layout considerations which should be kept in mind. High frequency layout rules should be used when designing power switching systems as mutual inductance (i.e. capacitance between the drive circuit and load circuit) can cause coupling of erroneous signals resulting in false operation. The following precautions are offered:

Use of a power ground bus on the PCB to eliminate crosstalk between the power loads and input logic.

Addition of a 0.1 μF bypass capacitor between V_{CC} and the logic ground line, placed close to the device to dampen any stray signals experienced by the drive circuit.

Separate power and logic ground circuits.

Figure 5.3.8 shows an example implementation of these board layout considerations using the TPIC6595.

4. Bi-directional Motor Drive Application

4.1. DC Motors

DC motors play an important role in a wide variety of electronic systems. Efficient control of motor speed and torque is an important issue for many system designers.

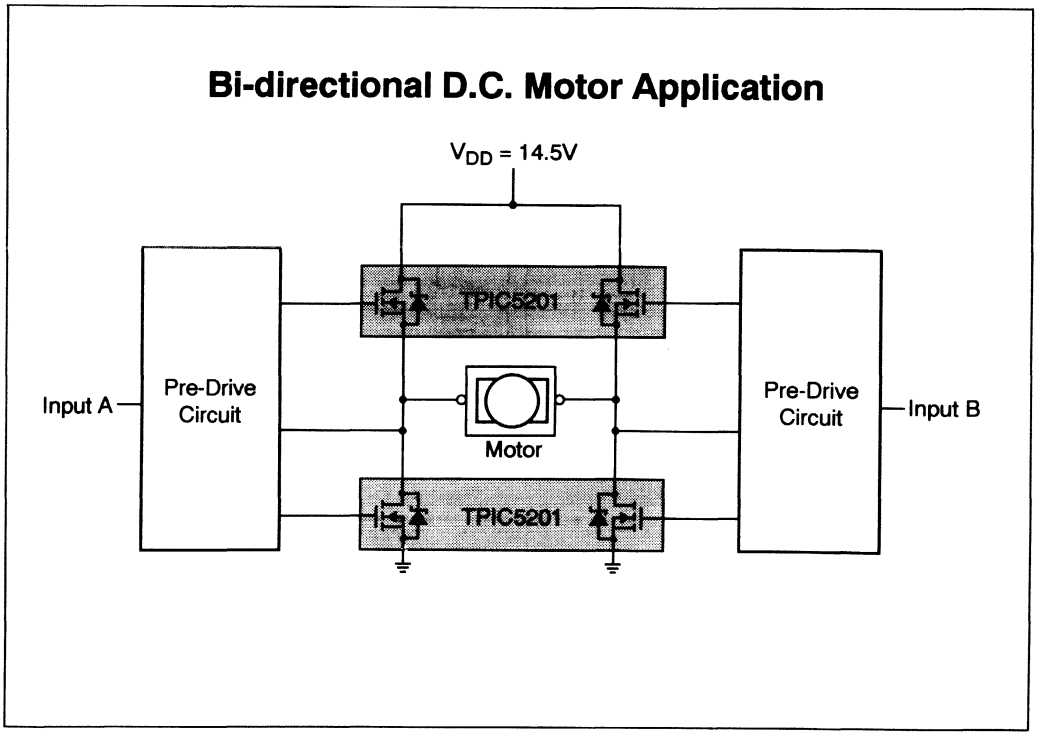


Figure 5.4.1 - Bi-directional DC Motor Drive

Figure 5.4.1 shows a bi-directional DC motor being driven from a 14.5-V supply by two dual DMOS switch devices arranged in a full H-bridge configuration. This circuit uses 20 kHz PWM input signals that are 180 degrees out of phase. In most systems, these signals would be supplied by a micro

controller. A 50% duty cycle on both input signals produces a net zero voltage across the motor, creating a stall condition. Control of the motor's speed and direction of rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net dc voltage across the motor, providing the drive current needed to meet the torque requirements of the motor.

4.2. Motor Operation

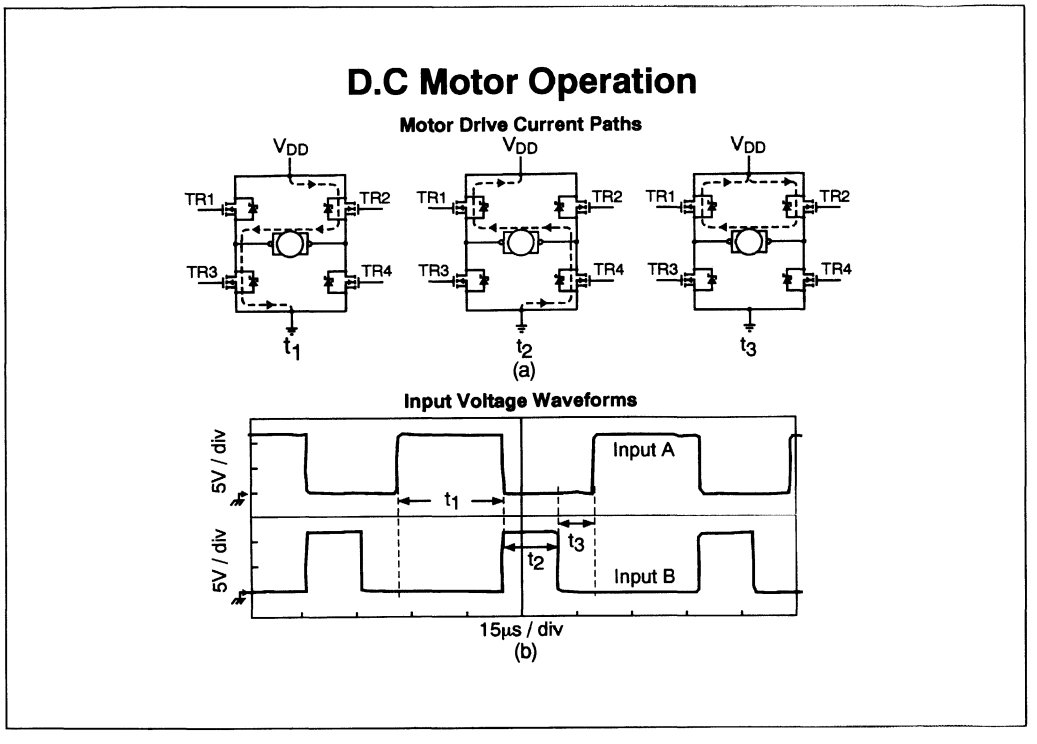


Figure 5.4.2 - Motor Operation

Motor operation is shown in Figure 5.4.2. In this example, the motor is driven in the forward direction, and the motor speed is controlled by varying the duty cycle of input signal B. While input signal A is high and input signal B is low, there is a net negative voltage across the terminals of the motor and current through the motor ramps up. Once input A goes low, a net positive voltage appears across the motor terminals and the motor current ramps down. When both input signals are low, there is no net voltage across the motor terminals, and the H-bridge recirculates a relatively constant current through its upper stages. To drive the motor in the reverse direction, input signal B is held to a 50% duty cycle, while the duty cycle of input A is varied.

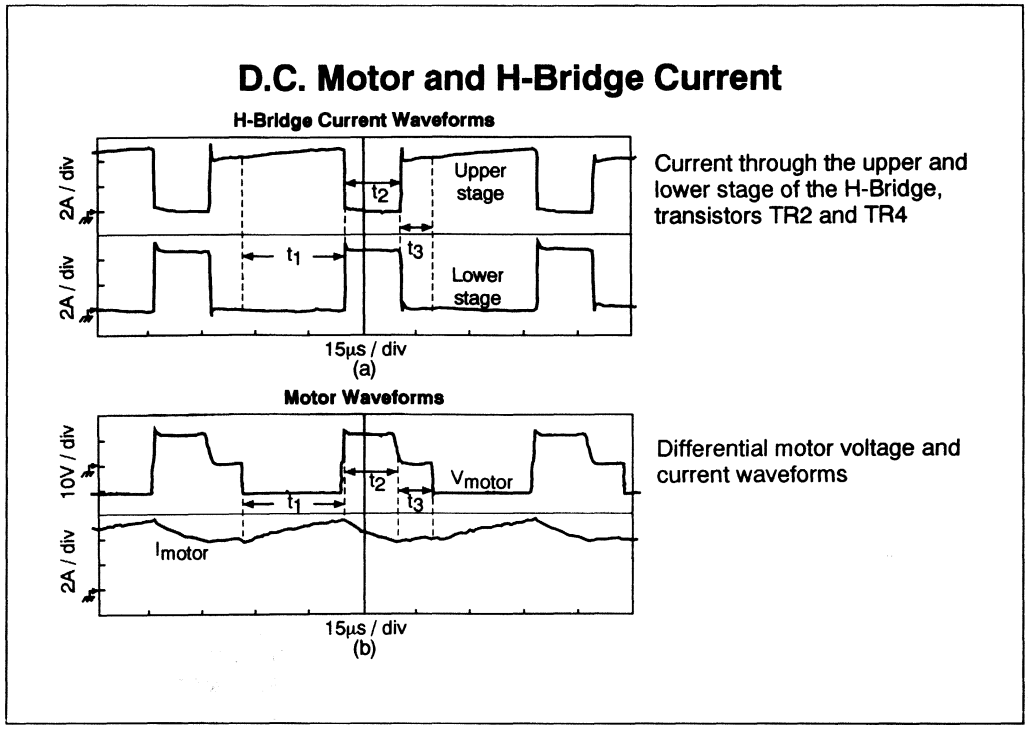


Figure 5.4.3 - Motor and H-Bridge Currents

Figure 5.4.3(a) shows the current through the transistors on one side of the H-bridge during time periods t_1, t_2, and t_3. Operation of the other side of the H-Bridge is similar.

Figure 5.4.3(b) shows the motor voltage and currents during the same time periods.

In this example, the pulse width of the input signal is approximately 25 µs at a 50% duty cycle. It is important to note that when switching both the upper and lower transistors on the same side of the H-bridge, a brief delay must occur to allow the conducting transistor to turn off before the non-conducting transistor is allowed to turn on. Without this delay, excessive cross conduction current may result. Cross conduction is a condition in which the upper and lower FETs on one side of the H-bridge are on simultaneously, providing a low impedance path between the source voltage and ground. While small cross conductance currents can actually be used to enhance system performance, uncontrolled cross conduction can result in excessive heat dissipation and degradation of the device.

4.3. System Power Considerations

The motor drive current shown in Figure 5.4.3(b) has a peak value of slightly less than 6 A with a minimum value of 4 A. Energy calculations must be based on the condition when one of the input signals is at the minimum duty cycle. The motor current during time t_3 is due to back e.m.f. and must be included in power dissipation calculations.

4.4. Choosing an Output Switch

The device required for this application must be capable of conducting at least 5 A continuous and as shown in the previous diagrams must be configured in an H-Bridge.

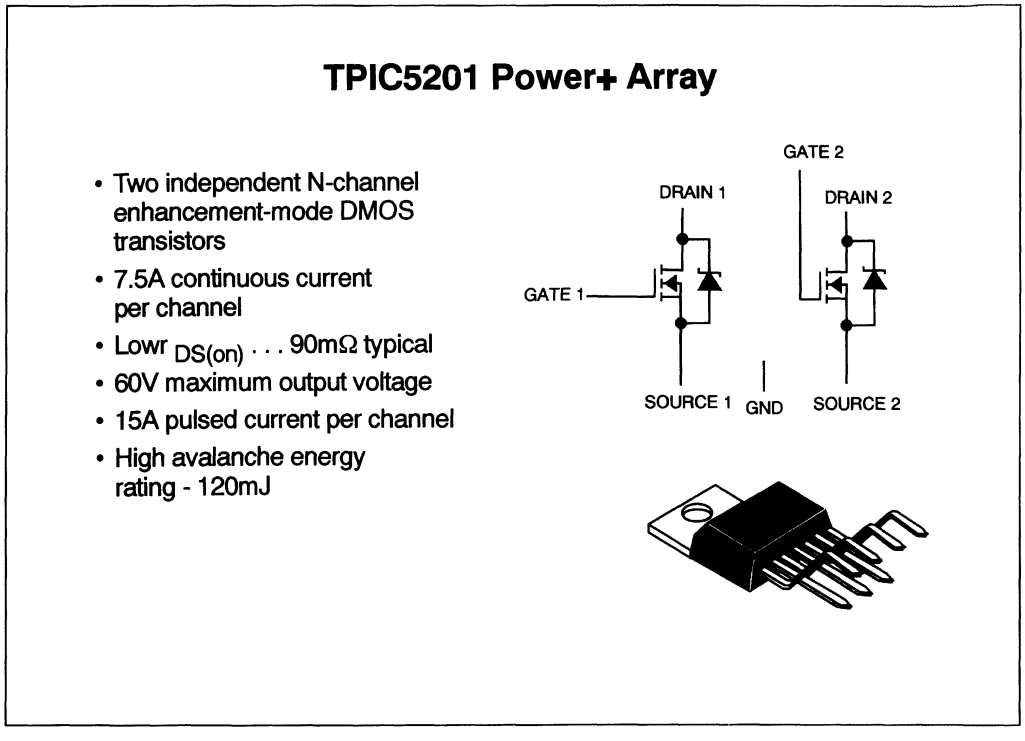


Figure 5.4.4 - TPIC5201 Power+ Array

The device chosen for this application is a TPIC5201 Power+ Array. This device contains two uncommitted high performance DMOS transistors in a single power package. The uncommitted transistors allow for an H-Bridge configuration. The low $r_{DS(on)}$ minimizes the device dissipation.

4.5. Pre-Drive Circuit

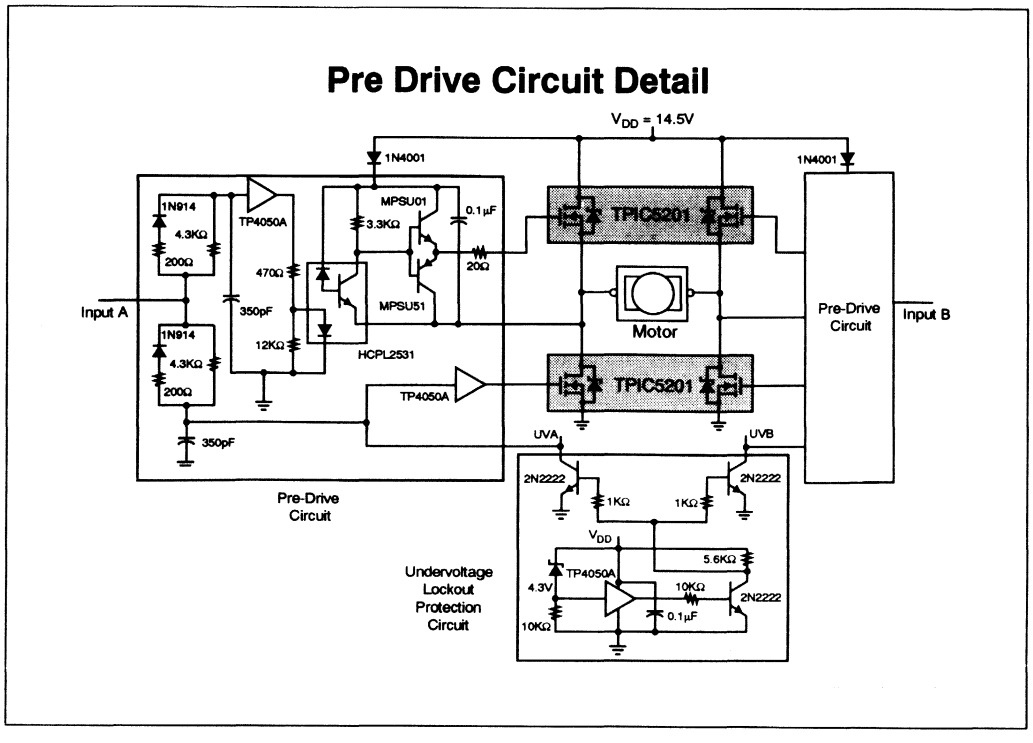


Figure 5.4.5 - Pre-drive Circuit Detail

In this application, two symmetrical pre-drive circuits are used to drive the gates of the upper and lower FETs. The pre-drive circuit schematic is shown in Figure 5.4.5. Drive to the upper transistors is achieved through the use of an HCPL2531 optocoupler followed by an emitter-follower stage. The high speed optocoupler isolates and level shifts the upper stage FETs from the input, while providing a reference to ground. The emitter-follower provides low impedance drive for fast charging of the intrinsic gate-source capacitor to enhance switching times.

A 0.1 μF bootstrap capacitor is used to allow the gates of the upper FETs to rise above the supply voltage rail. The bootstrap must be at least 10 times larger than the parasitic gate capacitance of the TPIC5201, typically 18 nF. Inclusion of the emitter-follower and the bootstrap capacitor allow the upper transistors to be turned on hard when the input signal transitions high.

The low gate capacitance of the TPIC5201 allows for improved efficiency in the motor control circuit. In a power switching application, as the switching frequency increases, switching losses due to the continuous charge and discharge of the gate capacitor become the dominating component of the power loss. By minimizing typical gate capacitance, the TPIC5201 reduces switching losses, which results in reduced system power consumption, and improved system efficiency.

The pre-drive circuit includes a delay RC network to insure that cross conduction does not occur. the time constant of this RC network must be greater than the 0.8 µs propagation delay associated with the switching times of the HCPL2531 optocoupler. By delaying the turn-on drive to the gates of the power MOSFET, cross conduction currents are eliminated.

External under-voltage lockout protection is added to the circuit to keep the lower stage FETs turned off until a pre-defined threshold voltage is obtained. This threshold voltage is determined by the threshold of the zener diode coupled with the threshold of the TP4050 buffer. In this circuit, the lower FETs remain off between 2 V and 6.2 V.

4.6. Advantages Over Discrete Transistors

Since the two power MOSFETs of each TPIC5201 are fabricated monolithically, the FETs within each device are inherently well-matched. As a result, there is little variation in the switching times and transconductance of the upper stage transistors. This device-matching aids in system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary pre-drive circuitry is greatly simplified.

Each power transistor in the TPIC5201 feature a low on-resistance of 90 mΩ. By minimizing on-resistance, the power consumption of the H-bridge is reduced, increasing the power available to the motor. Motor control systems built with low on-resistance power switches allow more efficient motor performance.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time rating curves. Unlike the single point energy specifications typical of discrete MOSFETs, designers using the TPIC5201 can accurately monitor compliance with active safe operating area design constraints.

5. Solenoid Application

5.1. Introduction

Solenoids are used to provide linear motion. Solenoid applications include electric locks on automobiles, mechanism actuators in tape recorders, and air control valves.

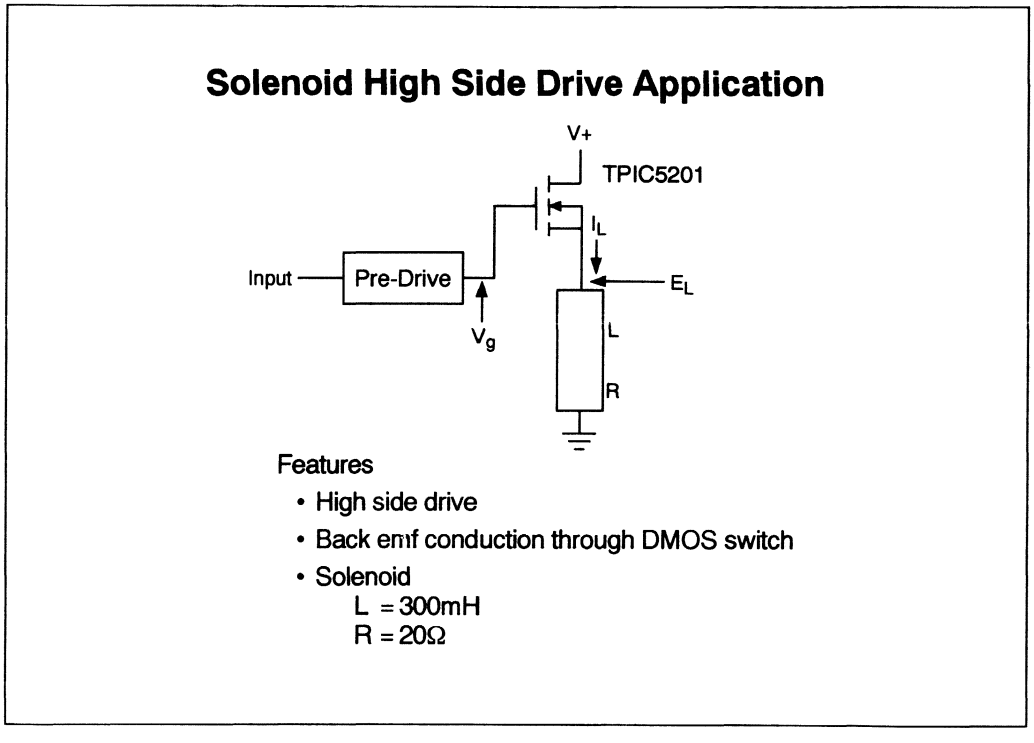


Figure 5.5.1 - Solenoid Application

Figure 5.5.1 shows a solenoid with a high side driver. The high side drive places the control switch between V_{CC} and the load. Selection of a switch device for this application must include an energy evaluation and a device which can operate as a high side switch. The solenoid load is inductive like the stepper motor, however instead of having cross coupled signals the solenoid has a dynamically changing impedance.

When the current reaches a level sufficient to cause the solenoid to operate the armature begins to move. When the armature moves relative to the coil the coil inductance changes. The amount of change is a function of the solenoid design. Conventional relays also exhibit this change in inductance since they are solenoids which operate switches.

Energy and power considerations are similar to the stepper motor. The interface circuit must drive an inductive load with a peak current. The solenoid winding inductance and resistance must be considered to evaluate the avalanche energy. Just as with any inductive load the total avalanche energy must be considered as well as the peak avalanche current.

5.2. Choosing an Interface Device

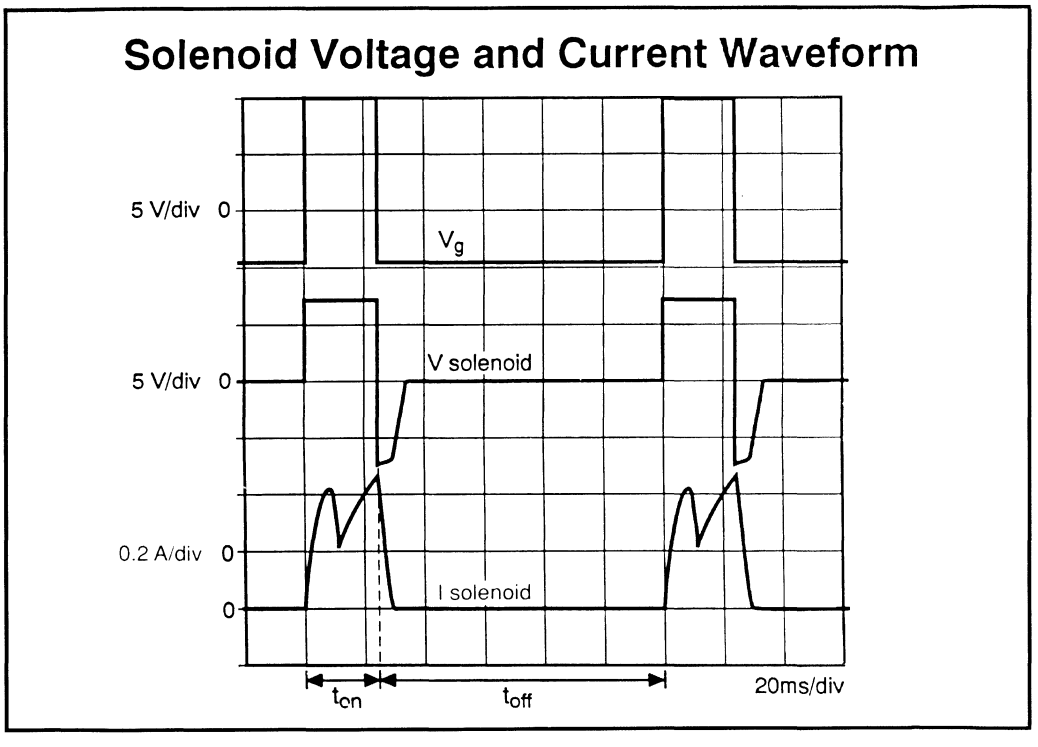


Figure 5.5.2 - Solenoid Voltage and Current

The voltage and current waveforms for the solenoid are shown in Figure 5.5.2. This particular solenoid was shown because of the drastic inductance change during operation. The inductance change causes the discontinuity seen in the inductor current during t_{on}.

Notice that Vg, the output from the predrive circuit, is at -5 V during t_{off}. The circuit as shown relies on the DMOS transistor to provide the conduction path for the back e.m.f. current from the inductor when drive is turned off (t_{off}). This was described in the stepper motor application (Section 5.3). When the switch is turned off the solenoid voltage goes negative. When the solenoid voltage reaches

approximately -7.5 V (V_g - 2.5 V) the DMOS transistor is turned on, effective clamping the inductor voltage. If V_g = 0 V at t_{off} then the solenoid voltage would be clamped at 2.5 V and the time required for the solenoid current to reach zero would be longer.

Using the current waveforms from Figure 5.5.2 the energy dissipated in the switch can be calculated. A TPIC5201 Power+ Array has been chosen as the switch for this application.

5.3. Energy Calculations:

Power & Energy Calculation

$$E_T = \frac{3 (L_H - * I_P V_{CL})}{6 (V_{CL} - V_{SS}) + 4 R * I_P}$$

$$= 113 \text{ mJ}$$

$$P_{off} = ET * f$$

$$= 0.94 \text{ W}$$

$$P_{on} = \frac{1}{3} IP@ * R_{DS(on)} \text{ d (Pulsed)}$$

$$= 1.5 \text{ mW}$$

$$P_T = P_{off} + P_{on} + P_{quires}$$

$$= 0.94 \text{ W}$$

$$P_{on} = IP2 * R_{DS} \text{ (Continuous)}$$

$$= 32.4$$

Where t_{on} = 25ms, L_H = 300 mH, t_{off} = 95ms, I_{Pk} = 0.5 A, V_{SS} = 12 V, $R_{DS(on)}$ = 90 mΩ, V_{CL} = 8 V, P_{quires} = 0

Figure 5.5.3 - Solenoid Energy Calculation

Using the calculations presented in section 5.2:

$$E_T = 3(L_H * I_P^2 * V_{CL})/[6(V_{CL}-V_{SS}) + R * I_P]$$

$$= 113 \text{ mJ}$$

$$P_{off} = E_T * f$$

$$=0.94 \text{ W}$$

$$Pon = 1/3 I_{PK}^2 * r_{DS(on)} * d$$

$$= 7.5 \text{ mW}$$

$$P_{T(av)} = P_{off} + P_{on} + P_{quies}$$
$$= 0.94\ W$$

Assuming that the solenoid could be turned on for an extended period of time the power dissipated in the switch would be :

$$PT = I^2 * rDS(on)$$
$$I = VCC/R$$
$$= 0.6\ A$$
$$PT = 0.6^2 * 0.09\ W$$
$$= 32.4\ mW$$

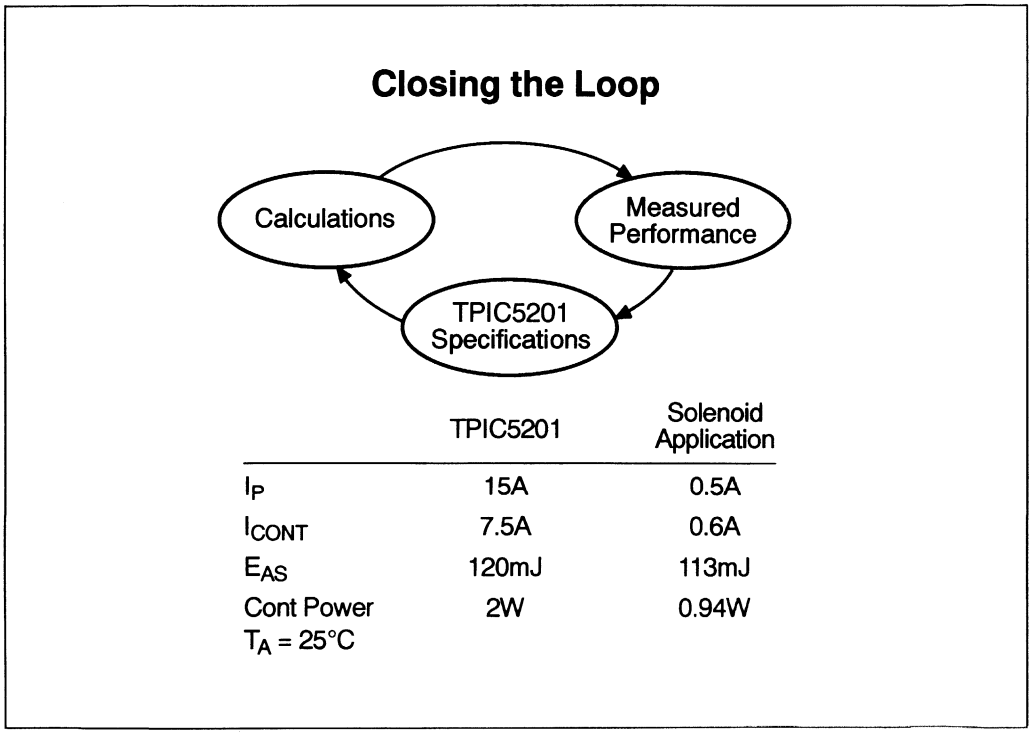


Figure 5.5.4 - Closing the Loop

Closing the design loop and comparing calculations, results and specifications will verify the design and indicate changes when necessary.

The results of this comparison are not what would be expected. The avalanche energy is high (113 mJ) while the power dissipation is quite low (0.9 W). This indicates that no heat sinking is required and that a device with a lower power and current rating could be used in this application. It also illustrates the

importance of doing thorough energy calculations. In this case a quick look at current handling alone might suggest the device chosen is overkill, but when avalanche energy is considered we can see the TPIC5201 is a good match for the application (a similar device rated at a lower peak current value would probably not be able to handle the avalanche energy, possibly resulting in repeated "mysterious" device failures!).

6. Incandescent Lamp Application

6.1. Introduction

Incandescent lamps are found in many industrial applications as well as automotive, marine and aeronautical applications. Incandescent lamps provide high output energy with rugged construction.

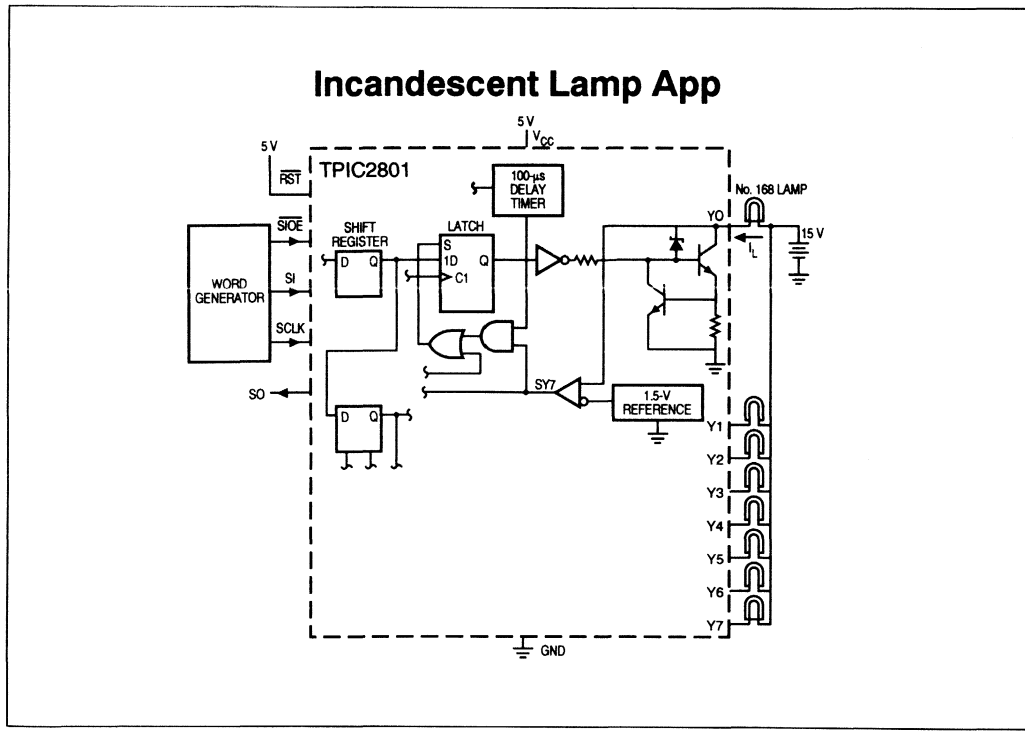


Figure 5.6.1 - Incandescent Lamp Application

The circuit in Figure 5.6.1 shows an application driving eight automotive lamps from a 15-V source. Incandescent lamps present a varying resistive load. The filament resistance increases dramatically as the lamp warms up to operating temperature.

Incandescent lamps are often operated with extended on time which results in a very low duty cycle time for the inrush current. If inrush current duty cycle is very low then the power dissipation could be ignored. If the high peak current is ignored premature failure of the switch transistor is likely. If the switch transistor is selected to accommodate the lamp peak current then circuit size and cost are sacrificed.

One solution is to current limit the inrush current. A conventional linear current limiting circuit would require dissipation of a large amount of heat during the warm up time. The choice of an Intelligent-Power device such as the TPIC2801 allows the output circuit to be implemented with a single integrated circuit. The TPIC2801 contains eight 1-A/30-V low-side switches packaged in a 15 pin Single-In-line Package (SIP). The eight switches are controlled with a single input, SI (Serial Input), by an 8-bit serial word. Diagnostics are also provided through the output, SO (Serial Output). Independent over-voltage and over-current protection is provided to all eight switches.

6.2. Circuit Operation

The rising edge of the SIOE- pulse following the data word is when shift register data is latched into the parallel latch and the output switches are activated by the new data. However, to allow the part to overcome high in-rush current, such as the lamp cold filament current, an internal 100 µs delay timer is started at the SIOE- pulse rising edge during which time the switch over voltage fault shutdown circuit is inhibited. During this 100 µs interval the switch is protected by an internal current limiter, which is set to regulate the current to approximately 1.5 A. Once the 100 µs timer period has elapsed, the output voltages are sensed by comparators and any output switch with output voltage greater than 1.5 V is latched off. It is important to note that these current-limited, 100 µs, soft start bursts of power not only protect the TPIC2801, but also protect the lamp filament from an otherwise filament degrading high in-rush current.

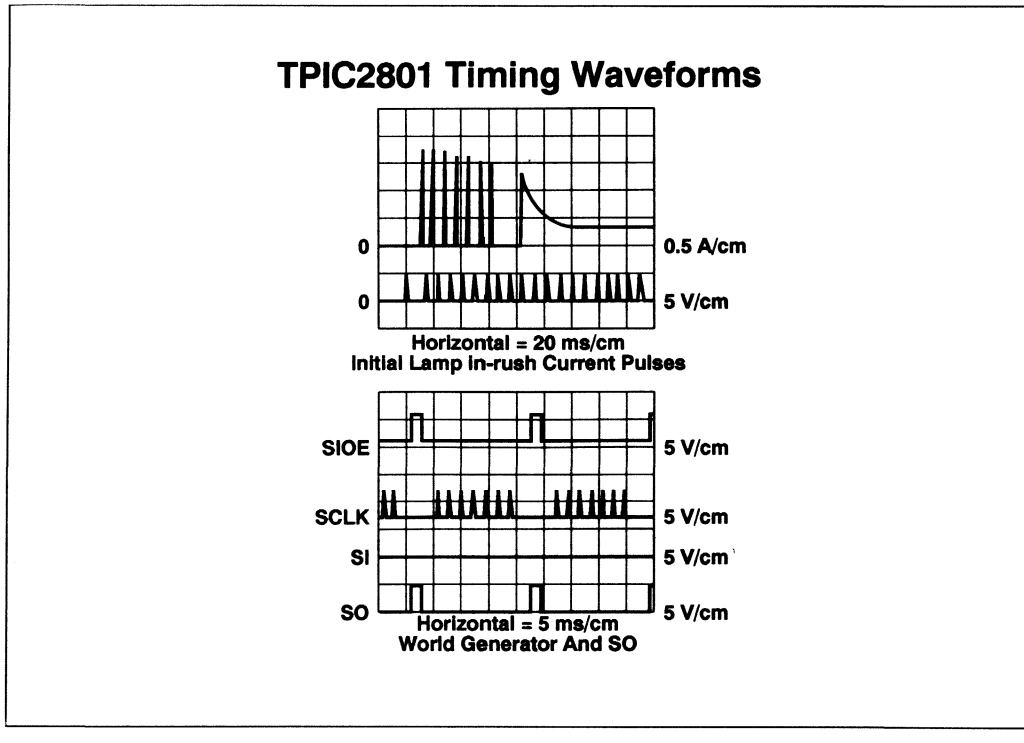


Figure 5.6.2 - TPIC2801 Timing Waveforms

The lamp current wave form shows the initial lamp in-rush current decrease from a value slightly greater that 1.5 A to a value of less than 0.5 A during a period of approximately 120 ms. The current initially presented to the lamps is a series of pulses. The first pulse is a 1.5 A/100 µs pulse that is coincident with the rising edge of the first SIOE- pulse that follows the data word.

6.2.1. TPIC2801 Power & Thermal Considerations

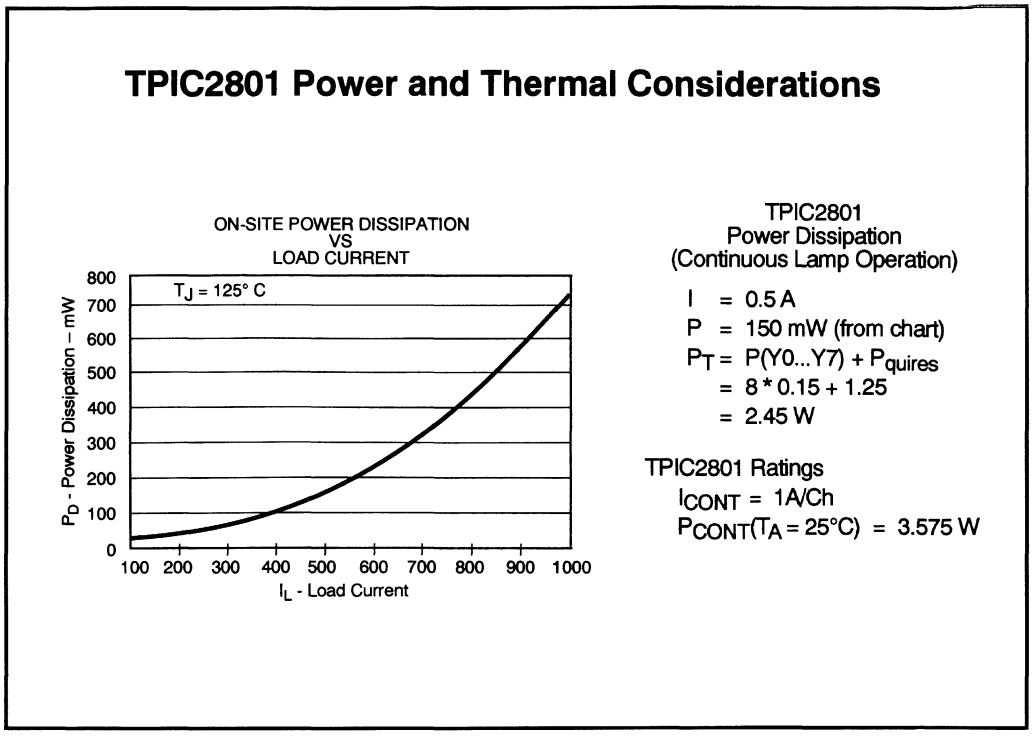


Figure 5.6.3 - TPIC2801 Power and Thermal Considerations

Figure 5.6.3 The On-State Power Dissipation vs. Load Current chart can be used to determine the dissipation of each output. This chart takes into consideration the bipolar transistor saturation voltage and the internal resistor I^2R power dissipation.

Calculation of the switch power dissipation for continuous duty:

Output Switches Y0...Y7: I = 0.5 A , duty cycle = 1.0

From figure 5.6.3:

$P_{(Y0...Y7)}$ = 0.15W x 1.0 x 8 = 1.2 W

$P_{(QUIES)}$ = 0.25 A x 5 V
= 1.25 W (per TPIC2801 data sheet)

$P_{T(AV)}$ = $P_{(Y0...Y7)} + P_{(QUIES)}$
= 2.45 W

The maximum power dissipation for the TPIC2801 at T_A = 25°C is 3.45 W

The self-protection capability of the TPIC2801 along with the power handling capability make this a good selection for this design .

Additional features include the ability to switch high currents and inductive loads. This device is well suited to switching high energy unclamped inductive loads since each of the eight power switches is equipped with an internal 35-V collector-to-base voltage clamp. The current capability of a single switch can be extended by parallel switch operation. This application utilized one of a series of intelligent power devices.

Other Intelligent Power devices are available with different configurations and feedback features providing effective system solutions for output systems.

7. Power+ Product Summary

7.1. Power+ Product Family

Power+ Product Configuration

Power+ Arrays — Multiple MOSFET in a Single Package

TPIC2202	2 Channel	Common-Source	Power	DMOS	Array
TPIC2301	3 Channel	Common-Source	Power	DMOS	Array
TPIC5201	Dual		Power	DMOS	Array
TPIC2701	7 Channel	Common-Source	Power	DMOS	Array

Power+ Logic Multiple MOSFET and Interface Logic in a Single Package

TPIC6259	Power+ Logic	8--Bit Addressable Latch
TPIC6273	Power+ Logic	Octal D-Type Latch
TPIC6595	Power+ Logic	8--Bit Shift Register

Intelligent Power — Power Outputs, Interface Logic and Diagnostics in a Single Package

TPIC2801	Octal Intelligent Power Switch with Serial Input
TPIC2404	Intelligent Power Quad Low-Side Switch
TPIC2406	Intelligent Power Quad MOSFET Latch

Figure 5.7.1 - Power+ Product Configuration

Power+ products are available in many configurations. The table in Figure 5.7.1 shows the Phase 1 products for Power+ Arrays and Power+ Logic plus some of the Intelligent Power products. This chart can serve as a starting point in choosing the product which functionally fits an application.

7.1.1. Power+ Product Performance

Power+ Product Performance

Power+ Arrays

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC2202	KC	7.5A	15A	90mΩ	120mJ	60V
TPIC2301						
TPIC5201						
TPIC2701	N	0.5A	2.5A	0.5Ω	22mJ	

Power+ Power

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC6259	N	250ma	15A	1.3Ω	75mJ	45V
TPIC6273						
TPIC6595						

Intelligent Power

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC2801	KV	1A	1A	Bipolar	40mJ	35V
TPIC2404	KN		15A	xstr		45V
TPIC2406	NE	0.7A	3A	0.5Ω	50mJ	60V

* I_{CONT} & I_{MAX} are per channel

Figure 5.7.2 - Power+ Product Performance

Selecting a Power+ Product includes choosing a product that meets the application performance requirements. The chart in Figure 5.7.2 compares some of the key specifications all three product families. These are the parameters most often used for an initial product selection.

The applications and design information presented in the previous sections has relied on some assumptions about device parameters in order to simplify the analysis while still arriving at a meaningful evaluation.

7.1.2. Power+ Array On Resistance

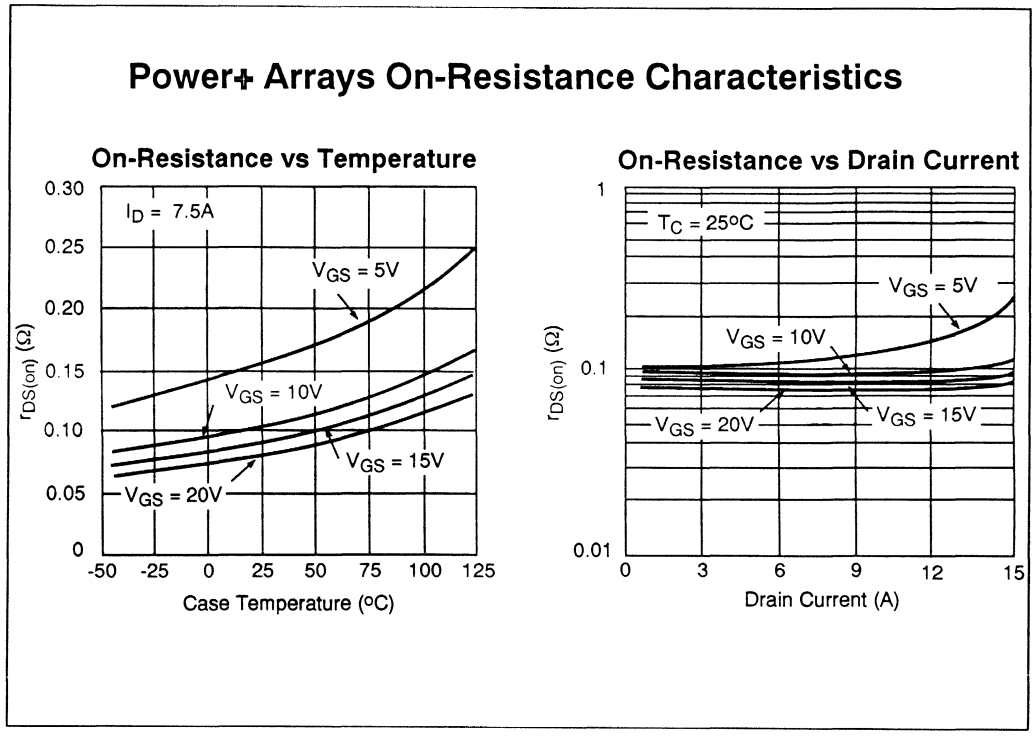


Figure 5.7.3 - Power + Arrays On-Resistance Characteristics

The two graphs in Figure 5.7.3 show the excellent on resistance stability for Power+ Array DMOS transistors. This also shows the type of device information available in the data sheet. Complete device characterization is provided in the data sheets for Texas Instruments Power+ products.

7.1.3. Power+ Logic Output Characteristics

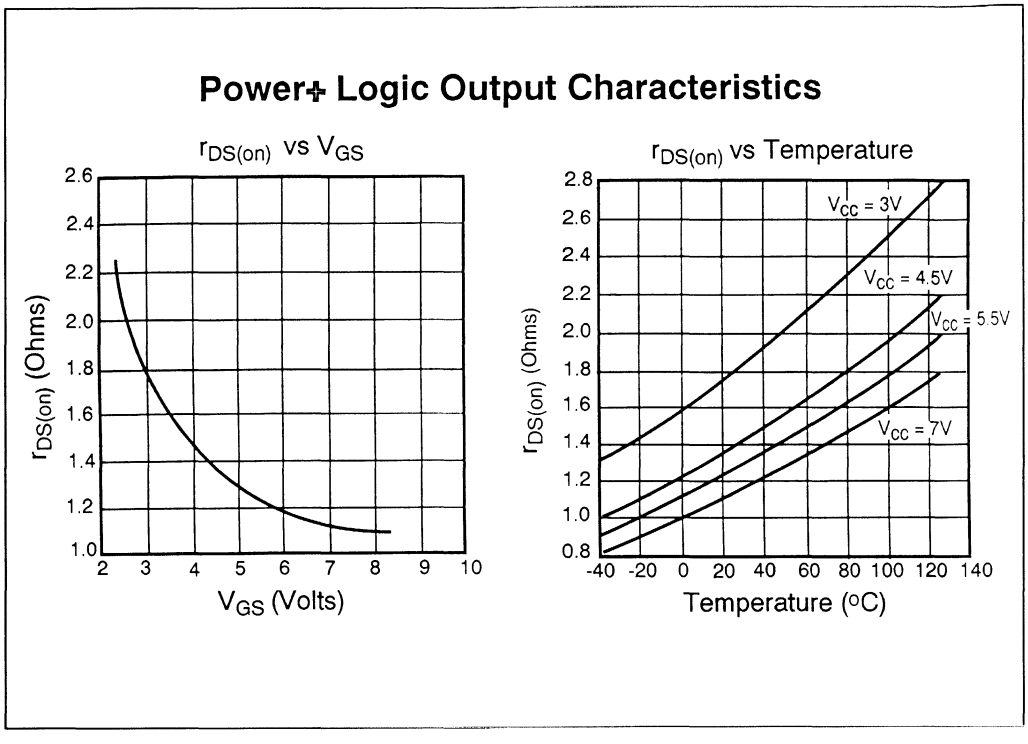


Figure 5.7.4 - Power+ Logic Output Characteristics

Figure 5.7.4 shows device on resistance performance for Power+ Logic output transistors. Note that while the $r_{DS(on)}$ is higher than for power arrays the power handling for these outputs is still substantial as shown in the chart of Figure 5.7.2.

7.1.4. Safe Operating Area

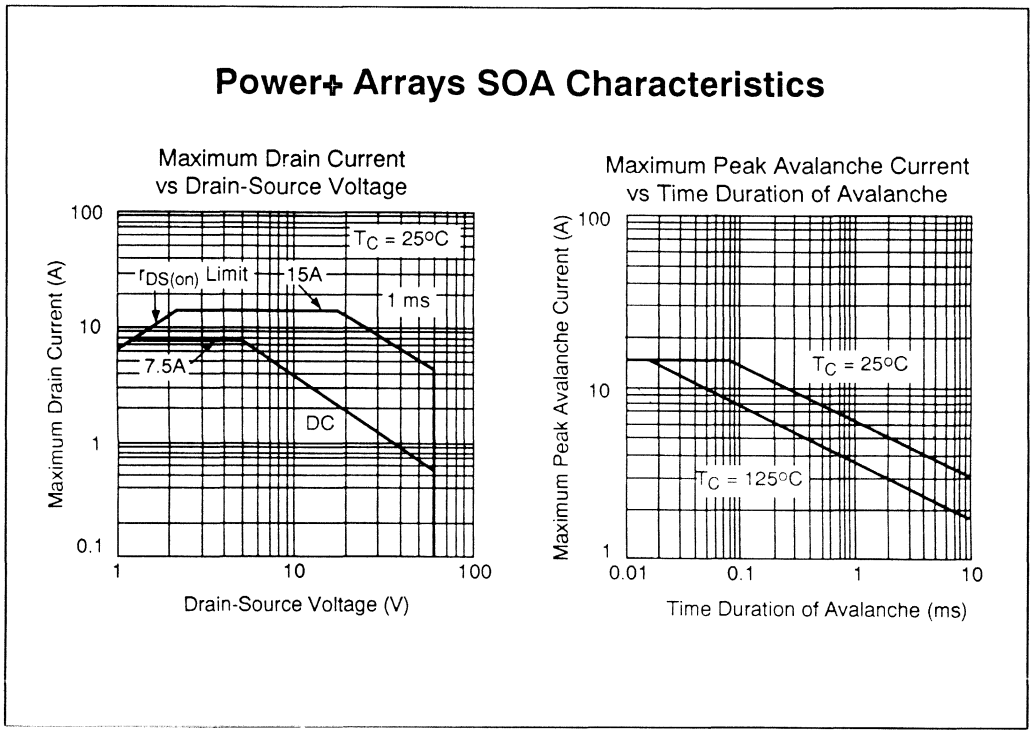


Figure 5.7.5 - Power+ Arrays Safe Operating Area Characteristics

The Safe Operating Area (SOA) characteristics are presented in graphical form to include peak currents and absolute times. Avalanche energy capability depends on many factors and cannot be adequately described by a single number. The graphs in Figure 5.7.5 indicate the relationship between safe avalanche operating conditions and time, temperature, and current for Power+ Arrays. Similar information is included in the data sheets for the other Power+ products.

8. Speech Application

8.1. Introduction

Speech and sound applications are another type of output system. Although speech systems have very little in common with the power output systems described previously they do serve to demonstrate the variety in design and function of output systems.

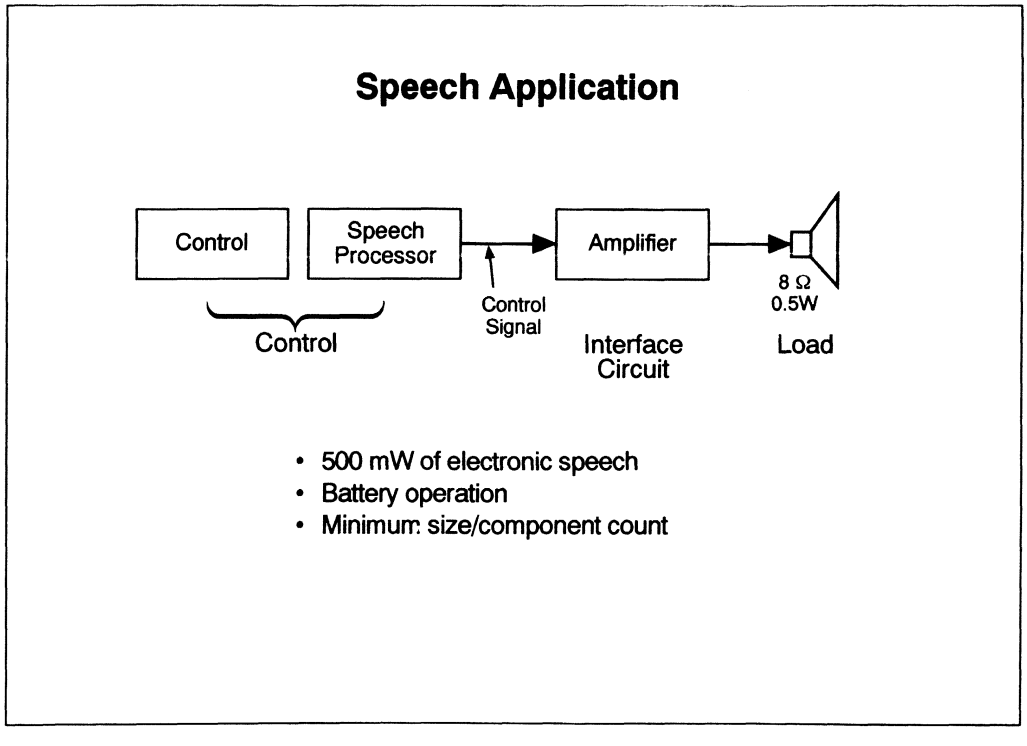


Figure 5.8.1 - Speech Application

Figure 5.8.1 shows a block diagram of a speech application. Speech or actually sound is another form of control system output.

This speech application includes a control and signal processing along with an output system which includes filtering and amplification and a loudspeaker as a load.

The control signal in this application is an analog signal, making the design "care abouts" different than those for the previous examples. A speech output system design must consider power, impedance and frequency response.

This application will include a special purpose speech processor and an amplifier/filter designed for speech applications.

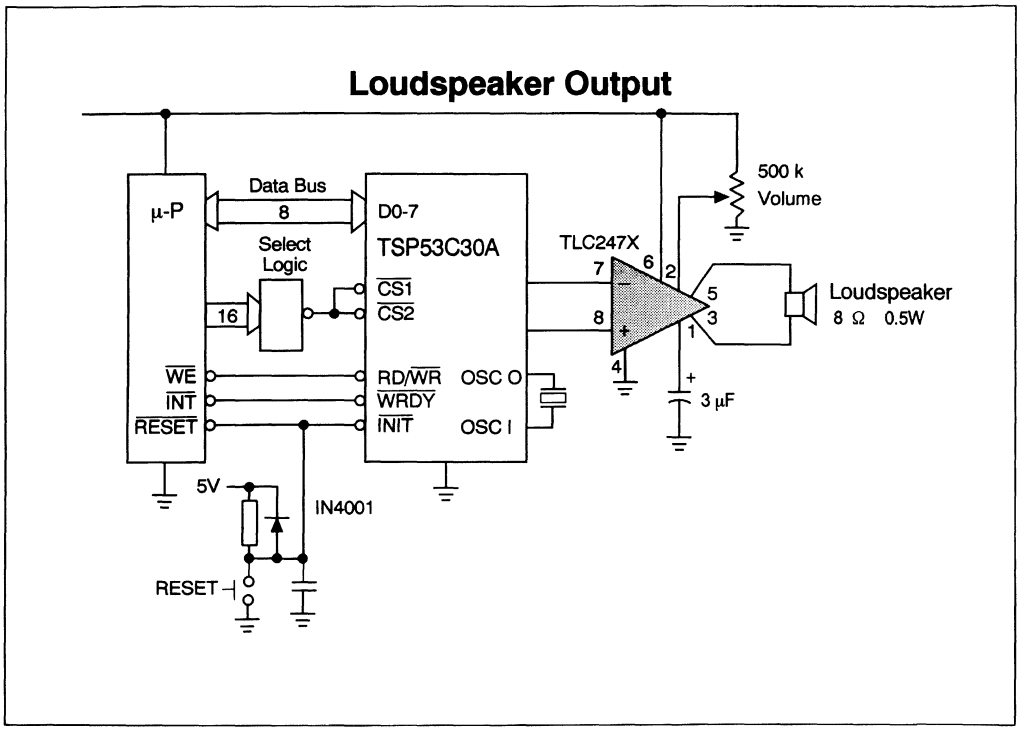


Figure 5.8.2 - Speech Application Circuit

Figure 5.8.2 shows the circuit diagram for a consumer type speech application. The overall system operation such as what words and sounds to speak and what sequence is controlled by a general purpose microprocessor. The microprocessor also sends the encoded speech data to the TSP53C30A speech synthesizer circuit. The TSP53C30A uses the encoded speech data to reproduce the speech sound. The output from the speech synthesizer is a high impedance differential signal generated by a DAC circuit. This output signal can directly drive a 50 ohm speaker, however best speech quality is achieved by filtering the signal and then amplifying it.

8.2. Choosing the components:

The choice of components was based on these requirements:

Maximum data compression (minimum memory requirement)

Quality speech reproduction (either LPC or PCM encoding)

Single battery operation.

The choice of Linear Predictive Coding (LPC) will provide an excellent trade off between data compression and quality. Quality is also enhanced by the use of filtering in the output circuit. Filtering and amplification can be accomplished with conventional op-amps and active filter circuits, however an integrated approach to this is the TLC247X circuits.

8.2.1. TLC2470/1

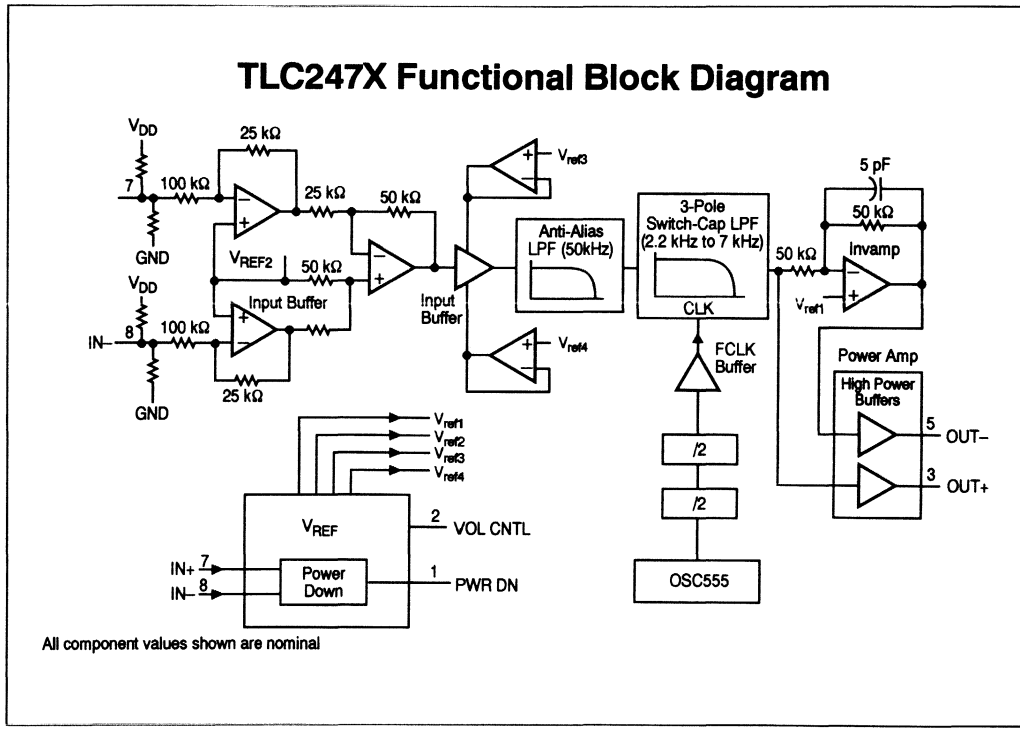


Figure 5.8.3 - TLC24701 - Differential Audio Filtered Amplifiers

The TLC24701 Differential Audio Filter Amplifier (DAFA) is designed for speech applications. The block diagram shows that the basic configuration is an amplifier with differential input and output. Low pass filtering is provided to filter the switching noise from the input signal. This circuit also

includes automatic power up/down control. This is an example of integrating the complete interface circuit into a single device to provide a very cost effective system solution for a consumer application.

9. Fluorescent Lamp Applications:

9.1. Overview

The following section focuses on a range of power products for fluorescent lighting applications. 50-60 Hz fluorescent lighting has been extensively used in industrial and commercial environments for many years now. Compared with conventional incandescent bulbs, fluorescent lamps offer many advantages including lower energy consumption and longer life for the same light output. With these benefits it is hardly surprising fluorescent lighting has become prevalent in the above mentioned environments. On the other hand, due to their size, the need for extra control gear and the higher initial cost, they have not yet achieved extensive penetration of the domestic market. However, all this is now beginning to change.

In the last decade, advances in power semiconductor technology and the desire to produce cheaper and more efficient lighting sources has led to many innovations to both further improve fluorescent lighting and to replace household incandescent lighting. Many new products, such as new, semi-intelligent starters and higher efficiency ballasts have begun to penetrate the market. An additional influence, becoming more important by the day, is that of the Greenhouse Effect. The concern for the environment and the desire to conserve the earth's resources has intensified the drive towards more energy efficient lighting and enabled the producers to look further afield to new market opportunities. All of these combined, has led to the rapid introduction of semiconductors into lighting systems in recent years and produced a market enjoying sustained growth for these new products.

Texas Instruments has been a leading supplier of power products for many years and now offers a range of products specifically targeted to the fluorescent lighting market. The following pages will look at two of these high growth areas, namely the electronic starter for 50 Hz fluorescent lamps and the high frequency electronic ballast. The latter can be further sub-divided into standard high frequency ballasts used to control the conventional 2 to 8 foot (60-240 cm) linear lamps and compact fluorescent ballasts recently introduced to replace the incandescent light bulb.

Emphasis will be placed on giving the reader a brief overview of the systems, what benefits can be attained, what are the key design constraints and finally a look at Texas Instruments product offerings and their key characteristics and benefits.

9.2. Fluorescent lamp starters

The control gear of any fluorescent lighting fitting provides two functions for the fluorescent tube, namely control and tube striking. In the running condition the gear provides a ballast function (series impedance from the supply source) to stabilize the electrical discharge in the gas. Under 50 Hz ac conditions, the voltage across the tube is approximately a square wave, which can range between 40 V and 200 V depending on tube type and length. The voltage difference between the sinusoidal supply

voltage and the "square" tube running voltage is thus developed across the ballast. In ac applications, an inductive ballast or choke performs this function with relatively little loss, although the lagging current often necessitates using a further capacitor to ensure a unity power factor.

The gear must also provide the correct sequence and conditions for starting the discharge. Normally, the tube cathode will be heated for a period in order to produce electrons for easy starting. This is termed "preheating" time. Then a sufficiently high voltage must be applied to initiate the discharge, this operation being termed "striking."

The simple series arrangement of a ballast and tube across the ac supply is possible when the maximum tube running voltage is below 60% of the peak supply voltage. Higher running voltages would create an unstable discharge condition. The tube running voltage strongly depends on the tube length. Thus in the UK (240 V ac), tubes of 6 and 8 feet are common, whilst in the rest of Europe (220 V ac), the limit tends to be 5 feet (150 cm). In countries where 110 V ac is used, such a series arrangement would severely limit tube length. As a result, control gear in these countries often incorporate a step-up auto transformer to boost the supply voltage.

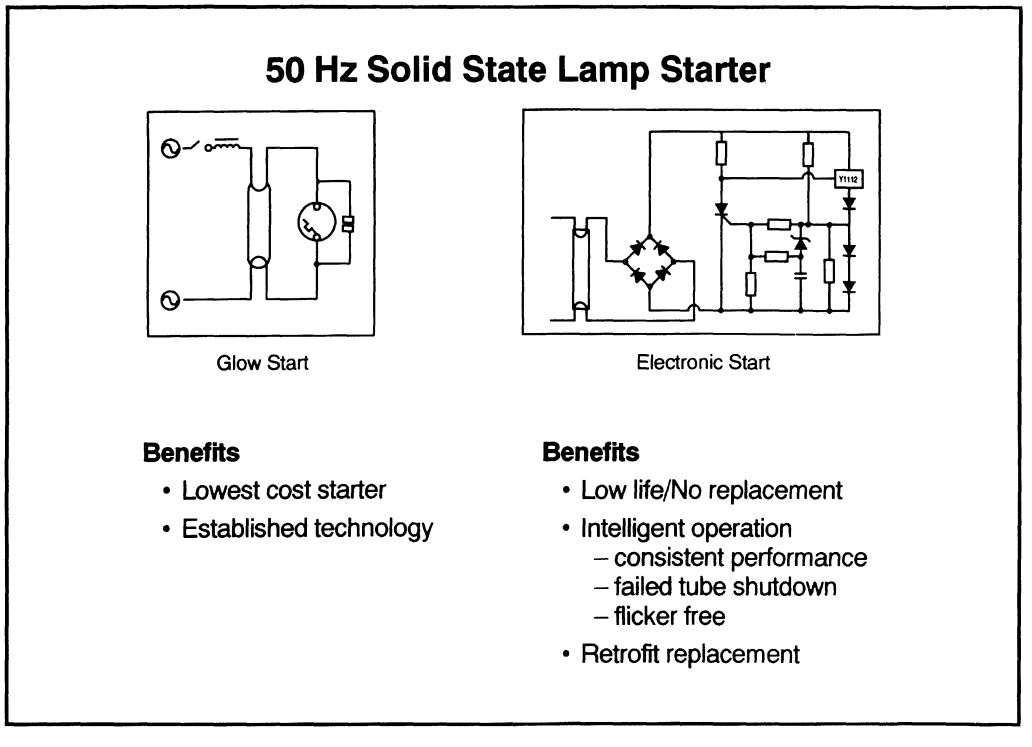


Figure 5.9.1 - Fluorescent Lamp Starters

Figure 5.9.1 shows the glow switch start configuration, which represents the lowest cost control gear system. The glow switch comprises a glass tube filled with a mixture of gases, such as helium and

hydrogen, in which is mounted a contact pair. One of the contacts is fixed and the other is mounted on the free end of a moveable bimetallic strip.

When power is first supplied to the terminals, the full ac voltage is applied to the glow switch, which starts a glow discharge in the gases (the ballast reactance limits the maximum current). After a short period, the heat from the discharge causes the bimetallic strip to bend, closing the contacts. This shorts out the discharge and starts the cathode preheating. A heavy current, limited mainly by the ballast reactance, flows through a series circuit composed of the ballast, tube upper cathode heater, closed glow switch contacts and the tube lower cathode heater. This condition continues until the bimetallic strip cools sufficiently to separate the contacts. The random nature of the contact opening means that current will normally be flowing at the instant of opening. Interrupting the current flow results in a back electromotive force (EMF) spike from the ballast inductance which, if large enough, will initiate a discharge in the fluorescent tube. If the generated voltage spike is not sufficient to strike the tube, the glow switch cycle repeats until the tube does eventually strike.

The gas reaction time of the fluorescent tube is faster than the glow switch. Thus, during striking, the glow switch does not limit the voltage applied to the fluorescent tube. When the fluorescent tube is running, its discharge voltage is lower than the level necessary to activate the glow switch. Hence, tube running prevents further operation of the glow switch. The glow switch circuit shown in figure 5.9.1 is for a "lagging" ballast. To improve efficiency further, power factor correction has to be introduced and this can be achieved via a shunt capacitor connected across the supply terminals.

The virtues of the glow switch are simplicity and low cost. However, several problems arise from its electromechanical nature. The first is that its random operation relative to the supply conditions means that several pulses may be necessary to strike the fluorescent tube. This not only serves to reduce the lifetime of the tube but can be extremely annoying, particularly in environments where the light source is continually switched on and off. Tubes nearing the end of there lifetime will continually flash as the glow switch attempts to strike the failed tube over and over again. This can be disruptive to the work environment and will require immediate replacement of tube to correct the problem.

9.3. The Fluoractor

To overcome the problems associated with the glow switch starter, Texas Instruments have introduced a solid state device, the Fluoractor™, (Y1112), which enables the construction of a solid state starter with greatly enhanced functionality. The right hand side of figure 5.9.2 illustrates a typical applications circuit for this starter.

Electronic starters built around the Fluoractor allow flicker free start up of the fluorescent tube, extended tube lifetime and permanent shutdown of faulty tubes. Furthermore, it is often the glow switch itself that fails prematurely, so the extended lifetime of the electronic starter will considerably reduce maintenance costs. All of this circuitry for the Fluoractor based starter is small enough to fit into the glow switch starter canister, therefore making it a retrofit replacement requiring no redesign of existing systems.

It should be noted that the Fluoractor is a unidirectional device and requires being inside a full-wave diode bridge to become bi-directional for ac operation. When power is first applied a low level current path will supply enough current to the fluoractor gate to trigger the device into conduction. Once turn on occurs, the lamp cathode preheating period starts. During this period the Fluoractor is "on" and passing the full-wave rectified current. The ballast current, flowing through the Fluoractor cathode

diodes, develops a voltage which forms the charging source for the capacitive timing network. Preheating ends and pulsing begins when the peak voltage reached at the turn off SCR gate is sufficient to cause triggering. Pulsing provides the back electromotive (EMF) spike which will strike the fluorescent tube, in this case , on the first attempt. Pulse duration is a function of zener voltage, supply voltage, choke inductance and Fluoractor holding current. At the end of the pulsing period, reached when the turn off SCR is triggered before the latched conduction in the Fluoractor is achieved, GTO action occurs. This results in the shutdown of the Fluoractor.

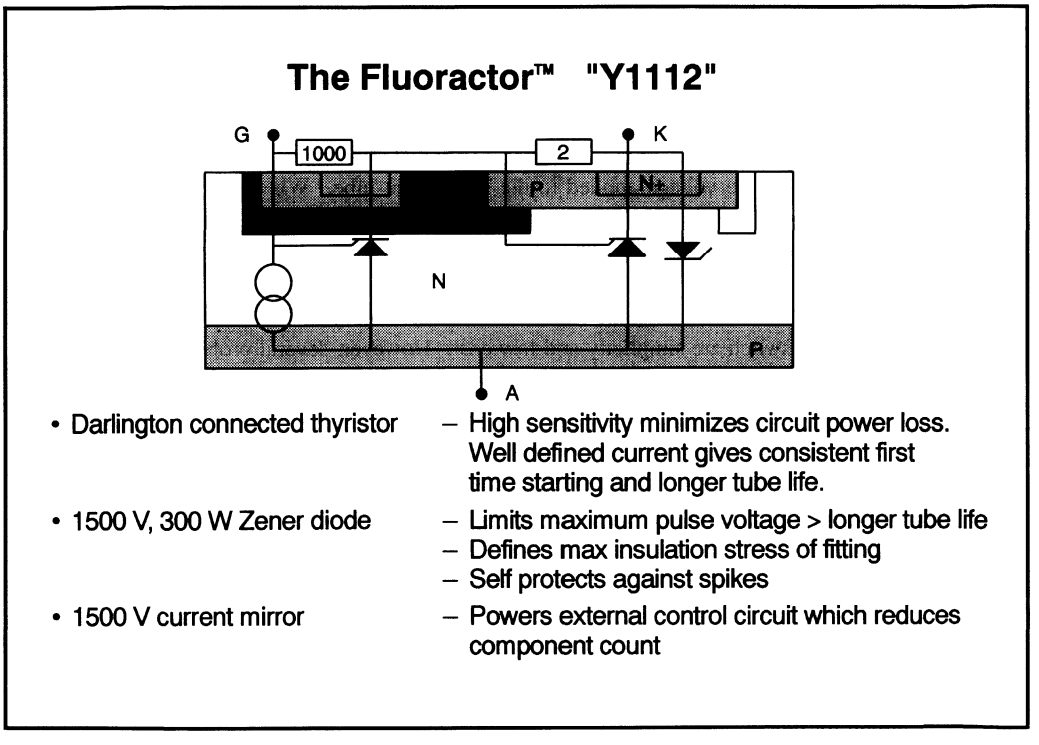


Figure 5.9.2 - The Fluoractor - Y1112

9.3.1. Fluoractor construction

In order to minimize the drive power requirement, the Fluoractor is constructed using a high sensitivity darlington connected thyristor. Figure 5.9.2 illustrates both the device cross section and the lumped equivalent circuit of the Fluoractor. Once triggered, the Fluoractor will remain on until the anode current is reduced to a critical value called the holding current, I_H. Below the holding current, the Fluoractor will turn off unless gate drive is re-applied. The high sensitivity of the device is controlled by the 1 k ohm gate-cathode resistor of the driver thyristor section. The lumped equivalent of gate-cathode resistor of the output thyristor section is of the order of 2 ohms. This means the triggering

sensitivity of this section is about 200 mA. More importantly, the holding current will be of the same order and it is this that defines the minimum switch breaking current which in turn leads to tube ignition.

The integral zener diode has a maximum voltage rating of 1500 V. This ensures sufficient volts are applied to the tube to ensure first time starting, but limits the maximum voltage seen in the circuit, therefore keeping the voltage ratings of the control circuitry down to about 1750 V.

A previously unmentioned function of the Fluoractor is the current mirror which considerably simplifies the required control circuitry. Once the Fluoractor is carrying current, a proportion of this flows out of the gate terminal. This current can be used as a power supply for the control circuit or a maintaining current if the Fluoractor is driven from an SCR type turn off device.

It is the Planar process used for the construction of the Fluoractor which allows very precise control of the holding current. This, along with the 1500-V rating of the zener are critical in determining the pulse duration. A precisely controlled pulse duration in turn leads to a soft start up with no tube flicker. An obvious benefit of soft start up is that of reduced stress on the tube cathodes and therefore, extended tube life.

A more detailed explanation of the Fluoractor, of both its construction and application can be found in the published application note.

9.3.2. High frequency electronic ballasts

As mentioned earlier, standard fluorescent lights are used extensively in industrial and commercial environments as a result of the many benefits they offer in terms of cost and energy consumption. Compared to a standard incandescent light bulb, 50 Hz fluorescent tubes offer the same light output for approx. one quarter of the power consumption and have longer life expectancy.

Recognizing the need for smaller, lighter and more efficient forms of lighting, lamp manufacturers turned their attentions to high frequency operation of the ballast. By increasing the operating frequency of the ballast from 60 Hz to approximately 30 kHz, one is able to achieve in the region of a 20% energy saving for the same light output. Along with this very obvious financial enticement, many other benefits such as reduced weight, increased lamp life, the elimination of stroboscopic effects and flicker free start up are also achievable. It is hardly surprising then, in recent years the industry has experienced considerable growth as manufacturers vie for market share with their new product offerings.

Even newer to the market, is the relatively recent introduction of the compact fluorescent high frequency ballast. Compact meaning suitable for direct replacement of the incandescent household light bulb. Compacts can come in two forms; firstly where the ballast and fluorescent tube are combined as a single unit and secondly, where the tube is removable and consequently replaceable when it fails. These new ballast/lamp combinations offer an 80% energy saving over the incandescent light bulb for the same light output and, at the same time, are claimed to have eight limes the life expectancy.

9.3.3. High frequency lamp operation

When a fluorescent lamp is running at a frequency of 50 or 60 Hz, the relatively slow rate of operation means that the conducting gas reacts faster than the ac line rate. This results in two phenomena. Firstly, when the lamp current falls to zero as the current polarity changes, the lamp stops conducting

and has to re-strike on the opposite current polarity. Second, is that the conducting gas has a negative impedance characteristic. To control the lamp current, the lamp must be connected in series with higher positive impedance (ballast). At ac line frequencies the ballast is usually an iron cored wound component.

When a fluorescent tube is operated at frequencies higher than a few kilohertz both these effects disappear. In this case, the lamp can be approximated to a resistive load. At these high frequencies, the persistence of the light emitting phosphor smoothes out any possible flicker. Some studies claim that the lack of flicker from high frequency operation reduces the incidence of headaches. The absence of flicker also removes the stroboscopic effects of conventional ac line powered fluorescent lamps. These stroboscopic effects can be highly dangerous as they can make rotating machinery appear stationary. frequency operation reduces the tube power required for a given light level. A 58 W, 50 Hz rated tube might only need 50 W at high frequencies to produce the same light output. At the system level the total power drawn from the ac supply might be 68 W for a 50 Hz ballast and only 55 W for a high frequency ballast. So generally an electronic ballast system draws less power than the 50 Hz equivalent.

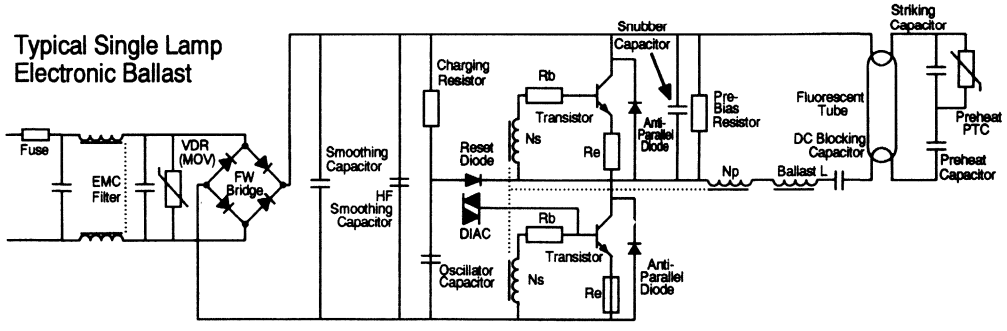
9.3.4. Basic operation

The basic function of an electronic ballast is to convert ac at line frequency to a much higher frequency, usually in the 30 kHz region. It is overly complex to do a direct low frequency to high frequency conversion, so normally a two stage process is used. The ac supply is first rectified to dc and then this dc is chopped at high frequency to produce the ac to power the lamp. Most European electronic ballasts are based on the principle of full wave rectifying the 50 Hz ac supply to produce a dc supply voltage, V_S, in the range of 250 to 370 V. (Where a boost converter is used to provide electronic power factor correction the dc rail voltage is higher, typically in the region of 400 V.) This dc supply then feeds a half "H" bridge inverter switching at 20 to 30 kHz. The high frequency square wave then powers one or more fluorescent tubes via an LC filter network.

9.3.5. Transistor operation

This section looks in detail at the transistor operation. In normal operation, the transistor is expected to switch efficiently, but not turn-off the current so fast that an EMC problem is generated. These two requirements are conflicting, so the turn-off speed has to be a compromise between efficiency and possible EMC problems. Start-up and fault conditions increase the current levels and, to be reliable under these conditions, the transistor needs to has an adequate high current performance. Inverters which use the storage time of the transistor switches to determine the oscillation timing will need transistors with consistent storage times.

High Frequency Ballast Design Considerations



Supply Volts	240 V rail voltage	V_{CEO} > 370 V
Tube Power	Defines min current rating	2.5 A < 50 W, 4 A < 125 W
EMC	Restricts switching speed	t_{off} not too fast
Efficiency	Must minimise losses	Fast switching, low on losses
Start Up/Fault Conditions	4 X normal running current	High current gain (h_{FE})
Tube Output/Lifetime	Balanced transistor operation	h_{FE}/t_{off} matched pairs

Figure 5.9.3 - High Frequency Ballast Design

9.3.6. Efficiency

Electronic ballasts are very efficient. Typically efficiencies in the 90% plus region are achieved. A ballast with 91% efficiency driving a 20 W lamp would have losses of about 2 W. Something like 0.5 W of these losses might be due to the inverter power switching transistors. This equates to a power loss of 0.25 W per transistor. It is important the characteristics of the transistors are chosen to minimize this power loss. These losses associated with the inverter transistors can be broken down into on-state and switching losses. The on-state losses are a combination of base-emitter and collector-emitter losses. Together, they constitute approx. 40% of the transistor losses, with collector-emitter accounting for two thirds of these. Switching losses account for approx. 60% of the overall losses and in particular, the 90% - 10% collector current fall time, t_{fi}, is the prime contributor to this.

It is possible to estimate the fall time switching loss, P_f, by using straight line approximations to the wave forms. The current wave form will start at a value of I_{cpk} and decrease to zero in time 1.25 * t_{fi}. Correspondingly, the voltage will start at zero and ramp at dv_r/dt during the fall time. At any instant, t, after the start, the instantaneous power, p_f, will be :-

$$p_f = I_{cpk}\left(1-\frac{t}{1.25t_{fi}}\right)\frac{dv_r}{dt}t$$

Integrating this power over the switching period and averaging at the operating frequency, f, gives:-

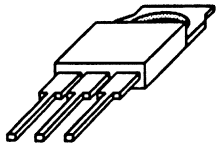
$$p_f = 0.26I_{cpk}f(t_{fi})^2\frac{dv_r}{dt}$$

This shows that the power is proportional to the square of the fall time.

9.3.7. Start-up and fault conditions

In addition to normal running the transistor will also experience start-up and possibly fault conditions. Start-up can be considered a short term fault condition. Often for the start up condition, the operating transistor current is twice the normal running current until the lamp strikes. Under these conditions it is prudent to ensure the transistor has sufficient gain at twice the normal current to control the transistor's start up power loss. In the failed tube condition, the high current condition is not terminated by the tube striking. Further, when the PTC resistor switches, the circuit begins to develop much higher levels of voltage and current. If this condition persists, the transistor heating will lengthen the storage time resulting in further increases of the voltage and current. Hence, there will need to be some sort of fusing mechanism which will ultimately terminate the over load condition. More sophisticated systems will have electronic or electromechanical shut down, which will prevent damage to the circuit components.

High Frequency Ballast Transistors



	Ballasts < 50 watts BULL770	Ballasts > 50 watts BUL791
• V_{CEO} (min)	400V	400V
• I_C (peak)	6 A	8 A
• V_{CESAT} (max)*	0.25 V	0.4 V
• h_{FE}*	7-21	6-22
• t_n (max)*	190ns	180 ns

* Characteristics measured at typical ballast operating conditions

Figure 5.9.4 - High Frequency Ballast Transistors

9.3.8. BUL770/BUL791

The high voltage transistor requirements for electronic ballasts are different to those in the switching mode power supply. Recognizing this, Texas Instruments have introduced the BUL770 and BUL791 specifically for electronic ballast applications. By careful analysis of electronic ballast systems and their requirements, it has been possible to develop products to satisfy these needs exactly.

These transistors have low power loss under the relatively low base turn-off current conditions typical for this application. V_{cesat} characteristics are specified at 0.25 V and 0.3 V for the BUL770 and BUL791 respectively (typical operating conditions). The collector current fall times of 190 ns and 180 ns ensure the optimum balance between fast switching for low loss and potential EMC problems.

Both devices have a V_{ceo} of 400 V which is driven from the full wave rectification of the 50 Hz, 240 V ac supply. Voltages of up to 370 V are often seen and where a boost converter is used to provide electronic power factor correction, the dc rail voltage is higher, typically in the region of 400 V.

Inverters which use the storage time of the transistor switches to determine the oscillation timing will need transistors with consistent storage times and high current gains. Otherwise, an unbalanced circuit

will reduce light output and increase power loss. Both the BUL770 and the BUL791 have tightly controlled gains (also related to storage times) between 8 and 24 for typical circuit conditions.

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NOTES

TI Worldwide Sales Offices

ALABAMA: Huntsville: 4960 Corporate Drive, Suite 150, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: Irvine: 1920 Main Street, Suite 900, Irvine, CA 92714, (714) 660-1200;
San Diego: 5625 Ruffin Road, Suite 100, San Diego, CA 92123, (619) 278-9600;
Santa Clara: 5353 Betsy Ross Drive, Santa Clara, CA 95054, (408) 980-9000;
Woodland Hills: 21550 Oxnard Street, Suite 700, Woodland Hills, CA 91367, (818) 704-8100.

COLORADO: Aurora: 1400 S. Potomac Street, Suite 101, Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park South, Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake Boulevard, Suite 1008, Altamonte Springs, FL 32701, (407) 260-2116;
Fort Lauderdale: 2950 N.W. 62nd Street, Suite 100, Fort Lauderdale, FL 33309, (305) 973-8502;
Tampa: 4803 George Road, Suite 390, Tampa, FL 33634-6234, (813) 885-7588.

GEORGIA: Norcross: 5515 Spalding Drive, Norcross, GA 30092-2560, (404) 662-7967.

ILLINOIS: Arlington Heights: 515 West Algonquin, Arlington Heights, IL 60005, (708) 640-2925.

INDIANA: Carmel: 550 Congressional Drive, Suite 100, Carmel, IN 46032, (317) 573-6400;
Fort Wayne: 103 Airport North Office Park. Fort Wayne, IN 46825, (219) 489-4697.

KANSAS: Overland Park: 7300 College Boulevard, Lighton Plaza, Suite 150, Overland Park, KS 66210, (913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Drive, Suite 100, Columbia, MD 21045, (410) 964-2003.

MASSACHUSETTS: Waltham: Bay Colony Corporate Center, 950 Winter Street, Suite 2800, Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Road, Farmington Hills, MI 48018, (313) 553-1581;

MINNESOTA: Eden Prairie: 11000 W. 78th Street, Suite 100, Eden Prairie, MN 55344, (612) 828-9300.

MISSOURI: St. Louis: 12412 Powerscourt Drive, Suite 125, St. Louis, MO 63131, (314) 821-8400.

NEW JERSEY: Iselin: Metropolitan Corporate Plaza, 485 Bldg. E. U.S. 1 South, Iselin, NJ 08830, (908) 750-1050.

NEW MEXICO: Albuquerque: 2709 J. Pan American Freeway, N.E., Albuquerque, NM 87101, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Drive, East Syracuse, NY 13057, (315) 463-9291;
Fishkill: 300 Westage Business Center, Suite 140, Fishkill, NY 12524, (914) 897-2900;
Melville: 48 South Service Road, Suite 100, Melville, NY 11747, (516) 454-6601;
Pittsford: 2851 Clover Street, Pittsford, NY 14534, (716) 385-6770.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Charlotte, NC 28217, (704) 527-0930;
Raleigh: 2809 Highwoods Boulevard, Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Road, Beachwood, OH 44122-5875, (216) 765-7528;
Beavercreek: 4200 Colonel Glenn Highway, Suite 600, Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 S.W. 105th Street, Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Parkway, Suite 200, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: 615 Mercantil Plaza Building, Suite 505, Hato Rey, PR 00919, (809) 753-8700.

TEXAS: Austin: 12501 Research Boulevard, Austin, TX 78759, (512) 250-6769;
Dallas: 7839 Churchill Way, Dallas, TX 75251, (214) 917-1264;
Houston: 9301 Southwest Freeway, Commerce Park, Suite 360, Houston, TX 77074, (713) 778-6592;
Midland: FM1788 & I-20, Midland, TX 79711-0448, (915) 561-7137.

UTAH: Salt Lake City: 2180 South 1300 East, Suite 335, Salt Lake City, UT 54106, (801) 466-8972.

WISCONSIN: Waukesha: 20825 Swenson Drive, Suite 900, Waukesha WI 53186, (414) 798-1001.

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Richmond Hill: 280 Centre Street East, Richmond Hill, Ontario, Canada L4C 1B1, (416) 884-9181;
St. Laurent: 9460 Trans Canada Highway, St. Laurent, Quebec, Canada H4S 1R7, (514) 335-8392.

AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd., 6-10 Talavera Road, North Ryde (Sydney), New South Wales, Australia 2113, 2-878-9000; 14th Floor, 380 Street, Kilda Road, Melbourne, Victoria, Australia 3004, 3-696-1211; 171 Philip Highway, Elizabeth, South Australia 5112, 8 255-2066.

BELGIUM: Texas Instruments Belgium S.A./N.V., Avenue Jules Bordetlaan 11, 1140 Brussels, Belgium, (02) 242 30 80.

BRAZIL: Texas Instruments Electronicos do Brasil Ltda., Av. Eng. Luiz Carlos Berrini, 1461-11o, andar, 04571, Sao Paulo, SP, Brazil, 11-535-5133.

DENMARK: Texas Instruments A/S, Borupvang 2D, 2750 Ballerup, Denmark, (44) 68 74 00.

FINLAND: Texas Instruments OY, Ahertajantie 3, P.O. Box 86, 02321 Espoo, Finland, (0) 802 6517.

FRANCE: Texas Instruments France, 8-10 Avenue Morane-Saulnier, B.P. 67, 78141 Velizy-Villacoublay Cedex, France, (1) 30 70 1003.

GERMANY: Texas Instruments Deutschland GmbH., Haggertystrasse 1, 8050 Freising, (08161) 80-0; Kurfurstendamm 195-196, 1000 Berlin 15, (030) 8 82 73 65; Dusseldorfer Strasse 40, 6236 Eschborn 1, (06196) 80 70; Kirchhorster Strasse 2, 3000 Hannover 51, (0511) 64 68-0; Maybachstrasse II, 7302 Ostfildern 2 (Nellingen), (0711) 3403257; Gildehofcenter, Hollestrasse 3, 4300 Essen 1, (0201) 24 25-0.

HOLLAND: Texas Instruments Holland B.V., Hogehilweg 19, Postbus 12995, 1100 AZ Amsterdam-Zuidoost, Holland. (020) 5602911.

TEXAS INSTRUMENTS

HONG KONG: Texas Instruments Hong Kong Ltd., 8th Floor, World Shipping Center, 7 Canton Road, Kowloon, Hong Kong, 737-0338.

HUNGARY: Texas Instruments Representation, Budaorsi ut.42, 1112 Budapest, Hungary, (1) 1.66 66 17.

IRELAND: Texas Instruments Ireland Ltd., 7/8 Harcourt Street, Dublin 2, Ireland, (01) 755233.

ITALY: Texas Instruments Italia S.p.A., Centro Direzionale Colleoni, Palazzo Perseo-Via Paracelso 12, 20041 Agrate Brianza (Mi), Italy, (039) 63221; Via Castello della Magliana, 38, 00148 Roma, Italy (06) 6572651; Via Amendola, 17, 40100 Bologna, Italy (051) 554004.

JAPAN: Texas Instruments Japan Ltd., Aoyama Fuji Building 3-6-12 Kita-Aoyama Minato-ku, Tokyo, Japan 107, 03-498–2111; MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-ku, Tokyo, Japan 108, 03-769-8700; Nissho-iwai Building 5F, 2-5-8 Imabashi, Chuou-ku, Osaka, Japan 541, 06-204-1881; Dai-ni Toyota Building Nishi-kan 7F, 4-10-27 Meieki, Nakamura-ku, Nagoya, Japan 450, 052-583-8691; Kanazawa Oyama-cho Daiichi Seimei Building 6F, 3-10 Oyama-cho, Kanazawa-shi, Ishikawa, Japan 920, 0762-23-5471; Matsumoto Showa Building 6F, 1-2-11 Fukashi, Matsumoto-shi, Nagano, Japan 390, 0263-33-1060; Daiichi Olympic Tachikawa Building 6F, 1-25-12, Akebono-cho, Tachikawa, Tokyo, Japan 190, 0425-27-6760; Yokohama Business Park East Tower 10F, 134 Goudo-cho, Hodogaya-ku, Yokohama-shi, Kanagawa, Japan 240, 045-338-1220; Nihon Seimei Kyoto Yasaka Building 5F, 843-2, Higashi Shiokohji-cho, Higashi-iru, Nishinotoh-in, Shiokohji-dori, Shimogyo-ku, Kyoto, Japan 600, 075-341-7713; Sumitomo Seimei Kumagaya Building 8F, 2-44 Yayoi, Kumagaya-shi, Saitama, Japan 360, 0485-22-2240; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki-shi, Oita, Japan 873, 09786-3-3211.

KOREA: Texas Instruments Korea Ltd., 28th Floor, Trade Tower, 159, Samsung-Dong, Kangnam-ku Seoul, Korea, 2-551-2800.

MALAYSIA: Texas Instruments, Malaysia, Sdn. Bhd., Asia Pacific, Lot 36.1 #Box 93, Menara Maybank, 100 Jalan Tun Perak, 50050 Kuala Lumpur, Malaysia, 2306001.

MEXICO: Texas Instruments de Mexico S.A. de C.V., Alfonso Reyes 115, Col. Hipodromo Condesa, MExico, D.F., 06170, 5-515-6081.

NORWAY: Texas Instruments Norge A/S, P.B. 106, Refstad (Sinsenveien 53), 0513 Oslo 5, Norway, (02) 155 090.

PEOPLE'S REPUBLIC OF CHINA: Texas Instruments China Inc., Beijing Representative Office, 7-05 CITIC Building, 19 Jianguomenwai Dajie, Beijing, China, 500-2255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd., Philippines Branch, 14th Floor, Ba-Lepanto Building, Paseo de Roxas, Makati, Metro Manila, Philippines, 2-8176031.

PORTUGAL: Texas Instruments Equipamento Electronico (Portugal) LDA., Ing, Frederico Ulricho, 2650 Moreira Da Maia, 4470 Maia, Portugal (2) 948 1003.

SINGAPORE (& INDIA, INDONESIA, THAILAND): Texas Instruments Singapore (PTE) Ltd., Asia Pacific, 101 Thomson Road, #23-01, United Square, Singapore 1130, 3508100.

SPAIN: Texas Instruments Espana S.A., c/Gobelas 43, Urbanizasion La Florida, 28023, Madrid, Spain, (1) 372 8051; c/Diputacion, 279-3-5, 08007 Barcelona, Spain, (3) 317 91 80.

SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen), Isafjordsgatan Box 30, 164 93 Kista, Sweden, (08) 752 58 00.

SWITZERLAND: Texas Instruments Switzerland AG, Riedstrasse 6, 8953 Dietikon, Switzerland, (01) 744 2811.

TAIWAN: Texas Instruments Taiwan Limited, Taipei Branch, 10th Floor, Bank Tower, 205 Tung Hua N. Road, Taipei, Taiwan, 10592, Republic of China, 2-713 9311.

TURKEY: Texas Instruments, DSEG MidEast Regional Marketing Office, Karum Center, Suite 442, Iran Caddesi 21, 06680 Kavakildere, Ankara, Turkey, 4-468-0155.

UNITED KINGDOM: Texas Instruments Ltd., Manton Lane, Bedford, England, MK41 7PA, (234) 270 111.

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